Maintaining quality of results with shift-left for DFT

ITC2023

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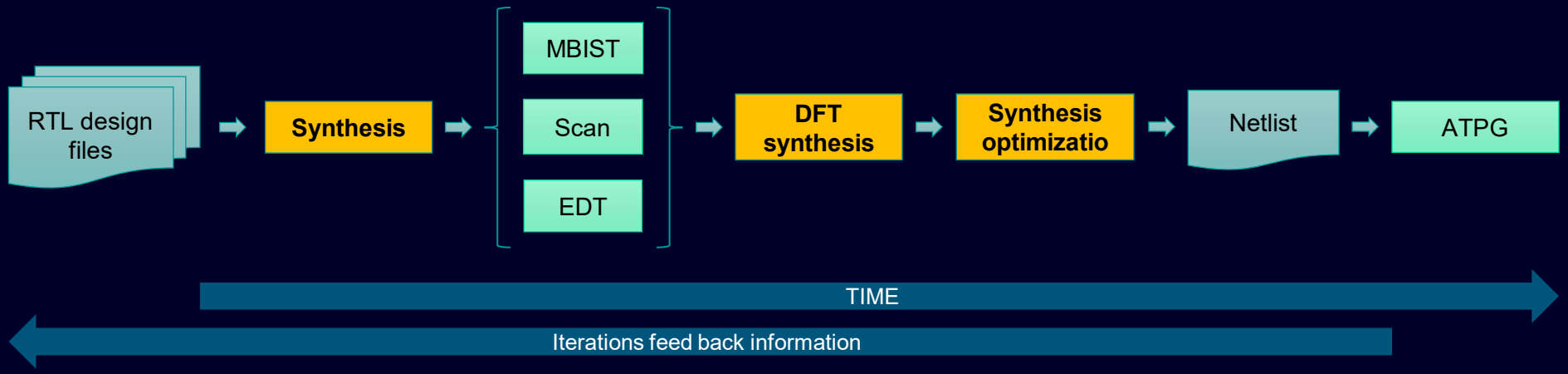
What is “Shift-left” for DFT?

DFT industry has changed

DFT was once implemented on gate-level designs

- Required multiple synthesis steps for the design and added DFT logic, increasing turn-around time
- Optimization was performed separately to fully integrate the design and DFT logic
- ATPG is only possible after a fully synthesized design is available



Design sizes grew and these steps took increasing amounts of time and iterations

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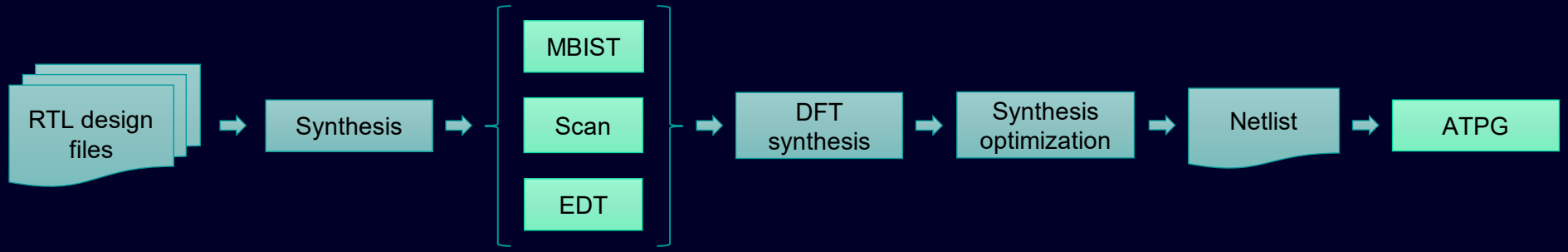
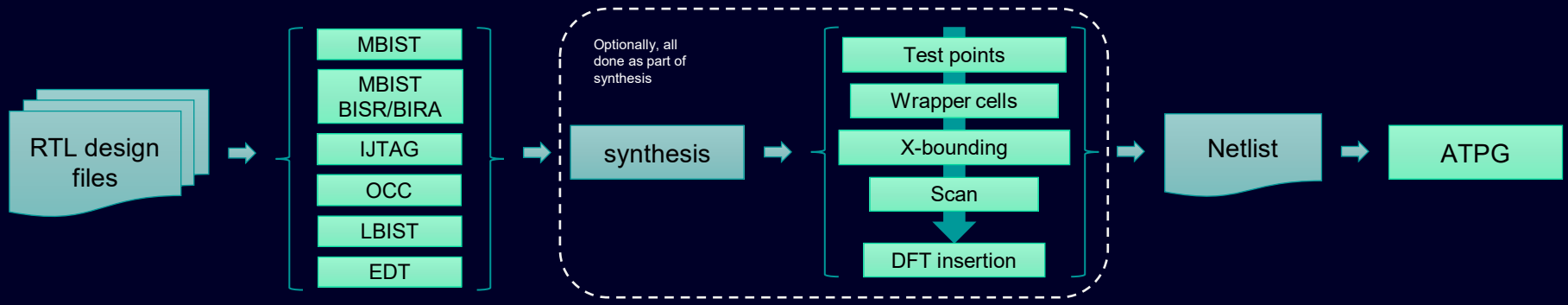
Design growth and time-to-market (TTM) pressures led to shift-left methodologies

While content and iterations have grown, industry has condensed time-to-market requirements

DFT, and the design process in general, has gradually shifted from this:



To this:



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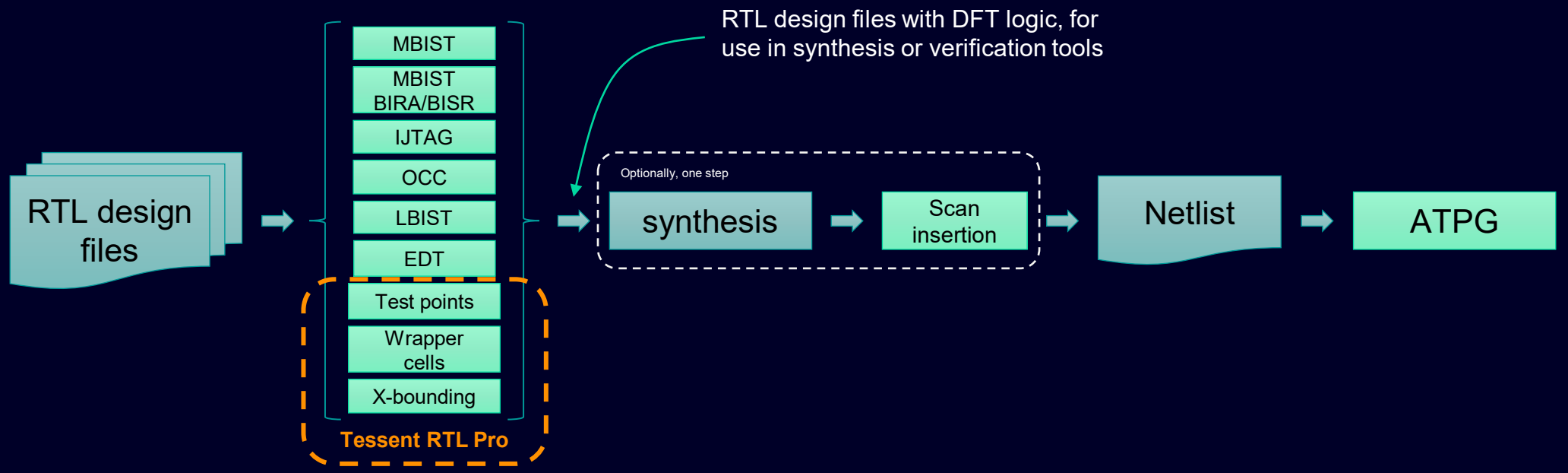
Industry challenged to fully shift-left

To be complete, shift-left for DFT must encompass remaining gate-level tasks

- X-bounding logic, wrapper cells, and test points
- Scan stitching requires a netlist and remains a gate-level task

RTL insertion of DFT logic allows synthesis to optimize results, improving timing and area estimates



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RTL challenges and solutions for DFT

RTL DFT needs

RTL Testability Analysis	➢ RTL complexity analysis ➢ RTL design rules checking / DFT Lint ➢ Test point, wrapper cell, and x-bounding analysis ➢ Test coverage & pattern count estimation

RTL Design Editing	➢ Design-for-Test logic insertion
	  ➢ MBIST, EDT, SSN, LBIST, OCC, IJTAG
	  ➢ Test points, wrapper cells, x-bounding
	➢ Structured / scripted design editing & testability fixing
	➢ Maintain look and feel of original RTL

RTL DFT Verification	➢ DFT simulation and verification
	  ➢ IJTAG, LBIST, & SSN continuity checking
	  ➢ MBIST operation set (opset) verification

Benefits of using Tessent Shell for shift-left flows

All Tessent DFT products use the same platform for logic Insertion

- Information is exchanged between tools using Tessent Shell DataBase (TSDB)

Same commands used throughout the tools

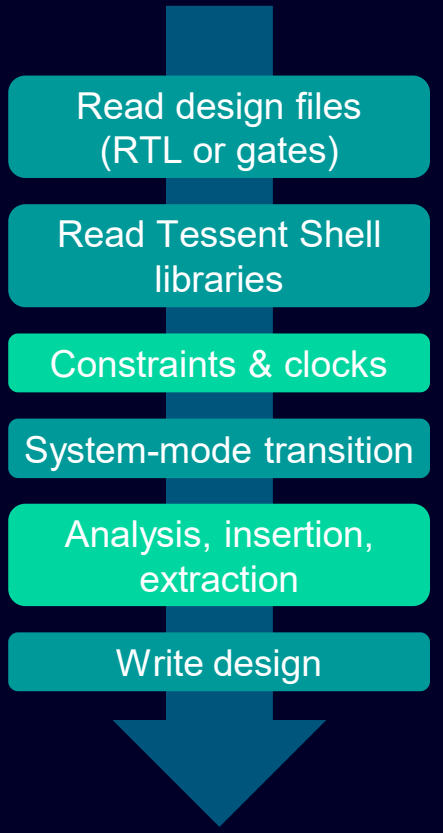
- Tcl-based environment supports highly-scripted environments

Catch testability issues early while inserting DFT logic

- RTL DRCs are run automatically based on logic being inserted

All Tessent DFT logic may be created as RTL, except scan

- E.g. Tessent TestKompress, Tessent MemoryBIST, Tessent LogicBIST, etc.



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Inserting Tessent DFT logic at RTL

RTL test points with Tessent RTL Pro

New context for RTL test points

- `set_context dft -test_points -rtl`

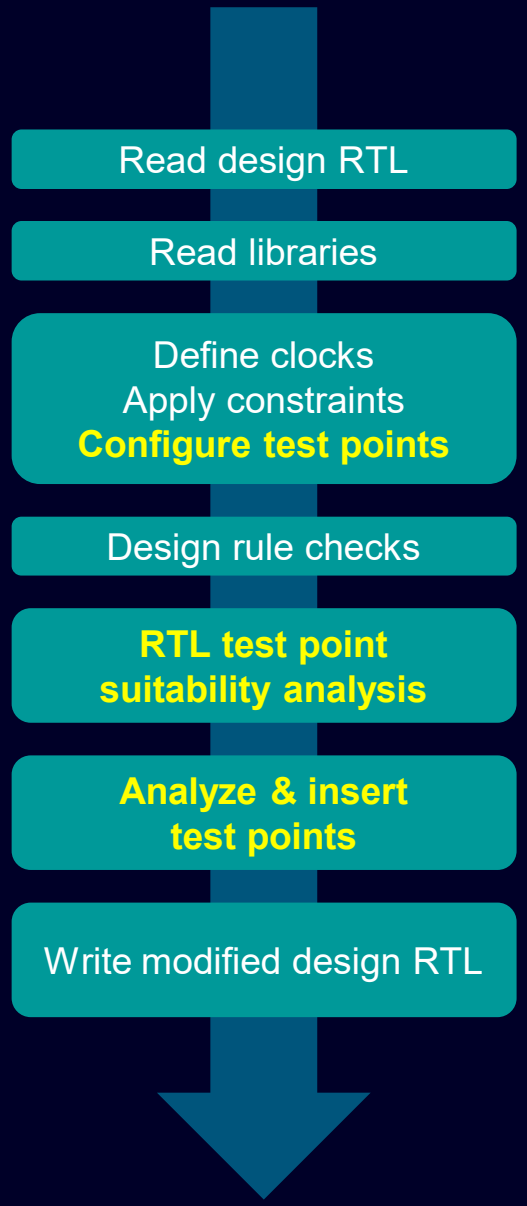
Follows the same, general Tessent logic insertion flow

New RTL suitability and complexity reporting

- `report_rtl_complexity`

Test point analysis based on quick-synthesis view; locations mapped to RTL

- Read the design RTL
- DRC & quick synthesis
- Test point analysis, mapping, and insertion
- Write the modified design RTL



RTL complexity and test point suitability

New functionality developed for complexity and suitability reporting of RTL circuits

- Analysis of RTL to gauge complexity of RTL structures
- Analysis of RTL design suitability for test points

Complexity analysis and reporting

- Feed information about the circuit back to RTL designers about complexity of the RTL
- Hierarchical analysis and reporting of structures such as control logic, functional blocks, constant and floating pins

RTL test point suitability

- Fast, structural analysis to gauge design suitability for insertion of RTL test points
- Optional, high-effort analysis based on test point analysis output, measured against editable nodes of the design

RTL complexity and test point suitability

Design knowledge: RTL complexity score

- Detailed understanding about the structure of the design RTL
- Additional details about design & library profiling helps better understand RTL structures

Quality of results: test point suitability score

- Design analysis to determine if RTL structures are suitable for RTL test point insertion

```
================================================================================
Overall Complexity SCORE                    : Low RTL complexity
================================================================================
Overall Test Point Suitability              : High
================================================================================
Overall design profile
    RTL modules                             : 433 (95.37%)
    Structural modules                      : 5 (1.10%)
    Black boxes modules                     : 16 (3.52%)
    Total design instances                  : 6270
    High expression depth                   : Instances=12.17%, Area=52.32%
    Medium expression depth                 : Instances=3.85%, Area=10.93%
    Low expression depth                    : Instances=83.98%, Area=36.75%
================================================================================
```

RTL test point results versus gate-level with TestKompress ATPG

			Baseline		Gate-level test points			RTL test points			
Design ID	Design gates	Scan cells	Test Coverage	Patten Count	Test Points	P.C. @ Base	P.C. Redux	RTL TP Suitability	Test Points	P.C. @ Base	P.C. Redux
D1	1.12M	44k	93.1	8387	943	3071	**63.4**	**High**	942	4799	**43**
D2	3.4M	150k	94.9	2579	3031	704	**72.7**	**High**	2969	960	**63**
D3	0.57M	22k	96	18560	439	8743	**53**	**Medium**	439	8932	**52**
D4	5.3M	255k	97.32	10291	5088	4717	**54**	**High**	5064	6130	**40.5**
D5	1.2M	43k	99.26	18526	861	11102	**40**	**High**	861	11006	**40.6**
D6	10M	440k	93.7	29256	3777	23618	**19.3**	**High**	**1305**	13169	**55**
D7	3.7M	208k	98.27	10125	4299	7194	**29**	**High**	4291	7923	**22**
D8	1.74M	119k	95.49	14217	2386	5788	**59.3**	**High**	2386	8516	**40**
D9	3.4M	103k	96.66	63381	2099	38133	**40**	**High**	2099	43317	**32**
D10	9.36M	458k	98.61	8226	9774	5808	**29.4**	**Medium**	7322	6463	**22**
D11	10.6M	739k	99.08	14238	14822	9787	**31.3**	**High**	14849	9970	**30**
D12	4M	222k	99.32	16584	4497	10005	**39.7**	**High**	4343	9395	**43.35**

Summary

Shift-level methodologies are driving DFT implementation earlier in the design process

Tessent DFT logic creation and insertion is possible for all DFT except scan chains at RTL

- Tessent reads RTL and writes RTL, preserving the look and feel for easier debug

Tessent provides quality metrics to determine whether design RTL is suitable for RTL test points

- Allows designers to make informed choices & understand if downstream results don’t match expectations

Thank you

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