Tessent Streaming Scan Network Implementation for Renesas Heterogeneous Multi-Core SoC

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About Renesas Electronics Corporation

Our mission is to develop a safer, healthier, greener, and smarter world by providing intelligence to our four focus growth segments: Automotive, Industrial, Infrastructure, and IoT that are all vital to our daily lives, meaning our products and solutions are embedded everywhere.

Automotive	**Industrial**	**Infrastructure**	**IoT**
Highly reliable vehicle control, safe and secure autonomous driving, Eco-friendly electric vehicles	Lean, flexible and smart industry	Robust infrastructure, enabling safety and efficiency	Comfortable, safe and healthy lifestyles through IoT

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# Outline

1. **Challenges of DFT for Heterogeneous SoC**

2. **SSN Implementation method for Heterogeneous SoC**

3. **Conclusion**

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Market Trend of Test time

- Increasing test time with increasing circuit size

  - Exponential increase

    – Several dozen times in 15 years

    – Nearly tripled in the last 4 years

- We need to reduce test time and test data volume, without compromising test quality

Typical Test Time Expectations
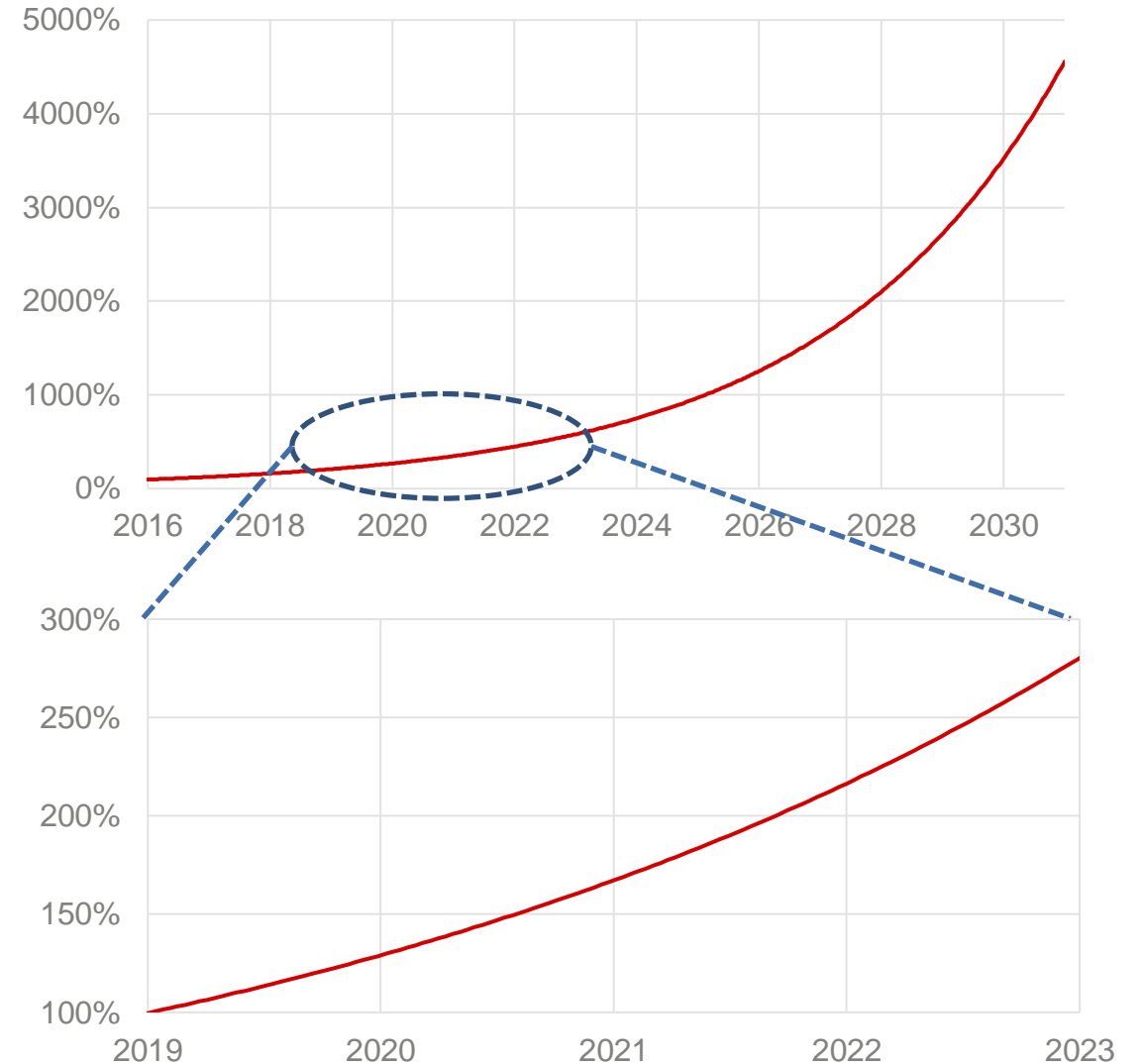
2019 Heterogeneous Integration Roadmap prediction of test time growth
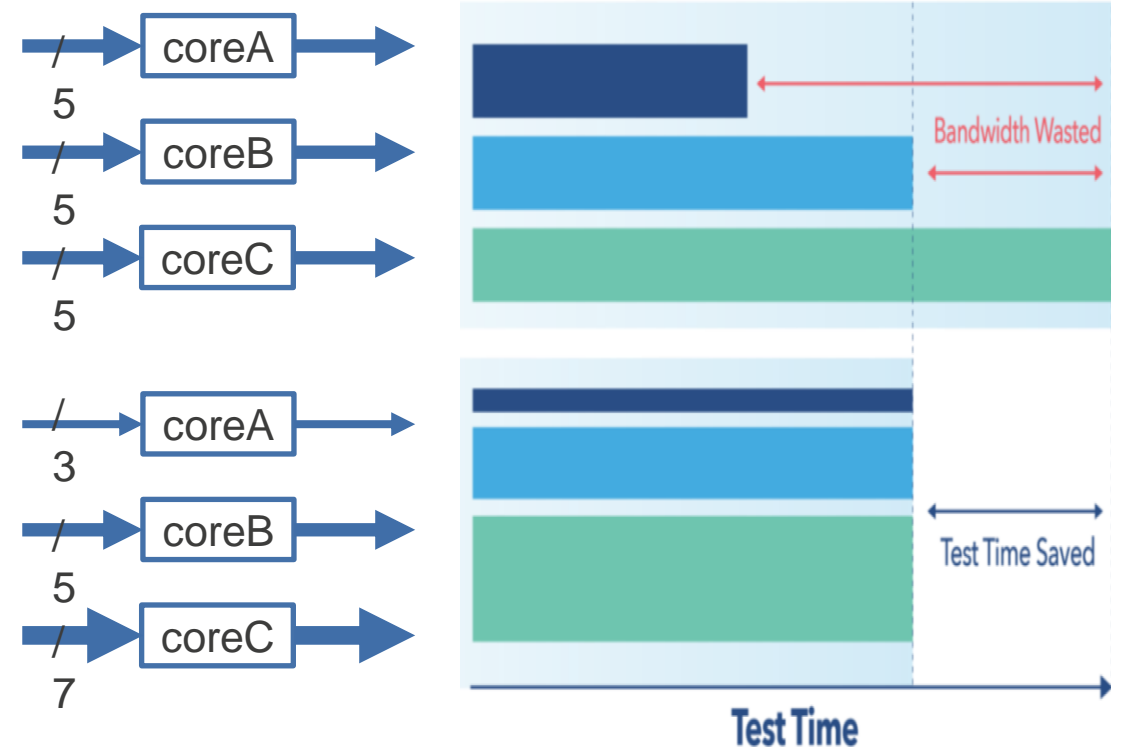https://eps.ieee.org/images/files/HIR_2023/ch17_test.pdf

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Legacy Hierarchical DFT Method

- **Design Specification of Renesas Previous generation SoC**

  - 50+ hierarchical DFT Cores

  - About 210 scan I/O pins (input 160/ output 50)

    – Pin-mux structure is used

  - Low power process

  - Test frequency 66 MHz
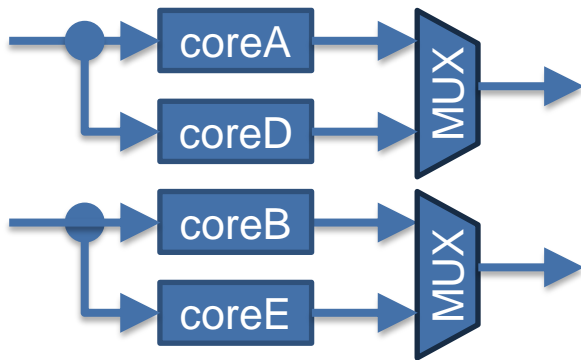
Pin-Mux Design

Test Time Optimization of Pin-MUX design

Manual optimization of the configuration is tool hard

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Latest Renesas SOC Design Specification

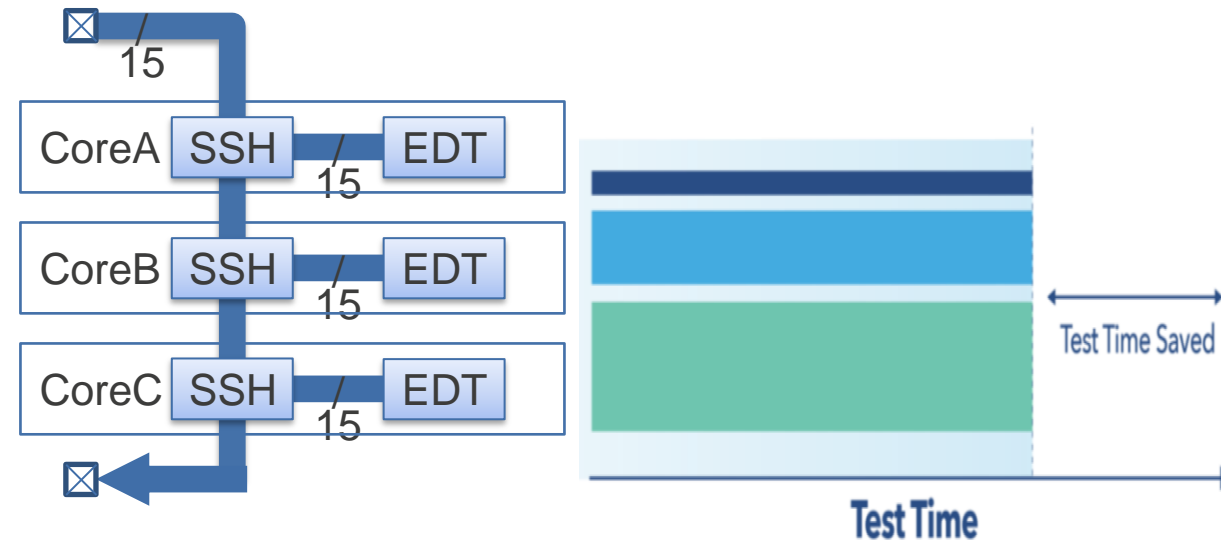- **Design Specification**

  - More than 200 hierarchical DFT Cores

  - 200+ scan IO pins (distributed around the chip)

  - Low power process

  - Need to speed up test frequency (target 2x) for test time reduction

- **What is suitable DFT method for this design?**

  - Pin-Mux is no longer applicable

  ⇒ **Tessent Streaming Scan Network (SSN)**

Tessent Streaming Scan Network

Streaming Scan Host (SSH) automatically allocates the bandwidth optimized for each core
⇒ The iterative implementation is unnecessary
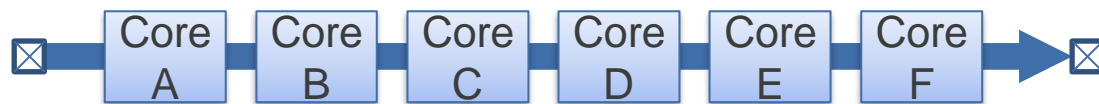
Challenges of SSN Implementation

SSN data bus configuration

- Multiple SSN data bus: less burden on layout

- Single SSN data bus: more effective to test time

⇒ Implemented the latter, prioritizing test time
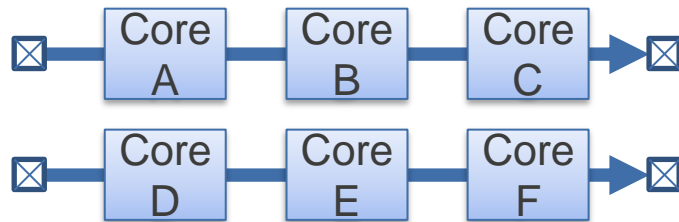
Multiple SSN data paths

Single SSN data path with wide bit-width

Challenges on implementing single SSN data bus for the effective test time reduction

1. Reducing clock skew at IO boundary for faster clock

2. Wiring from IO to configure large bit-width

3. Guaranteeing timing between asynchronous modules (E.g. located at the different power domains)

The clock skew affects the fast operation

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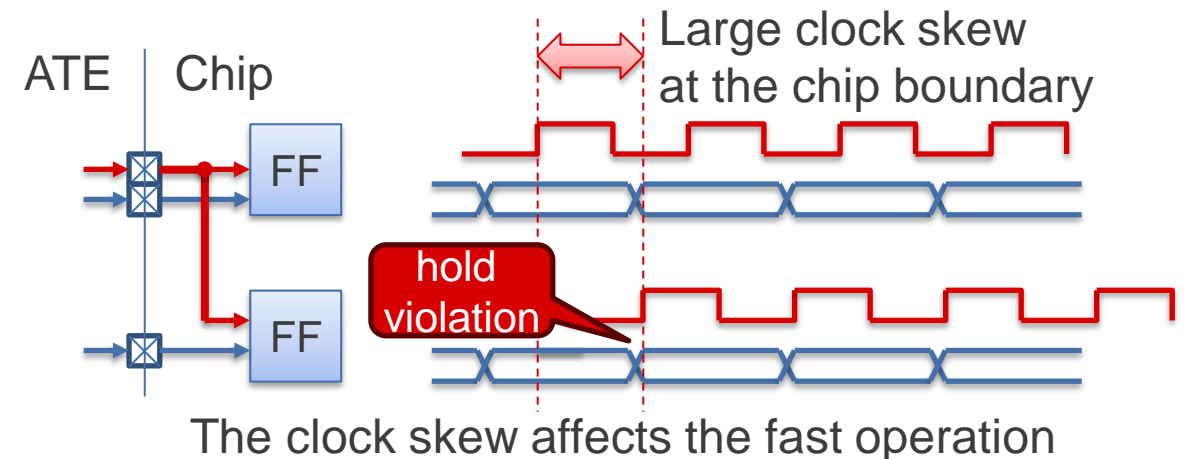
Challenge 1 : Reducing clock skew at IO boundary for faster clock

- More than one SSN clock is assigned in accordance with the placement of PAD logic

- The clock skew between internal and external clocks is tolerated with SSN FIFO

⇒ **The 2x faster clock is expected to be applied by this structure**
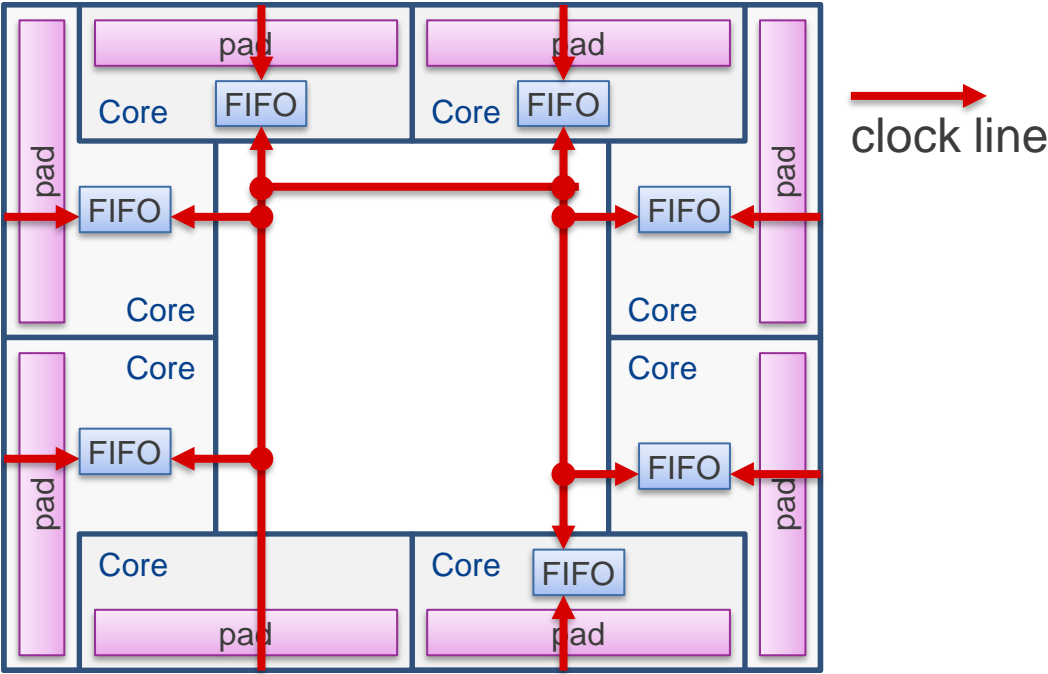
PAD logic location and ssn_bus_clock connection
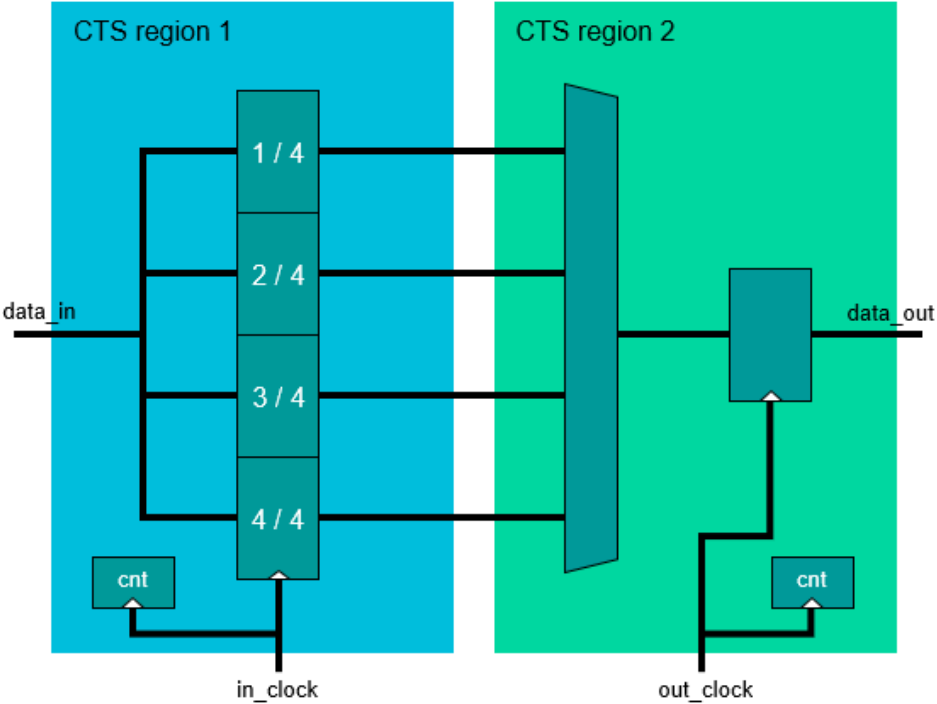
SSN FIFO Structure

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Challenge 2 : Wiring from IO to configure large bit-width

- **Convergence and branch structure allows the large SSN bit-width by exhausting available IOs**

  - The SSN data paths are bundled into one from each PAD logic for input

  - After passing through all the SSH, the data paths are distributed to each output PAD logic for output
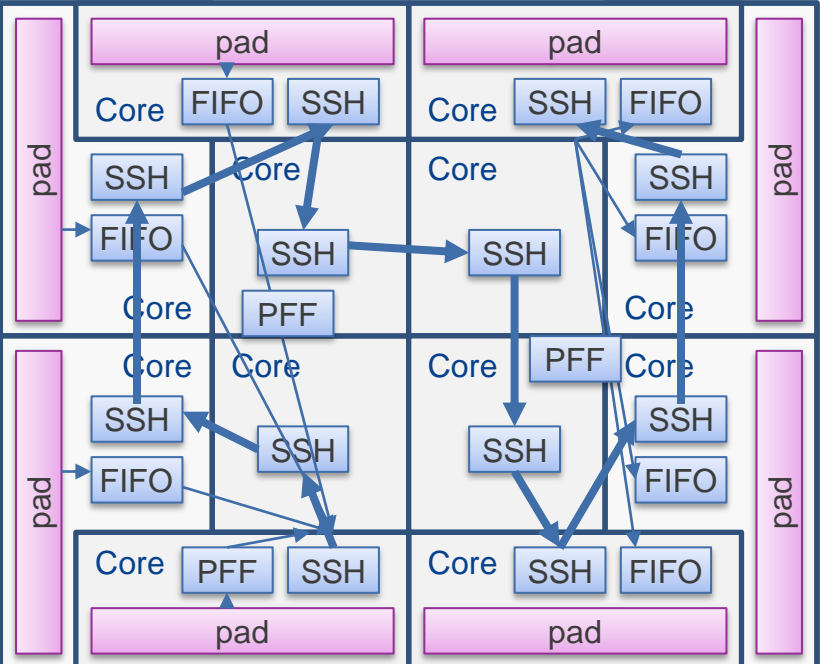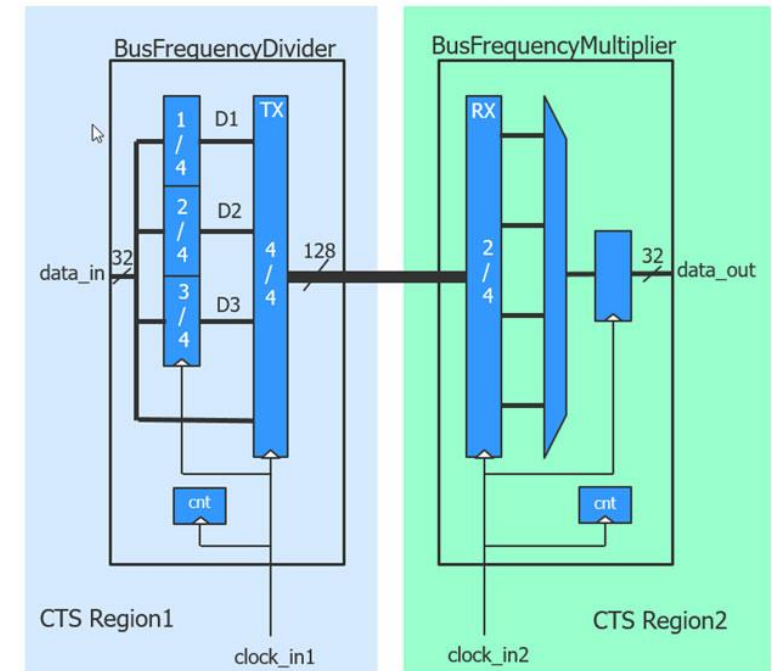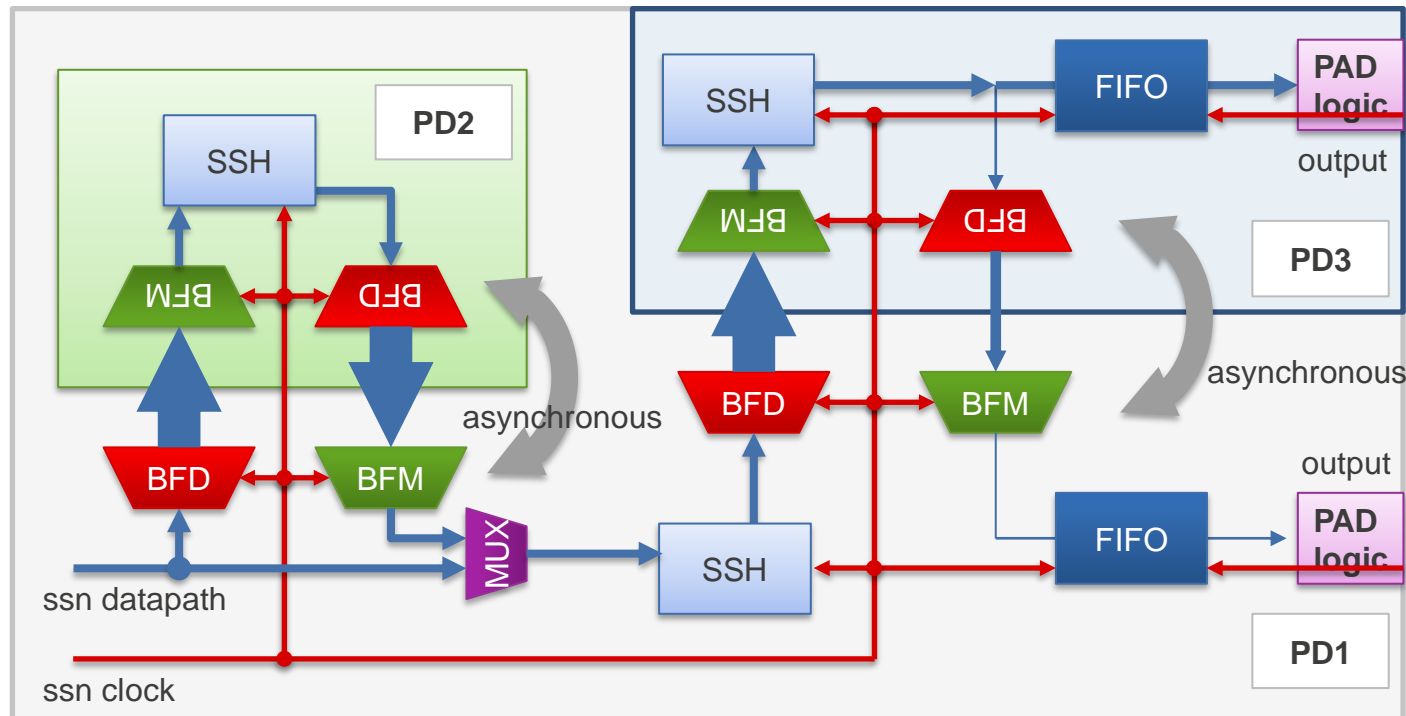

PAD logic location and datapath connection
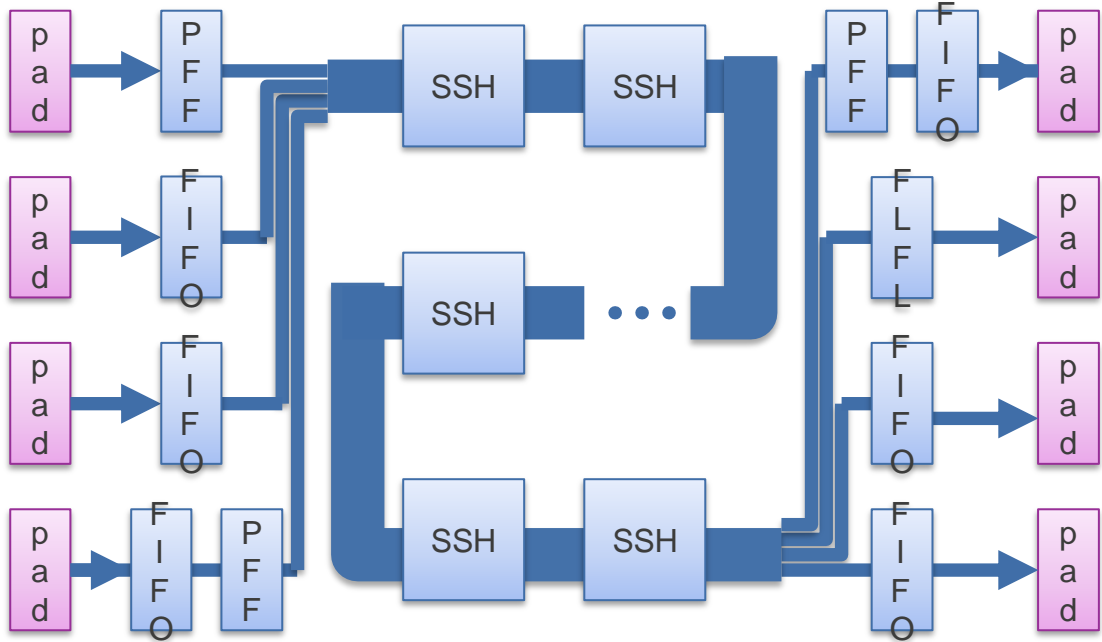
Schematic diagram

PFF : SSN Pipeline FF

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Challenge 3 : Guaranteeing timing between the asynchronous modules

- Bus Frequency Divider (BFD) and Bus Frequency multiplier (BFM) are placed between asynchronous modules, e.g. different Power Domains

⇒ **The data rate is guaranteed between asynchronous modules**

An example of BFM and BFM

Conclusion

- **Renesas guarantees high quality testing without compromising test patterns**

  - Tessent SSN is a practical solution for reducing test time and test volume

    - It can support the complex SoC by utilizing the mechanism
      that achieves the high-speed operation and facilitates the timing closure

    - 2x faster test clock frequency is expected to be achieved in our design

- **Expectations for Siemens EDA**

  - Advanced automation of SSN Implementation

    - E.g. automated connection order between cores
      by leveraging the layout information and the power specification (DEF, UPF/CPF)

  - Comprehensive solution to reduce design work, chip area and test costs
    through consistent Tessent design flow with shift-left initiatives

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