DFT Clock Generation Methods for Packetized Scan Data Designs

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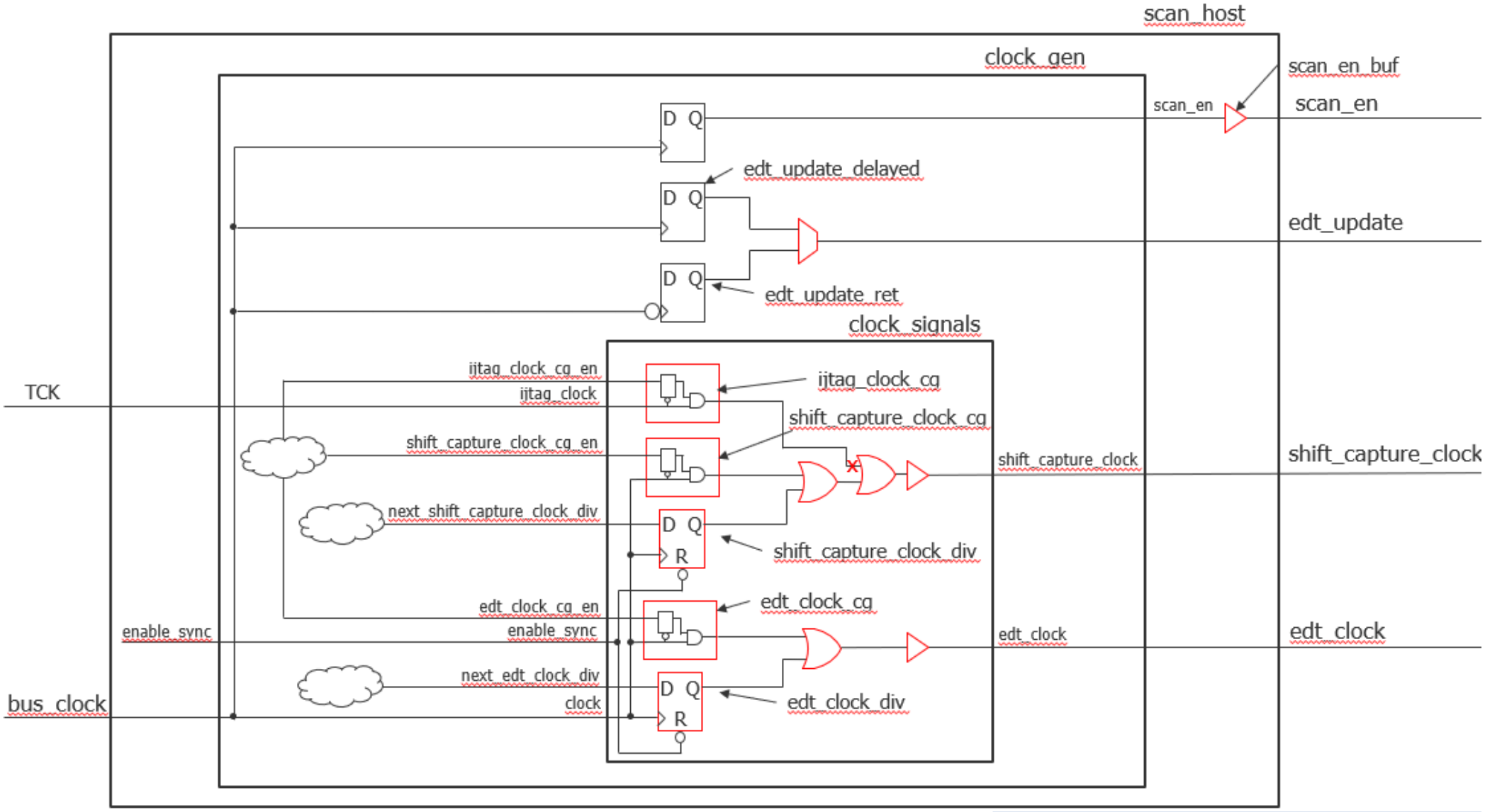
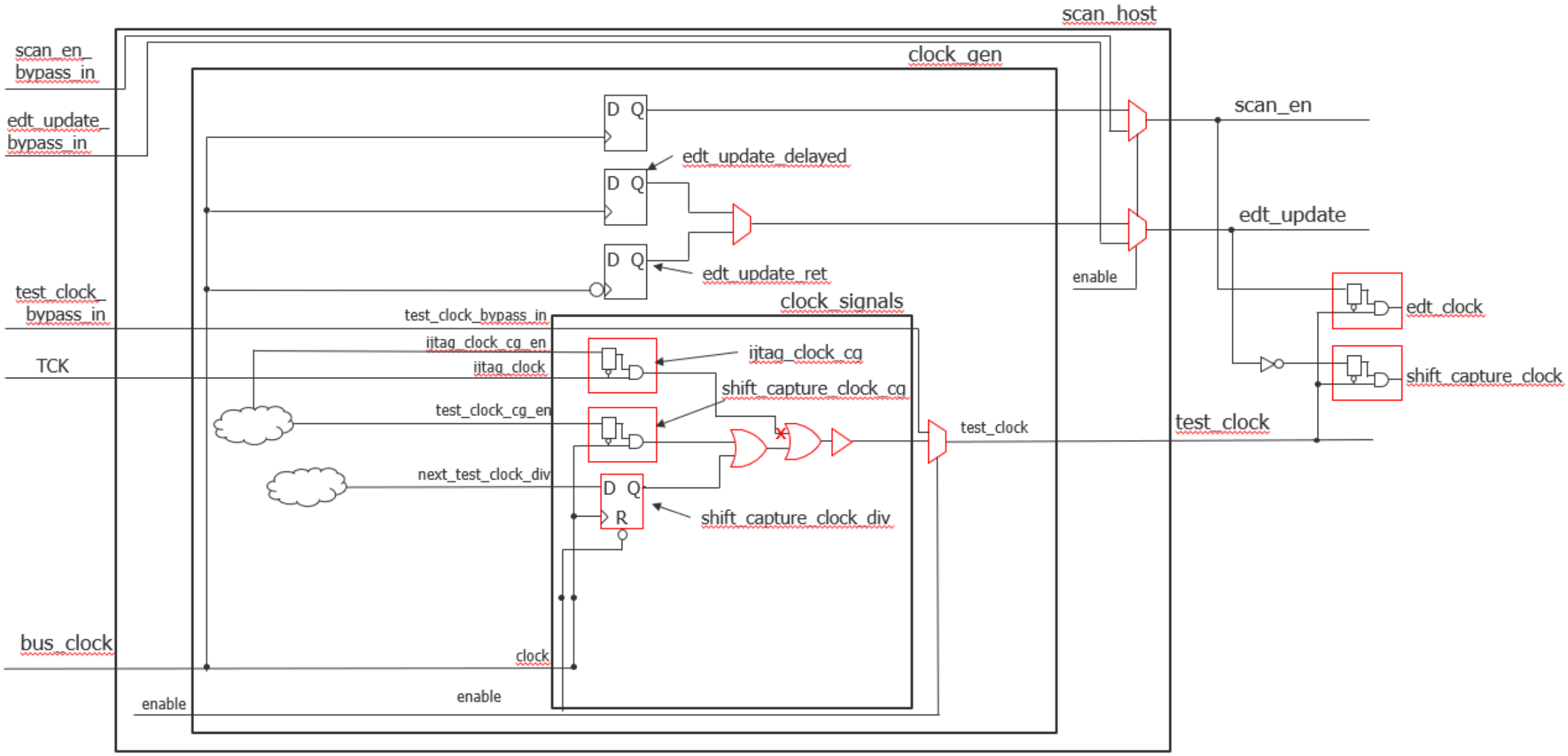
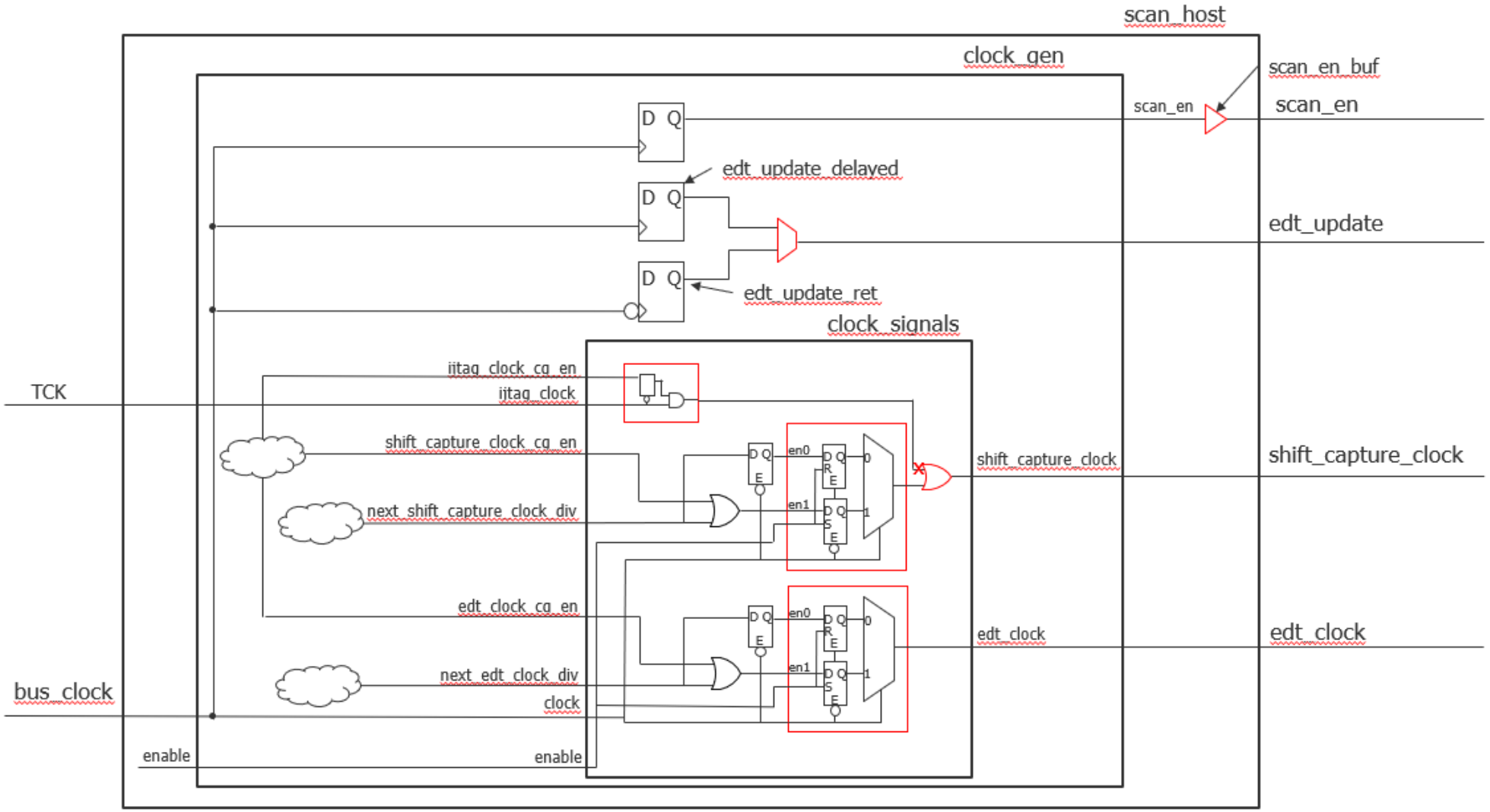
Method 1: Streaming Scan Host using Clock Gaters and Dividers to generate scan clocks



Method 2: Streaming Scan Host using Clock Gater and Divider for test_clock (clock-gaters/scan control signals to generate scan clocks)

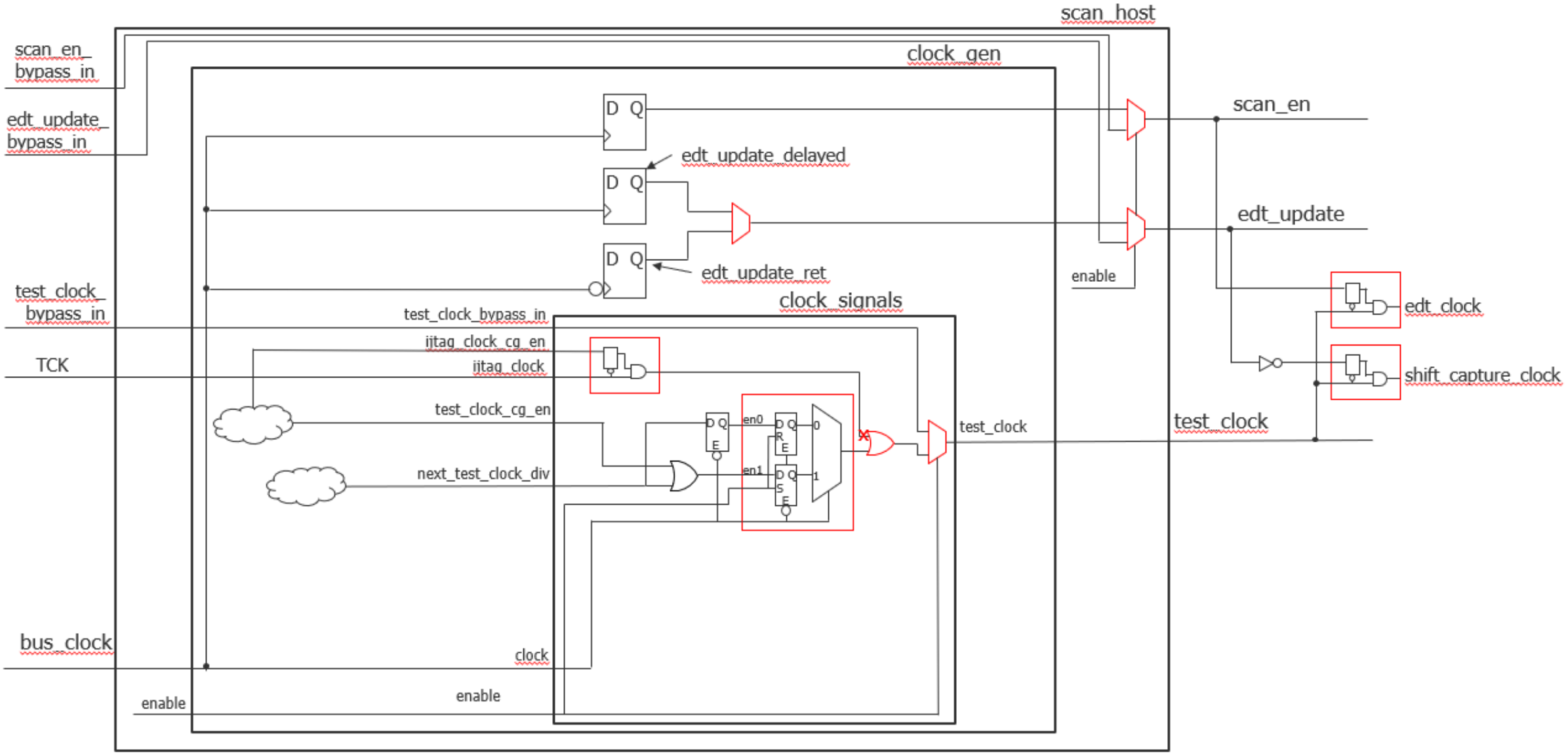


Method 3: Streaming Scan Host using a Clock Shaper Cell to generate scan clocks



Method 4: Streaming Scan Host using Clock Shaper for test_clock

(clock-gaters/scan control signals to generate scan clocks)



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Summary

Method	Clocking Method Description	Advantages/Disadvantages
1	Clock Gaters/Dividers-→ shift_capture_clk, edt_clk	• Simple standard cells used • Disadvantage: Reconvergence of clocks
2	Clock gaters/Dividers→ test_clock→ shift_capture_clk, edt_clk	• Better timing w/ clock gating cells more local • Only test clock needs to be balanced • Disadvantage: Reconvergence of clocks
3	Clock Shapers→ shift_capture_clk, edt_clk	• Single timing arc • No timing reconvergent paths
4	Clock Shapers→ test_clock→ shift_capture_clk, edt_clk	• Clock Shaper allows to have any clock waveform for a packetized data delivery mechanism • Single timing arc, No timing reconvergent paths • Fewer SDC constraints and clock definitions • Recommended clocking methodology