SIEMENS
Ingenuity for life

MemQuest memory compiler

Siemens Digital Industries Software

Benefits

- Cloud-based solution, no local software to install
- Industry's easiest memory selection GUI aids optimizing your memory configuration based on area, speed, and power requirements
- Single GUI management of your Memory IP portfolio
- Full simulation verification for each compiled instance
- Instant generation and downloading of datasheets and FE kits
- Offers a wide range of column mux and multi-bank memory configurations
- Industry's lowest power search, based on patented ripple bitcell architecture
- High speed achieved through short segmented match lines, no sense-amplifier
- Easy pipelining to achieve high frequency for wide search words

The engine driving the Siemens family of embedded memory IP is MemQuest, an advanced compiler-based memory generator and optimizer. This powerful memory compiler and optimization environment is cloud-based, so there is no local software to support and maintain. It is also easily accessible using your existing Siemens support ID.

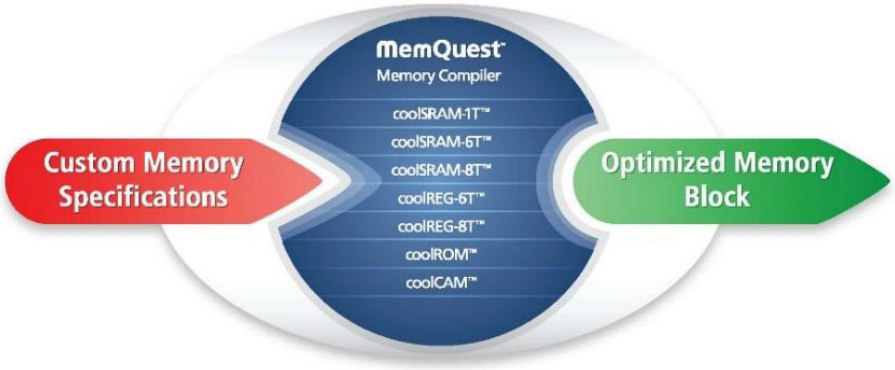
MemQuest provides a home page for each customer project to organize and quickly view all the memory IP selected for each chip. A new memory is added to the project by selecting the desired depth and width, as well as other additional features.

One can then select the desired option from a table, sortable by area, speed, and power, of the available configurations.

Once a configuration is chosen, the corresponding datasheet can be immediately downloaded, and a front-end kit can be generated. The back-end kit is available as soon as the IP completes a comprehensive verification performed on Siemens cloud servers and using Siemens EDA verification tools.

Using MemQuest, you can easily find and generate the optimum macro for your application from across the entirety of Siemens' Memory IP product line.

The Siemens compiler-based family of advanced embedded memories include low-power, high-speed, config-urable TCAM and BCAM targeting the most demanding SoC applications.



MemQuest memory compiler

Benefits *continued*

- Compiler driven to provide arbitrary number of rows and columns
- Freely mix TCAM and BCAM in a single macro
- Single-cycle search provides match output before the next rising clock edge
- Optional single-and multi-hit detection
- Match-row address output
- Provided with Tessent custom CAM memory BIST algorithm
- Range
- Up to ¼ Mbit
- Up to 1024 entries
- Up to 256 wide search word
- Easily combine macros for larger search tables
- Standard CMOS with no extra process, layer, or mask
- Save up to 50% area compared to SRAM-6T
- Portable between foundries
- Ultra low leakage compared toSRAM-6T
- Silicon proven in 180nm-65nm
- Compiler driven to generate arbitrary size macro
- SRAM style synchronous interface with single-cycle full random access
- Compiler driven to match arbitrary size requirement

Embedded CAM blocks are user-definable for organization and performance depending on your requirements.

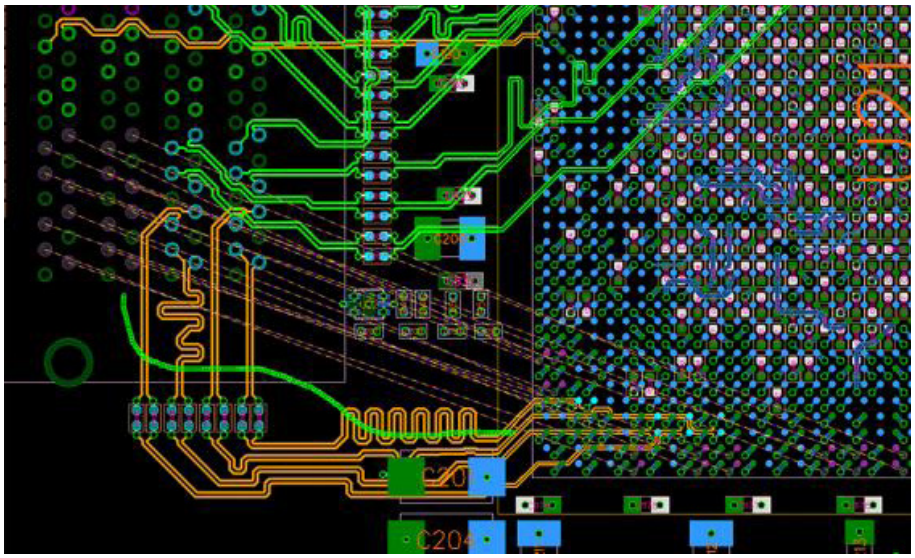
The coolCAM family is based on a patented ripple bitcell architecture providing breakthrough low power performance for search operations. During search operations, a mismatch in the LSB portion of a word automatically disables the search for the remaining portion of the word, reducing the overall power dissipation.

The standard coolCAM configuration provides a match line output for every CAM word. The coolCAM operates synchronously on a rising clock edge and the search or read output is available before the next rising clock edge. Separate coolCAM macros can be directly stitched together to seamlessly and automatically pipeline the search operation of wide words while maintaining a high search bandwidth.

Powerful features (available on request) include single- and multi-hit detection, match-address output, and row redundancy. Additionally, coolCAM is tightly supported by Tessent memory BIST.

Behind this breakthrough in embedded memory is MemQuest™, an advanced compiler-based memory generator and optimizer. Use MemQuest to easily find and generate the optimum macro for your application across our entire memory IP product line.

The Siemens compiler-based family of advanced embedded memories includes low-power, high-speed, configurable Single Transistor SRAM targeted for the most demanding SoC applications. Large scale embedded memory blocks are user-definable for organization and performance depending on your requirements.



coolSRAM

Benefits *continued*

- Column-mux selection for optimal aspect ratio
- Optional column redundancy
- Wide I/O bus for high bandwidth
- Bit / Byte writable
- Compatible with Tessent memory BIST
- Range
- Up to 4 Mbit
- Up to 64K entries
- Up to 576 wide IO bus
- Single-port Synchronous SRAM based on the foundry 6T bitcell
- Megabit scale blocks
- Best-in-class Area vs Performance figure of merit
- Multi-mux (2-32) and Multi-bank (1-8) configurations are available
- High density custom layout and attention to DFM rules
- Internal clock-gating for low dynamic power
- Single-port Synchronous SRAM optional column redundancy for large macros, compatible with Tessent MBIST
- Solution for reducing routing congestion
- Two-port emulation
- Leakage power management reduces leakage current by more than 50% while memory is fully active

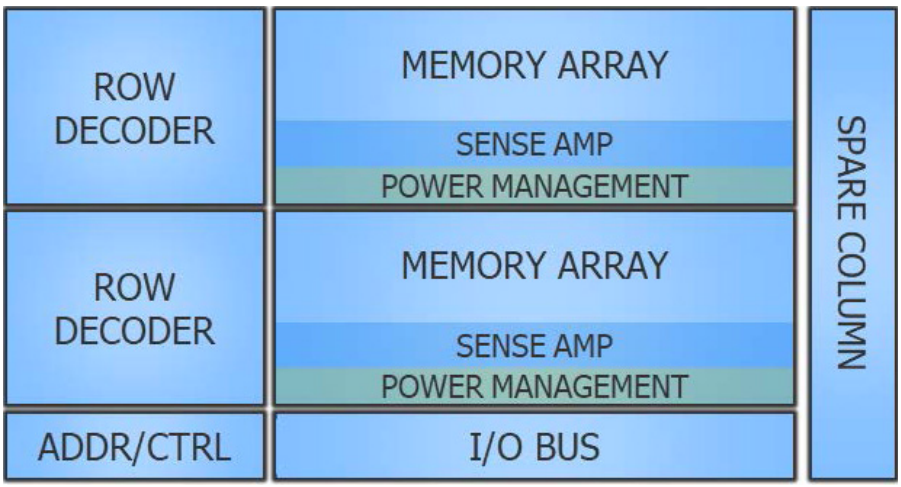
The coolSRAM-1T family provides SRAM style memory at up to 50% area savings in standard CMOS with no additional process, layer or mask. Because it is fully CMOS compatible, there is no process to qualify, and the IP is easily portable across foundries. This IP is targeted for applications requiring several megabits of on-chip memory, although the area benefits can be obtained on macros down to ½ Mbit.

Each coolSRAM-1T instance is generated by a compiler to match specific customer requests for word depth and width, and is available with several column multiplexing options to provide aspect ratio control. Optional column redundancy is available to guarantee maximum yield. The bit- and byte-writable feature enables the use of a wide IO bus to maximizing bandwidth while reducing clock rate.

Behind our family of embedded memory is MemQuest, an advanced compiler-based memory generator and optimizer. MemQuest can easily find and generate the optimum memory macros for your application across the entire Memory IP line.

The Siemens compiler-based family of advanced embedded memories includes low-power, high-speed, configurable Single-port SRAM targeting the most demanding SoC applications. Embedded memory blocks are user-definable for organization and performance depending to best meet the application requirements.

The coolSRAM-6T family uses proprietary and patented circuit and layout techniques to achieve the lowest power and highest speed specifications in the industry while providing cost savings through reduced silicon area.



coolSRAM

Benefits *continued*

- Optional HVT to further reduce leakage
- Low-leakage retention mode
- Custom library characterization at low voltage
- Split supply for low-voltage periphery
- Integrated level shifters and power switches
- Lowest total power solution with internal clock-gating and leakage-power-management (LPM)
- High speed and high frequency based on edge-based clocking techniques
- High density achieved with custom layout and attention to DFM rules
- Best-in-class area vs performance figure of merit
- FlexPort allows independent choice of Read (R), Write (W), or Read/Write (RW) for each port
- Optional M4 routing channels through the macro to reduce routing congestion
- Automatic transparent leakage power management reduces leakage current while maintaining data retention
- Bit / Byte writable
- Compatible with Tessent memory BIST
- Range
- Up to 360 Kbit
- Up to 40K entries
- Up to 144 wide IO bus

Optionally column redundancy that is compatible with Tessent MBIST, is also available. Column redundancy can increase the yield related to bitcell defects and is recommended for applications integrating several Mbits or more of embedded memory. Tessent MBIST and coolSRAM-6T provide a complete built-in self-repair solution in conjunction with a 3rd party nonvolatile storage solution.

Available M4 routing channels through the IP relieves routing congestion at the system level, can facilitate timing closure by providing shorter data path routes. This translates to system level area and power savings.

The Leakage Power Management (LPM) optional feature transparently reduces leakage current by 50% or more in the bitcell array and periphery while the memory is active, often eliminating the need to support special standby modes. An additional ultra-low-leakage retention mode can further reduce leakage when the application knows the memory will be idle for long periods of time.

The coolSRAM-6T architecture supports a standard bit- and byte- writable feature.

The standard compiler provides a standard-VT periphery with the highest density bitcell offering from the foundry. Multi-VT periphery and high-current bitcell support are also available to meet extreme performance or leakage needs.

The architecture is also suitable for the emulation of two-port memories, providing 50% area reduction and 30% leakage reduction against a traditional 8T based two-port IP

The Siemens compiler-based family of advanced embedded memories includes low-power, high-speed, configurable Dual/Two Port SRAM targeting the most demanding SoC applications. Embedded memory blocks are user-definable for organization and performance depending on your requirements.

coolSRAM and coolREG

Benefits *continued*

- Low power solution minimizes internal switching
- Long channel bias reduces leakage
- High speed and high frequency based on edge-based clocking techniques
- High density achieved with custom-layout and attention to DFM rules
- Best-in-class area vs. performance figure of merit
- Optional M4 routing channels through the macro to reduce routing congestion
- FlexPort allows independent choice of Read (R), Write (W), or Read/Write (RW) for each port for coolREG-8T
- Bit / Byte writable
- Optional LVT/HVT in the periphery for extreme speed or ultra-low leakage
- Compatible with Tessent memory BIST
- Range
- Up to 72(6T) 36(8T) Kbit
- Up to 2K(6T) or 1K(8T) entries
- Up to 144 wide IO bus
- Save 30%-50% area
- Zero bias core and leakage power management for ultra-low-leakage
- Best-in-class area vs performance figure of merit
- Innovative, reliable bitcell architecture
- M1 (or M1/CO) programmable
- Programming script delivered with IP
- Compatible with Tessent memory ROM BIST

Our coolSRAM-8T family is designed around the foundry 8T bitcell and provides fully independent clocks and I/O bus for each port. FlexPort technology allows each port to be independently defined as a Read (R), Write (W), or Read/Write (RW) port.

Advanced circuit techniques result in the highest density macros and simultaneously achieving high performance, while long channel biasing reduces standby leakage current.

Differentiating options include M4 routing channels to reduce routing congestion, and automatic leakage power management (LPM) to transparently reduce leakage current in the core array and periphery. Other available features are optional column redundancy, bit- and byte- writable macros, and a large selection of column mux to optimize the aspect ratio.

Behind Siemens breakthrough embedded memory is MemQuest, an advanced compiler-based memory generator and optimizer. Use MemQuest to easily find and generate the optimum memory macros for your application across our entire memory IP product line.

The Siemens coolREG family of advanced embedded memories includes low-power, high-speed, configurable Single and Dual/Two Port Synchronous Register File

The coolREG-6T/8T families' proprietary and patented circuit and layout techniques achieve the lowest power and highest speed specifications in the industry while providing cost savings through reduced silicon area.

The coolREG-8T family is designed around the foundry 8T bitcell and provides fully independent clocks and I/O bus for each port. FlexPort technology allows each port to be independently defined as a Read (R), Write (W), or Read/Write (RW) port.

Differentiating features include M4 routing channels to reduce routing congestion, and optional use of LVT/HVT in the periphery for extreme speed or ultra-low leakage.

coolROM Family

Benefits *continued*

- Up to 2 Mbit
- Up to 128K entries
- Up to 256 wide IO bus
- Best-in-class area vs performance figure of merit
- Optional M4 routing channels through the macro to reduce routing congestion
- FlexPort allows independent choice of Read (R), Write (W), or Read/Write (RW) for each port for coolREG-8T
- Bit / Byte writable
- Optional LVT/HVT in the periphery for extreme speed or ultra-low leakage
- Compatible with tessent memory BIST
- Range
- Up to 72(6T) 36(8T) Kbit
- Up to 2K(6T) or 1K(8T) entries
- Up to 144 wide IO bus
- Save 30%-50% area
- Zero bias core and leakage power management for ultra-low-leakage
- Best-in-class area vs performance figure of merit
- Innovative, reliable bitcell architecture
- M1 (or M1/CO) programmable
- Programming script delivered with IP
- Compatible with Tessent memory ROM BIST
- Range
- Up to 2 Mbit
- Up to 128K entries
- Up to 256 wide IO bus

Our coolROM family of advanced embedded memories includes low-power, high-speed, configurable Read-Only Memory.

The coolROM family uses proprietary and patented circuit and layout techniques to achieve the lowest power and highest speed specifications in the industry while providing cost savings through reduced silicon area.

Differentiating options include M4 routing channels to reduce routing congestion, and automatic leakage power management (LPM) to transparently reduce leakage current in the core array and periphery. Other available options are optional column redundancy, and bit- and byte-writable macros.

The standard compiler provides a standard-Vt periphery with the highest density bitcell offering from the foundry. Multi-Vt periphery and high-current bitcell support are also available to meet extreme high performance or low leakage needs.

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