

PDF/SOLUTIONS™

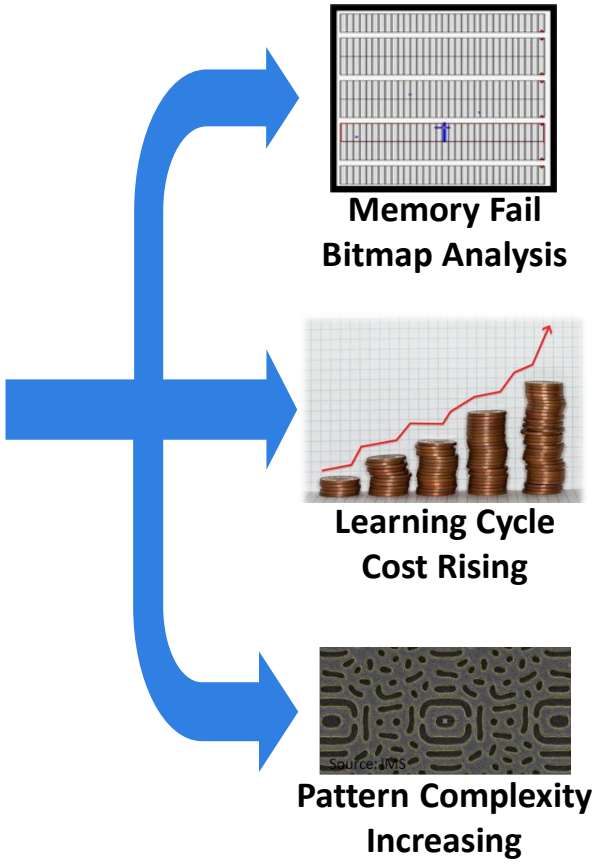
SIEMENS



Accelerating Yield Learning

ITC 2023 / OCT 2023

PDF Solutions and Siemens EDA accelerating yield



Tessent SiliconInsight + Exensio Bitmap Integration

Accelerating setup and analysis for complex embedded memory products

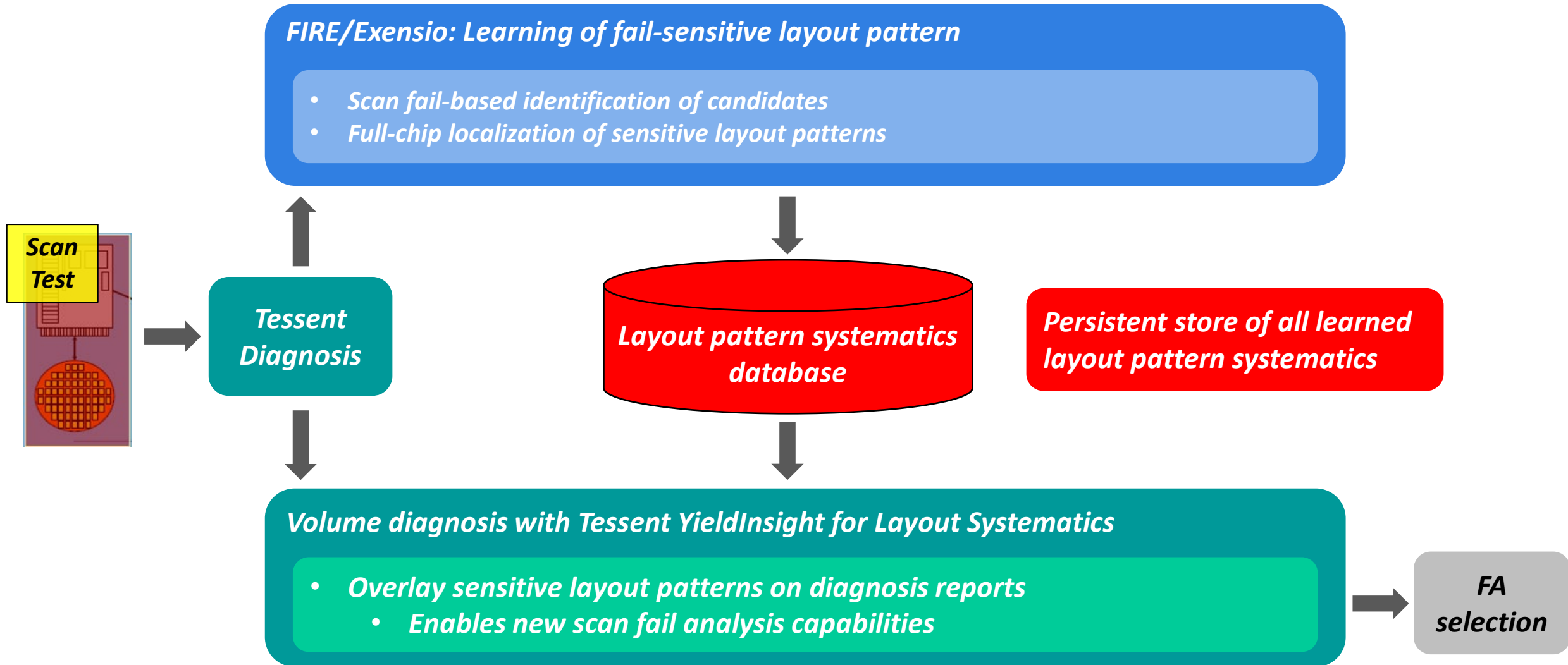
Tessent YieldInsight + Exensio Integration

Reduce time to yield by bringing together scan diagnosis data with manufacturing analytics

Tessent YieldInsight + FIRE layout pattern systematics

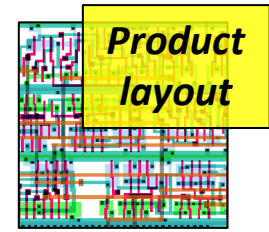
Extend volume scan diagnosis with layout pattern systematics

Tessent YieldInsight + FIRE/Exensio layout pattern systematics

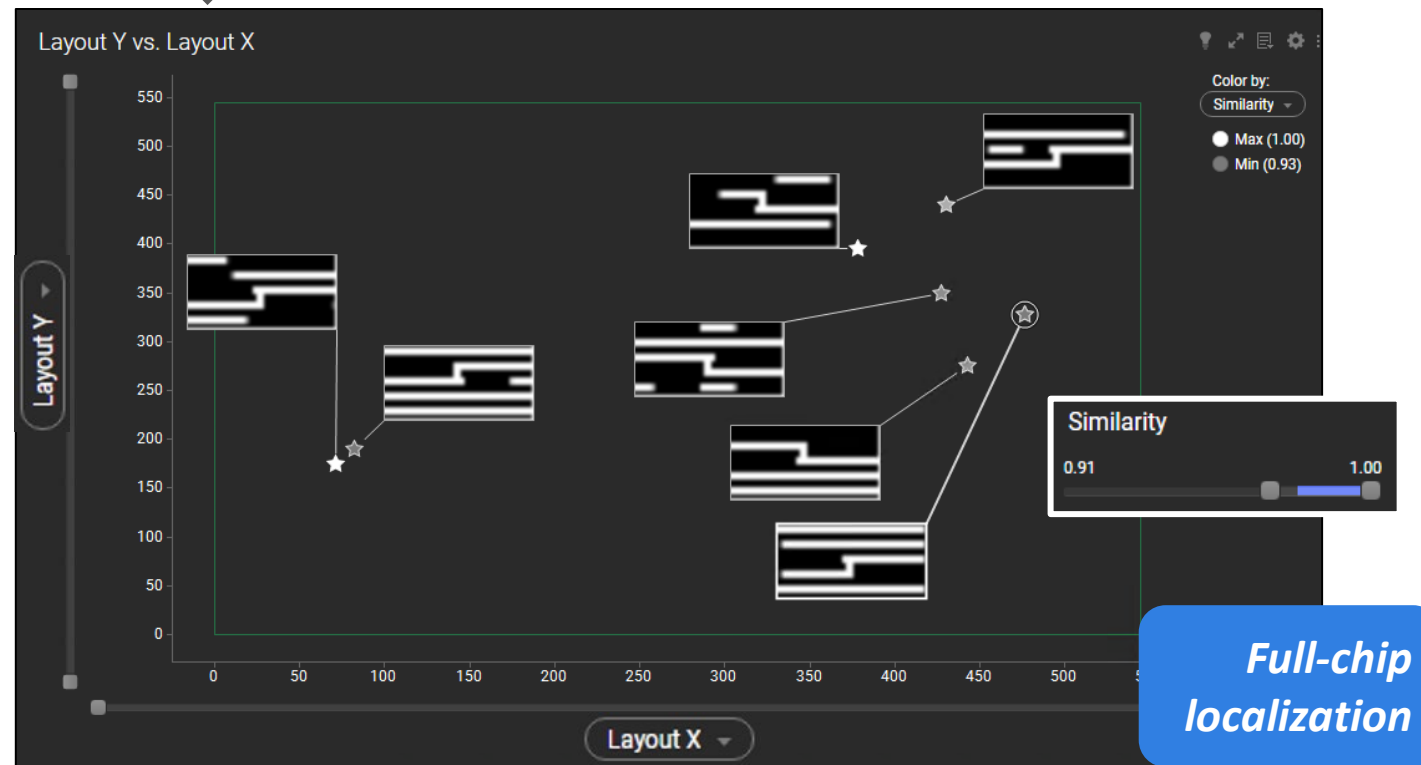
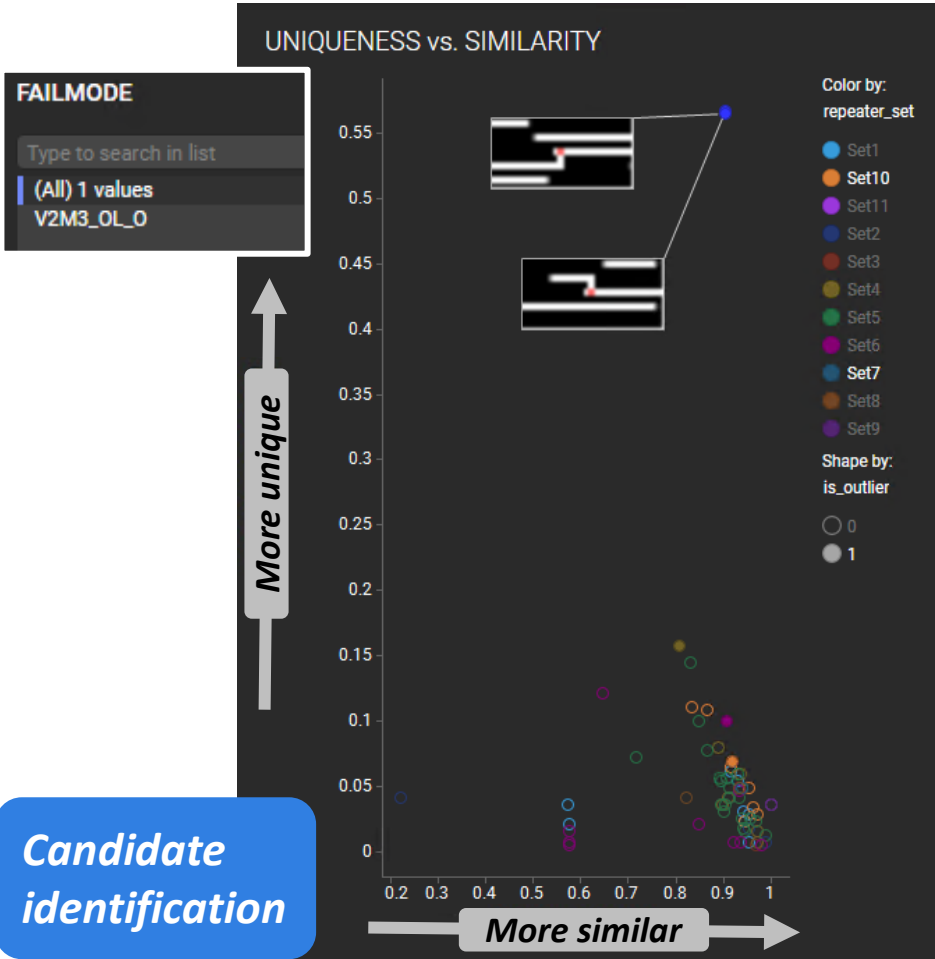


FIRE + Exensio: Layout pattern systematics learning

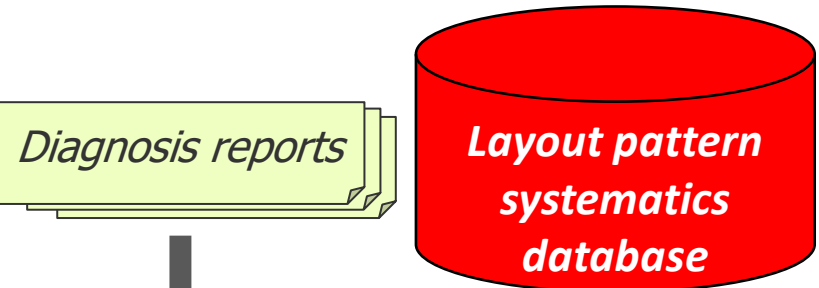
Net repeater fails



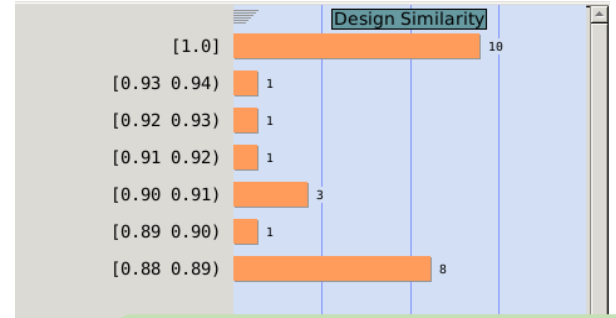
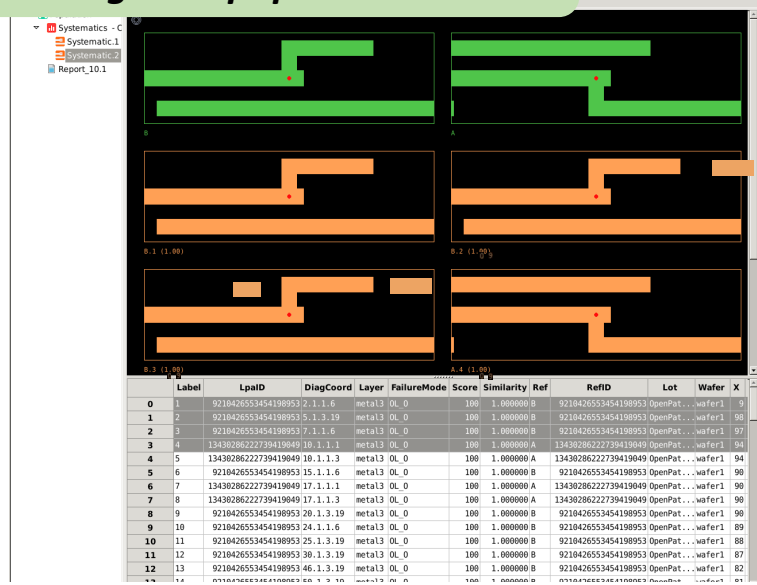
Layout pattern systematics database



Tessent YieldInsight: Volume scan diagnosis with layout pattern systematics



Analyze layout pattern similarity over diagnosis population



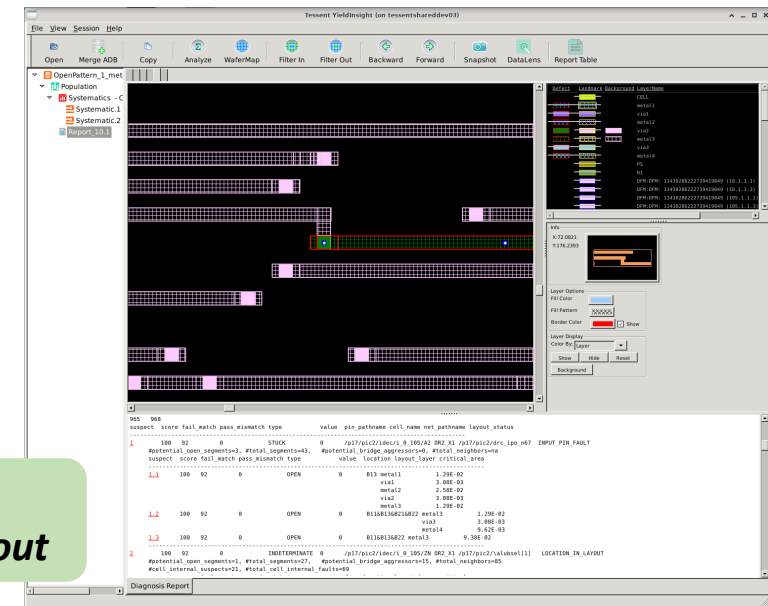
Pattern similarity histogram over diagnosis population

Annotate diagnosis population with layout pattern systematics

Identify fails with known sensitive layout patterns

FA selection

Review in context of diagnosis report and layout



Benefits of solution: FA efficiency

■ Confirming suspected systematics defect locations is

- expensive
 - Multiple PFA samples needed
 - Fault isolation (FI) + PFA costs range \$50-100k
- time consuming
 - 3-6 weeks for fault isolation / part + PFA time / sample

■ Solution provides

- isolation of PFA search area to high confidence locations → Shorter FI + PFA time
- tagging of fails with previously confirmed systematics → Reduced number of PFAs
- learning of layout pattern systematics across multiple products

Silicon demonstration results

- **Successful demonstration on silicon dataset comprising multiple lots/wafers of scan diagnosis data with foundry confirmed layout systematics**
- **Via opens in two lower metal layers identified as root cause for repeater fails**
- **88% of repeater sets attributed to the same two root causes**
 - Multiple identified locations confirmed by PFA results
- **<10 layout patterns per repeater set identified for visual inspection**
 - Demonstrated solution provides significant reduction in number of layout patterns to inspect
- **Ongoing live silicon engagements on advanced process nodes**

Summary

- Enables identification of layout pattern systematic candidates
- Silicon-validated methodology
- Improves productivity by making efficient use of FA resources
- Faster closing of the entitlement yield gap



Siemens and PDF Solutions are ready to engage with you to demonstrate the benefits of the integrated solution

Thank You

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Benefits of integrated Tessent – Exensio/FIRE solutions

Exclude
Include some in wor

Integration	Before integrated solution	Benefit of integration solution
<p><i>Tessent SiliconInsight (TSI) / MemoryBIST</i> + <i>Exensio Bitmap / Manufacturing Analytics (E-MA)</i></p>	<p>Configuration of embedded memories for bitmap analysis is time consuming</p>	<p>Efficient automated setup and comprehensive memory fail analysis using all yield and manufacturing data</p>
<p><i>Tessent YieldInsight (TYI)</i> + <i>Exensio Manufacturing Analytics (E-MA)</i></p>	<p>Use scan diagnosis data only to identify potential failure suspect for PFA</p>	<p>Use Exensio yield analysis to narrow down suspected wafer and die populations for TYI analysis ➔ Improve accuracy and efficiency</p>
<p><i>Tessent YieldInsight (TYI)</i> + <i>FIRE layout pattern systematics</i></p>	<p>Use random defectivity fail mechanisms to narrow down potential scan fail suspects</p>	<p>Add layout sensitive fail mechanisms into scan diagnostics ➔ Increased diagnosis resolution and accuracy</p>



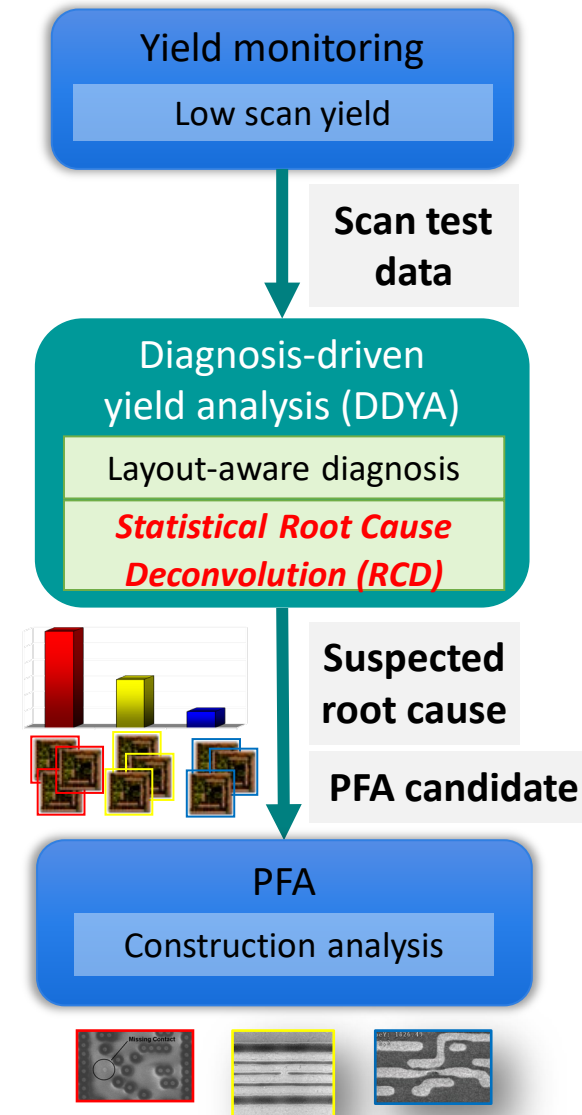
Tessent YieldInsight – Exensio integration

**Combining volume scan diagnosis data with
yield and manufacturing data**

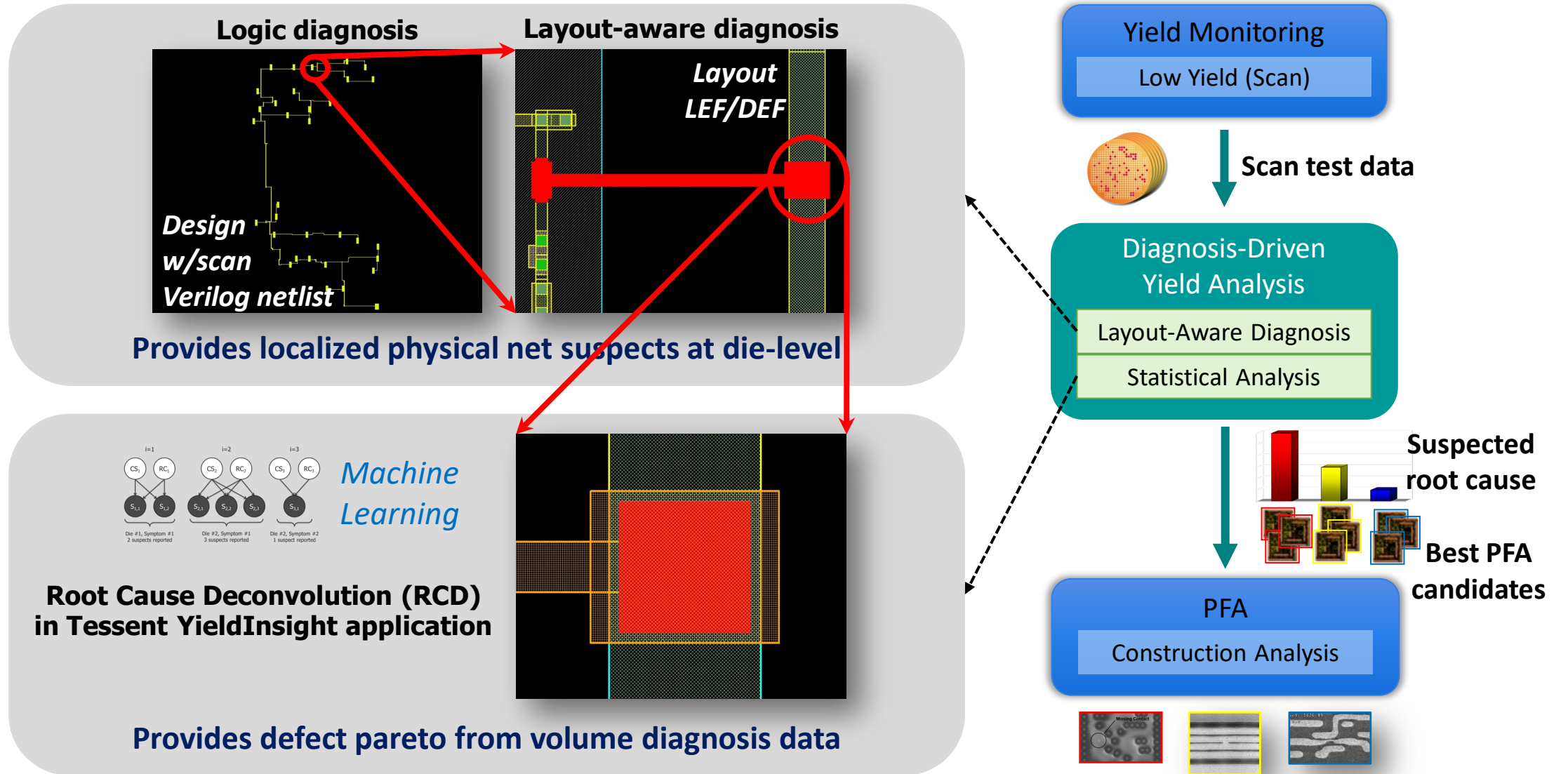
Comprehensive diagnosis-driven yield analysis

- Siemens' diagnosis-driven yield analysis (DDYA)
 - Provides root cause defect Paretos
 - Enables PFA candidate selection
- Effectiveness depends on good selection of failing dies
- DDYA methodology does not use all available product data

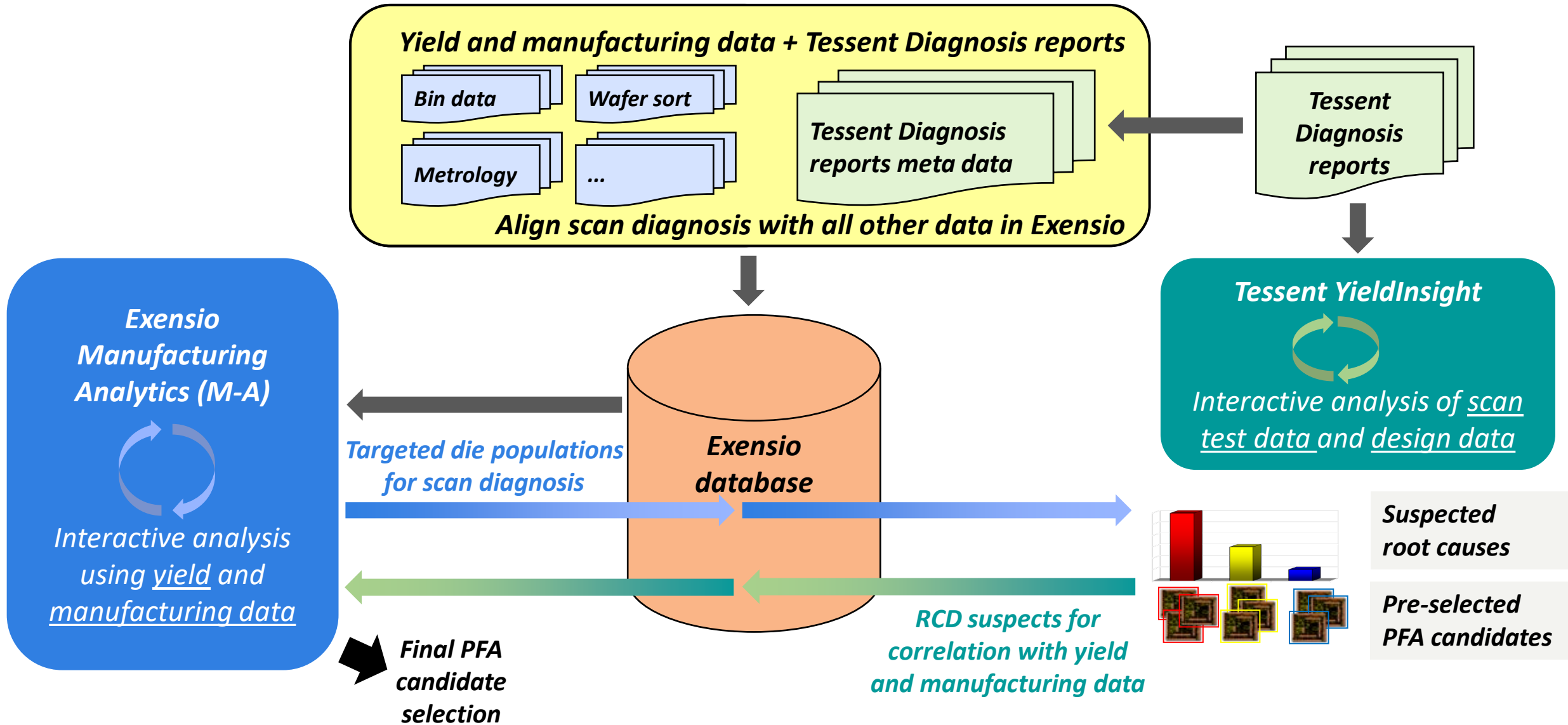
Needs efficient solution to identify best die population based on comprehensive product fail analysis
→ Integration with Exensio Manufacturing Analytics



Tessent Diagnosis-driven yield analysis (DDYA)

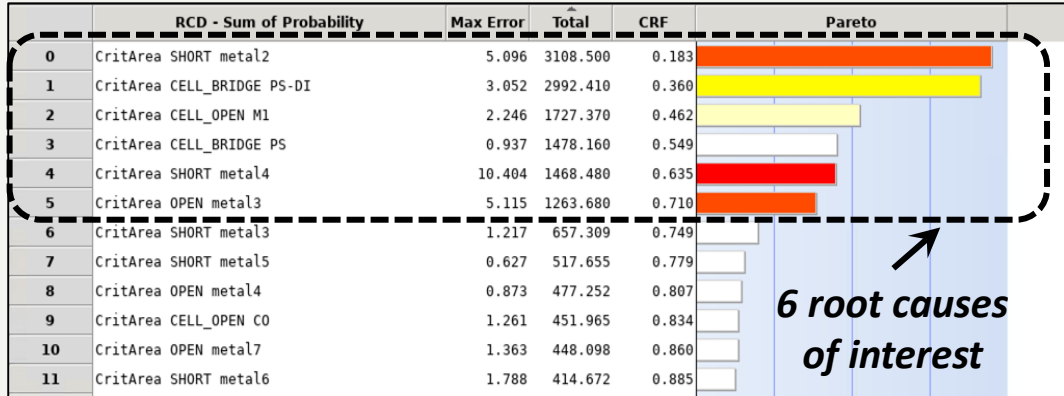


Tessent YieldInsight + Exensio integration overview

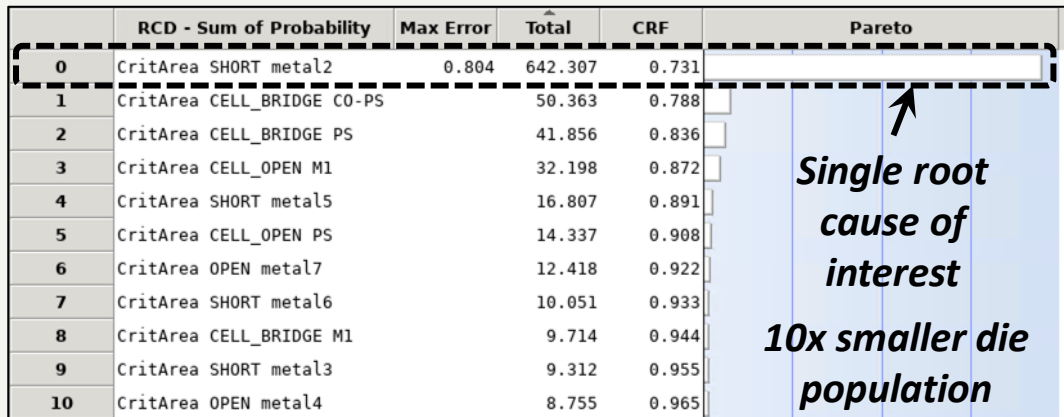


Generating targeted populations for Tessent YieldInsight

RCD Pareto with dies from all 200 wafers



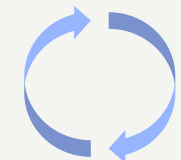
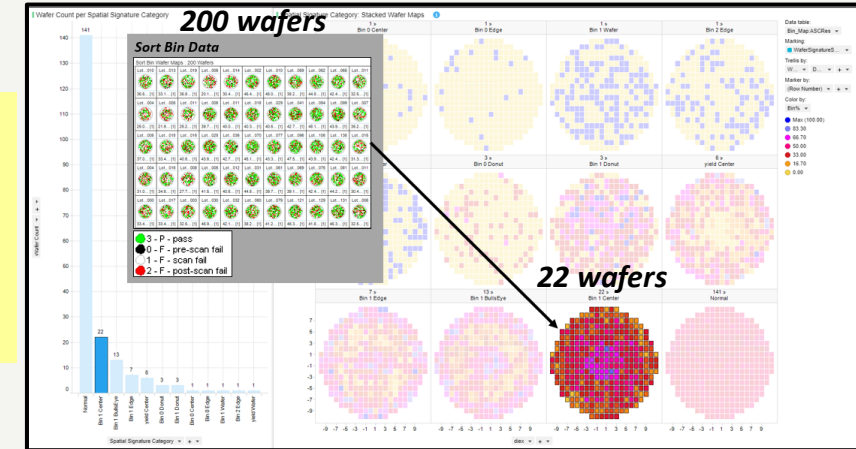
Tessent YieldInsight



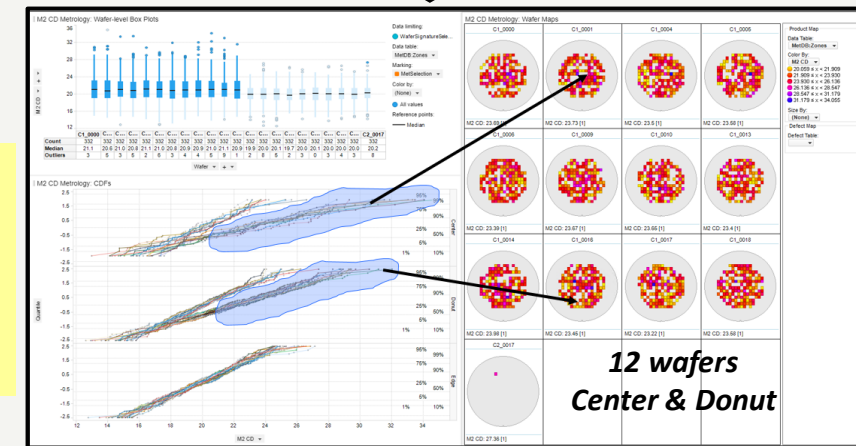
RCD Pareto with targeted die population

Exensio M-A

Targeted Wafer Population
E.g., Sort Bin Data Wafer-level SSA



Targeted Die Population
E.g., Metal CD Metrology / WAT Distribution Analysis



Die Population Transfer

Correlation of RCD suspects with yield & manufacturing data

Tessent YieldInsight

RCD Pareto : Dies from target population only

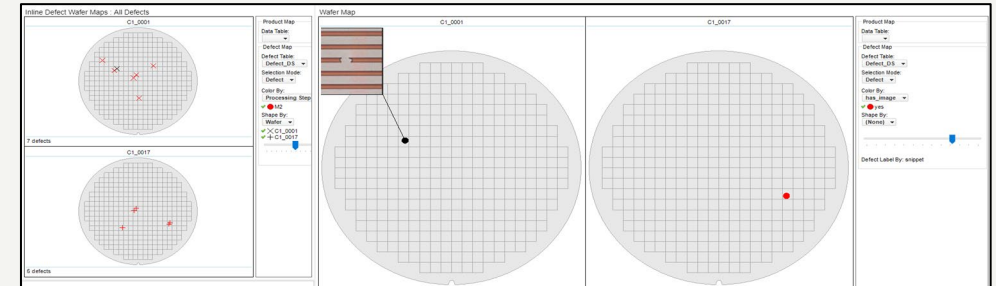
	RCD - Sum of Probability	Max Error	Total	CRF	Pareto
0	CritArea SHORT metal2	0.804	642.307	0.731	
1	CritArea CELL_BRIDGE CO-PS		50.363	0.788	
2	CritArea CELL_BRIDGE PS		41.856	0.836	
3	CritArea CELL_OPEN M1		32.198	0.872	
4	CritArea SHORT metal5		16.807	0.891	
5	CritArea CELL_OPEN PS		14.337	0.908	
6	CritArea OPEN metal7		12.418	0.922	
7	CritArea SHORT metal6		10.051	0.933	

	Wafer	X	Y	SymID	SusID	Score	SymCNT	SusCNT	SymSusCNT	TotalProb	CritArea SHORT metal2	CritArea CELL_BRIDGE CO-PS
0	Lot_0009:C1_0017	7	-3	11.1	100	100	1	1	1	1.000	1.000	0.000
1	Lot_0009:C1_0017	-3	4	11.1	100	100	1	1	1	1.000	1.000	0.000
2	Lot_0019:C1_0001	3	1	11.1	100	100	1	1	1	1.000	1.000	0.000
10	Lot_0019:C1_0001	5	0	11.1	100	100	1	4	4	1.000	1.000	0.000
11	Lot_0019:C1_0001	3	-5	11.1	100	100	1	4	4	1.000	1.000	0.000
15	Lot_0019:C1_0001	2	-7	11.1	100	100	1	17	17	1.000	1.000	0.000
18	Lot_0009:C1_0017	-3	2	11.1	100	100	1	7	7	1.000	1.000	0.000
38	Lot_0019:C1_0001	-2	6	11.1	100	100	1	1	1	1.000	1.000	0.000
44	Lot_0019:C1_0001	-3	-7	11.1	100	100	1	14	14	1.000	1.000	0.000
47	Lot_0009:C1_0017	0	-2	11.1	100	100	1	1	1	1.000	1.000	0.000
50	Lot_0019:C1_0001	3	3	11.1	100	100	1	1	1	1.000	1.000	0.000
56	Lot_0019:C1_0001	-1	-5	11.1	100	100	1	3	3	1.000	1.000	0.000

RCD suspects with high M2 short root cause

Exensio M-A

Correlation of RCD suspects with Yield & Mfg Data



Correlation of RCD suspects with yield & manufacturing data to increase the PFA success rate



Gallery review of RCD suspect layout snippets



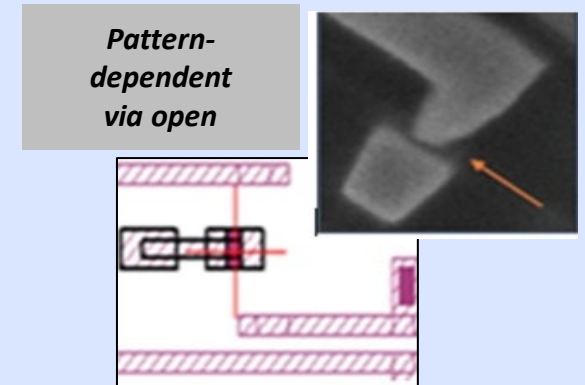
Tessent Diagnosis/YieldInsight + FIRE integration

Extending Tessent YieldInsight with FIRE layout pattern systematics

Volume scan diagnosis with layout pattern systematics

- Volume scan diagnosis with analysis in Tessent YieldInsight proven for learning of random defect sources
- In advanced technologies layout pattern systematics contribute significant yield loss well into volume production

Layout pattern systematic defects



Prevent entitlement yield for high volume production

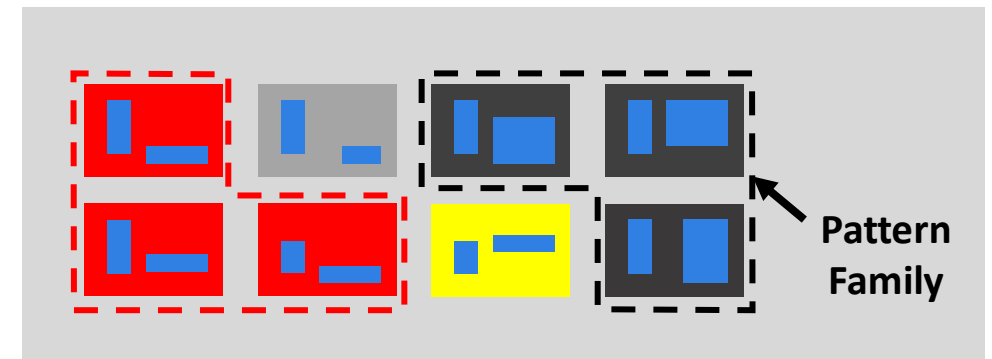
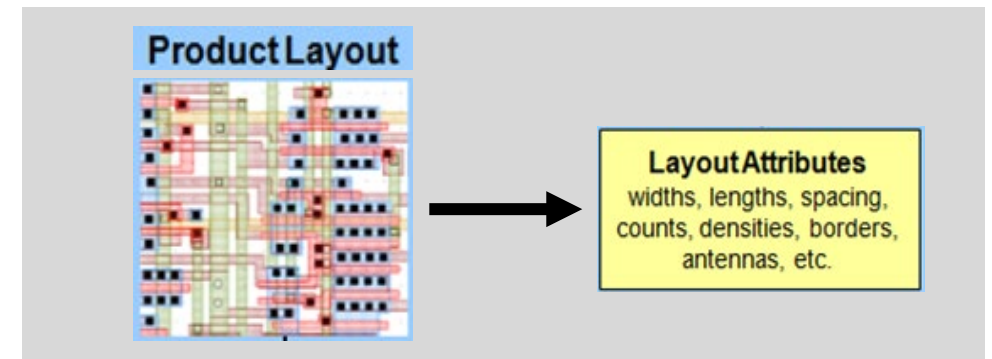
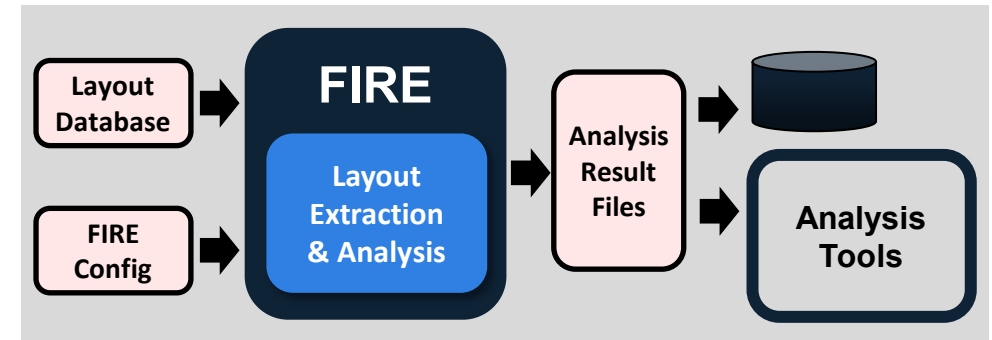
**Scan diagnosis-based yield learning needs to factor in layout patterns systematics
→ Combine Tessent Diagnosis / YieldInsight with layout pattern systematics using FIRE**

FIRE advanced layout analysis technology

High-performance
Full-chip
Electrical connectivity-aware

Extraction of layout attributes
Fully-customizable

Automated pattern classification
Grouping of similar patterns into pattern families



Net repeater-based layout pattern systematics learning

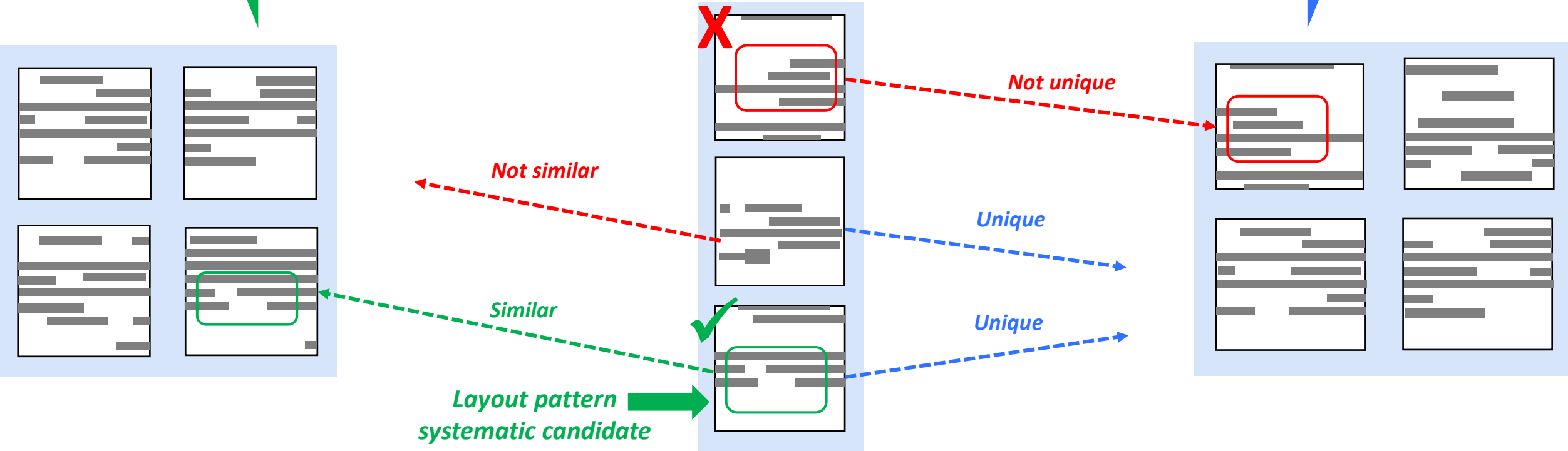
Patterns in other repeater sets

Similarity: A similar pattern occurs in other repeater sets

Repeater set of interest (~100 patterns)

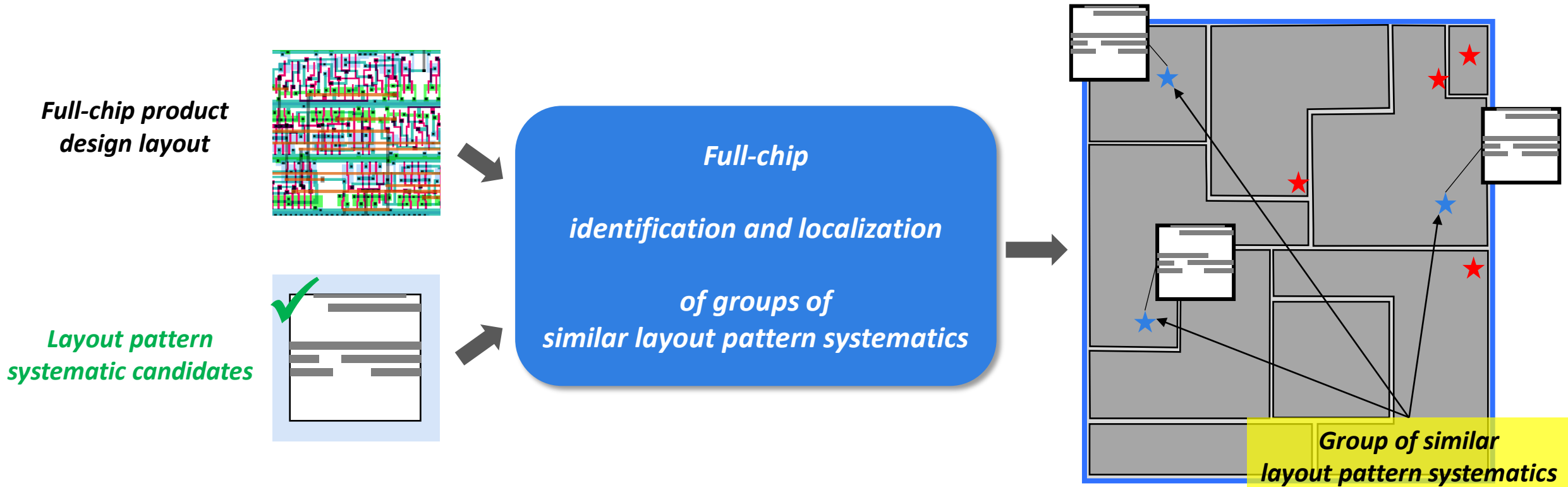
Uniqueness: Similar pattern rarely occurs outside repeater sets

Full chip (millions of patterns)

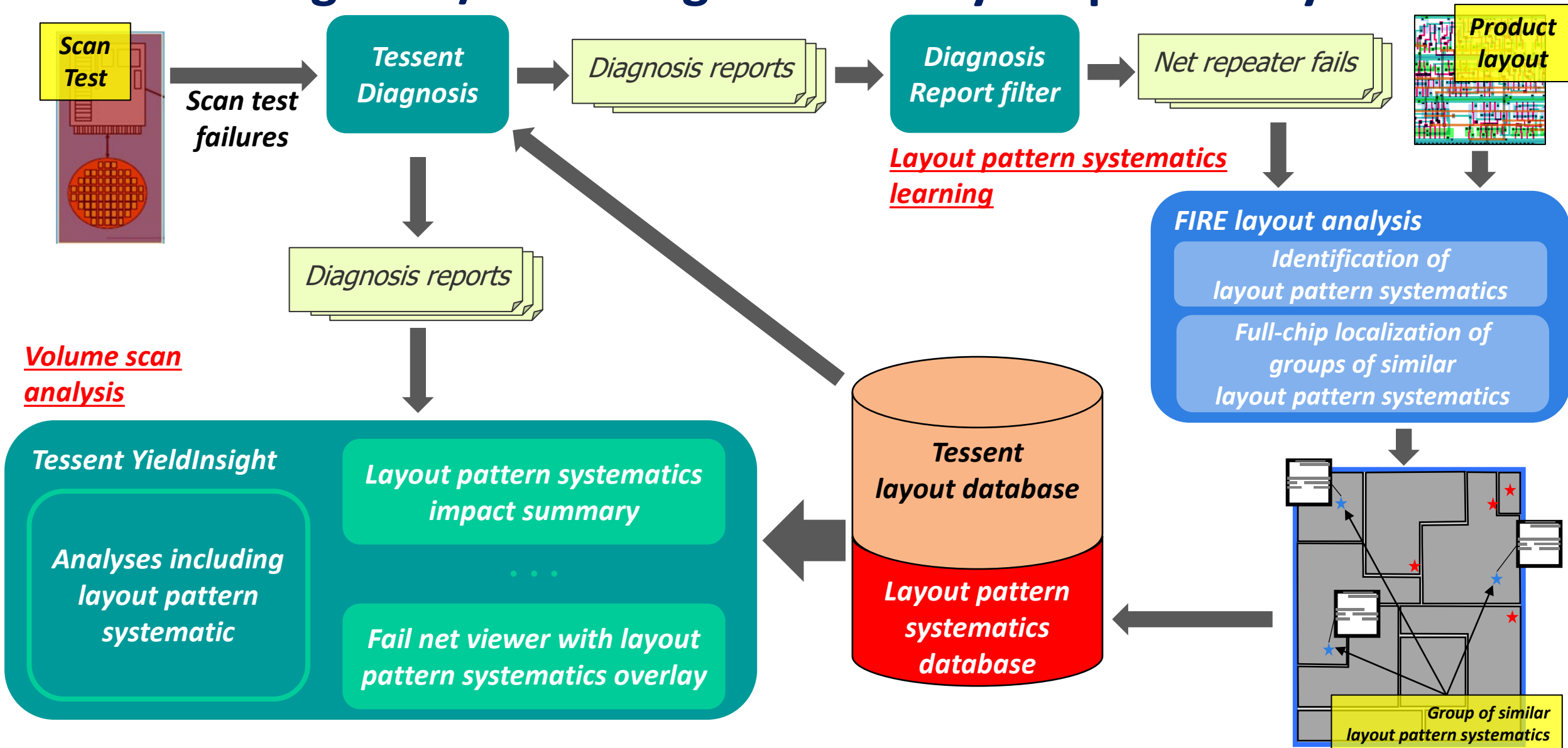


Net repeater fails - same net fails on multiple dies - are high-confidence indicators of an underlying systematic fail root cause

Full-chip extraction of layout pattern systematics



Tessent Diagnosis/YieldInsight + FIRE layout pattern systematics





Tessent SiliconInsight - Exensio integration

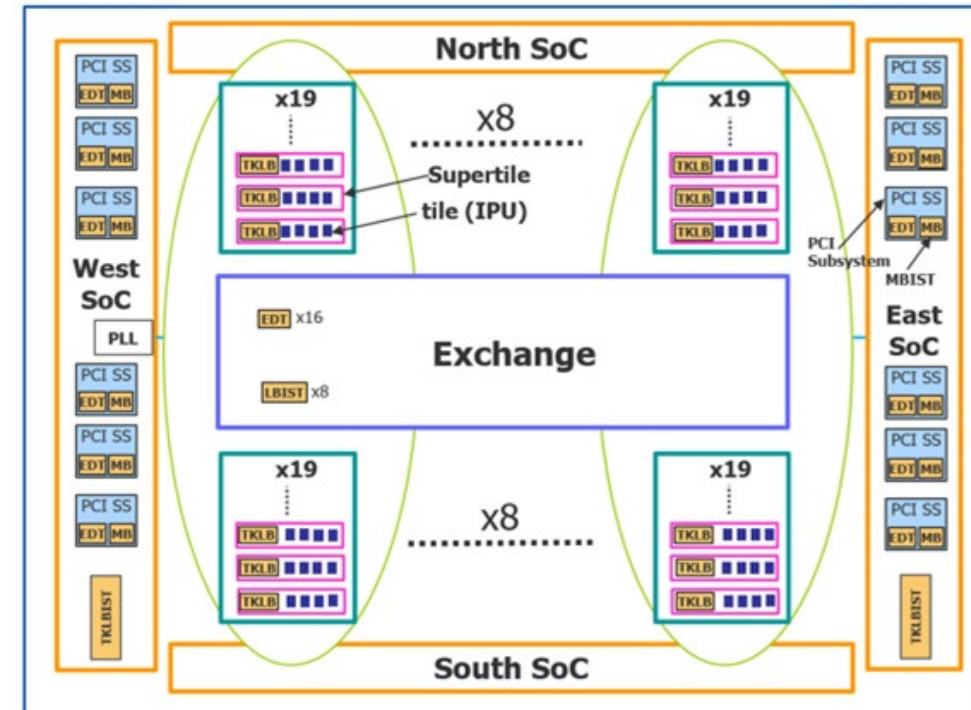
**Addressing the analysis needs of
complex embedded memory products**

Memory trends and yield learning challenges

- Complexity of embedded memory products increases
 - >10K memories
 - 100s of MBIST controllers
- Failure root cause analysis and setup of such complex embedded memory chips is a time-consuming task

Needs an efficient automated setup and analysis solution

Example of complex AI chip: Graphcore



- 1216 IPUs (Intelligence Processing Units) + local memory = 'Tiles'
- Total 10.000 memories = 300MB

Integrating Tessent SiliconInsight and Exensio M-A

Tessent SiliconInsight MemoryBIST technology

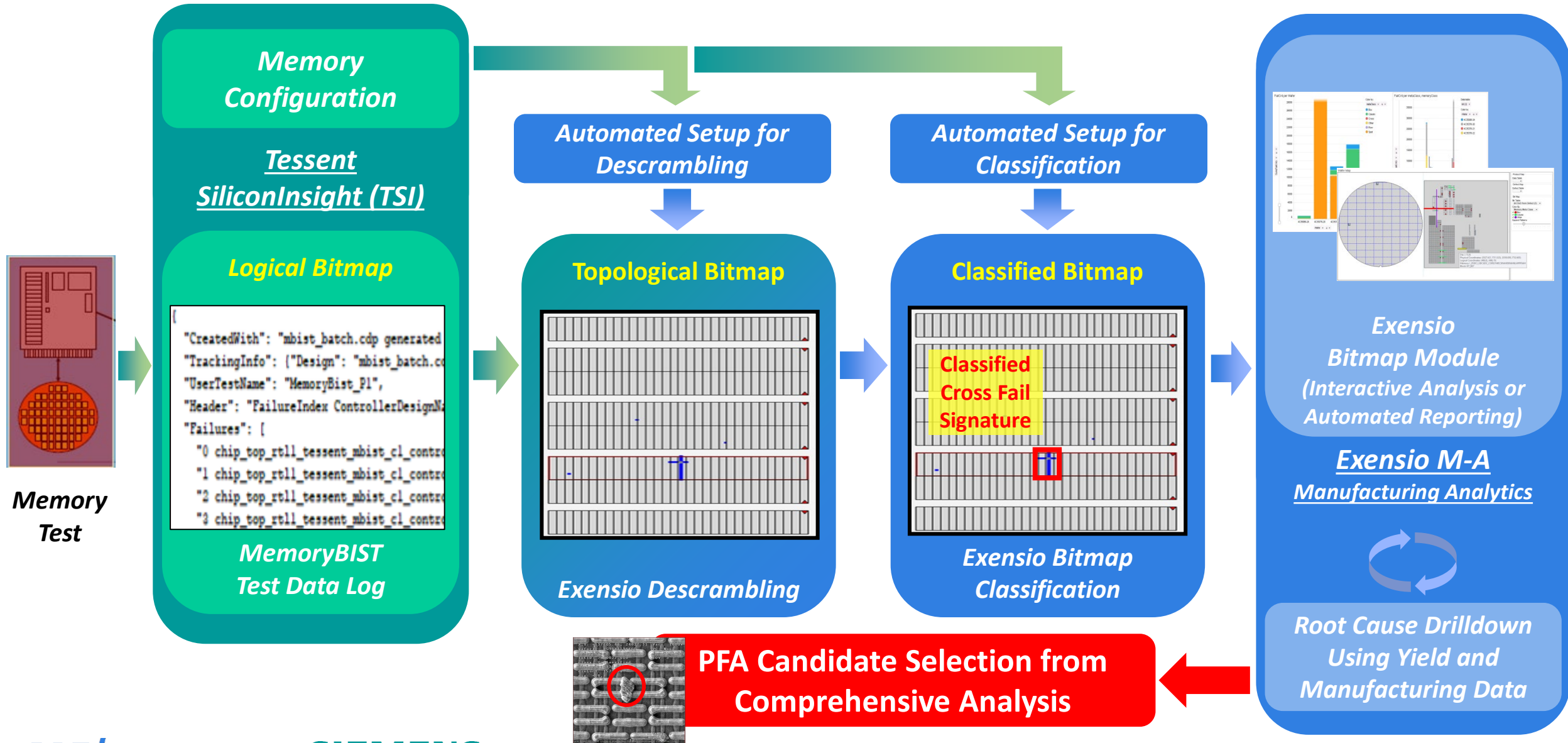
- Proven technology to collect fail information from complex embedded memory products
- Analysis of raw memory test data does not allow for volume data analysis

Exensio Manufacturing Analytics Exensio Bitmap

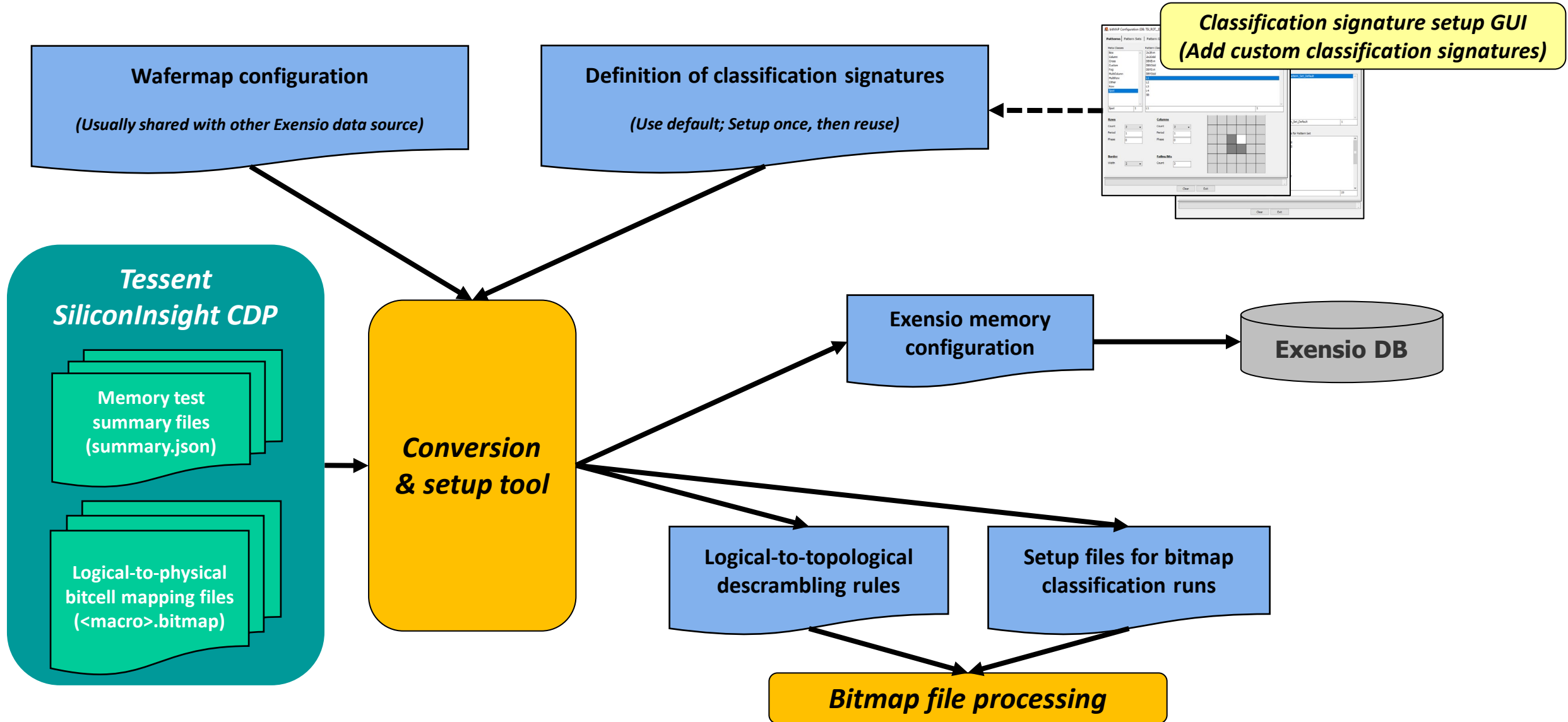
- Efficient processing of raw MemoryBIST data
- Extensive tool set for comprehensive memory fail analysis

***Tessent SiliconInsight / MemoryBIST + Exensio Manufacturing Analytics
= Single memory analysis platform***

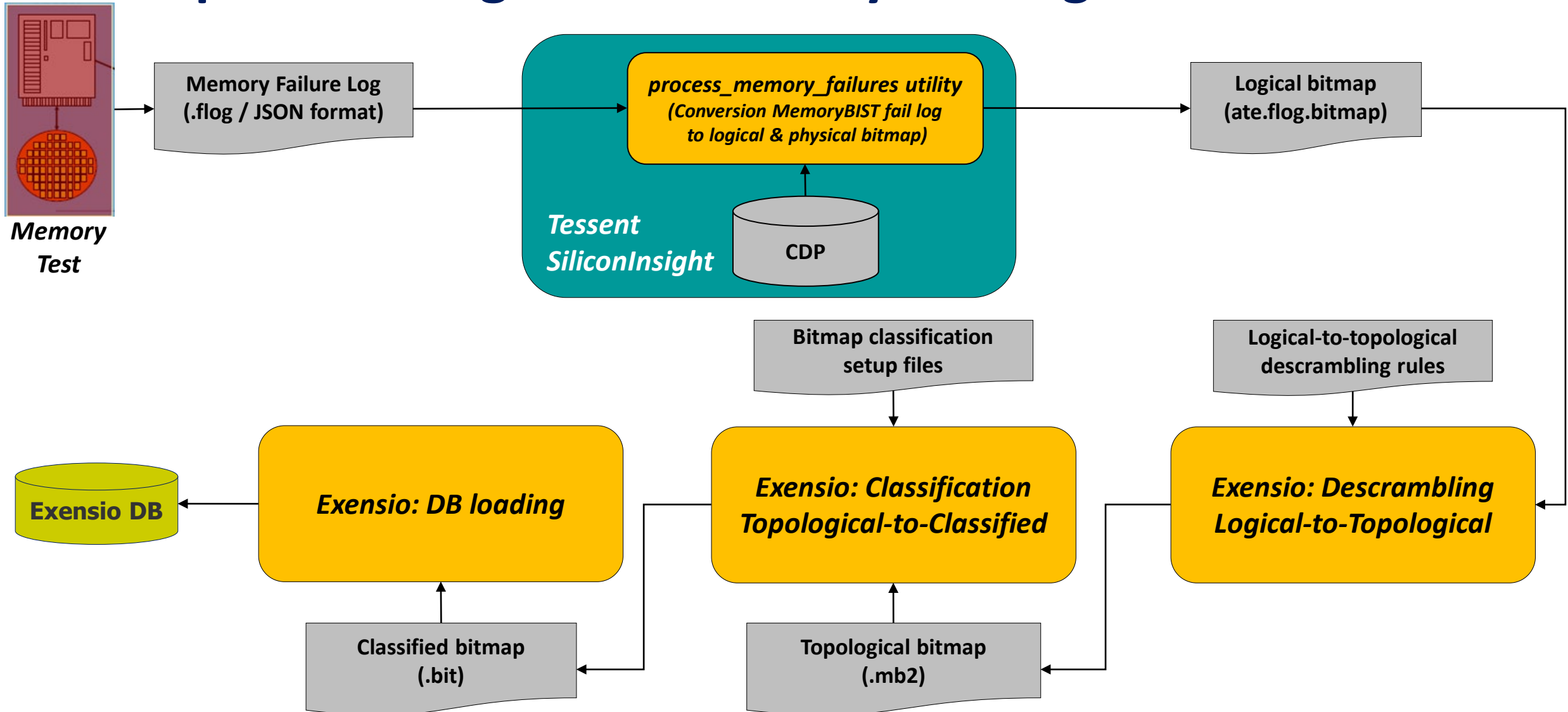
Tessent SiliconInsight + Exensio memory analysis platform



Setup of memory product

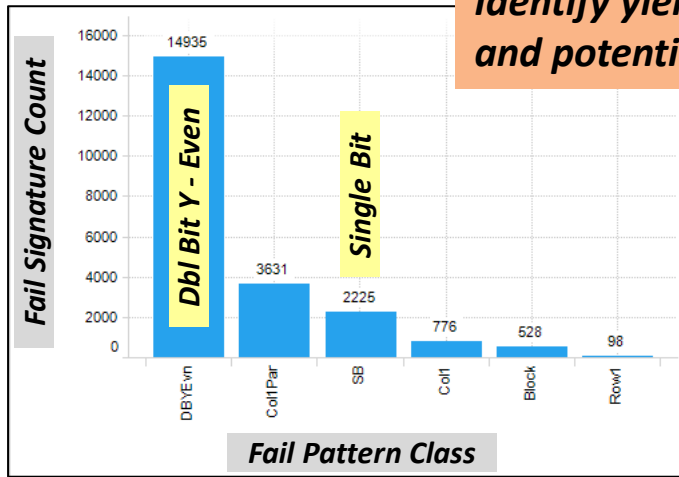


Bitmap Processing Flow: Memory Fail Log → Exensio DB



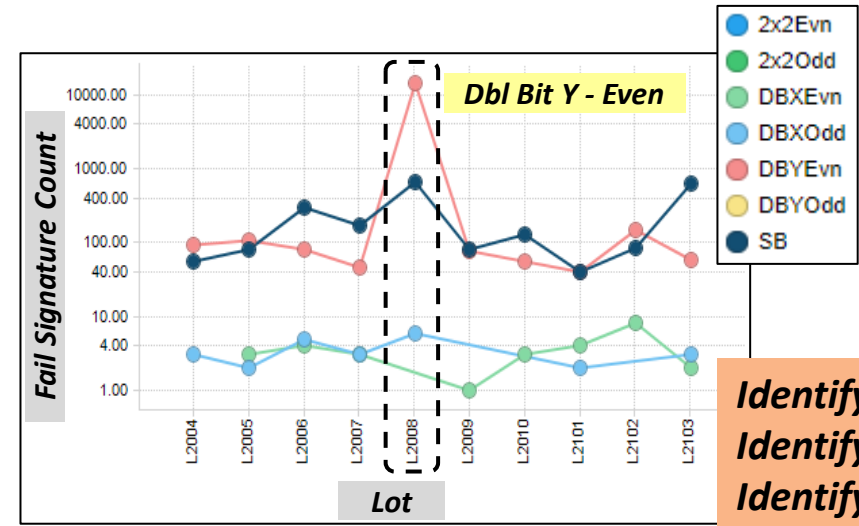
Exensio bitmap analysis capabilities

Fail Signature Paretos



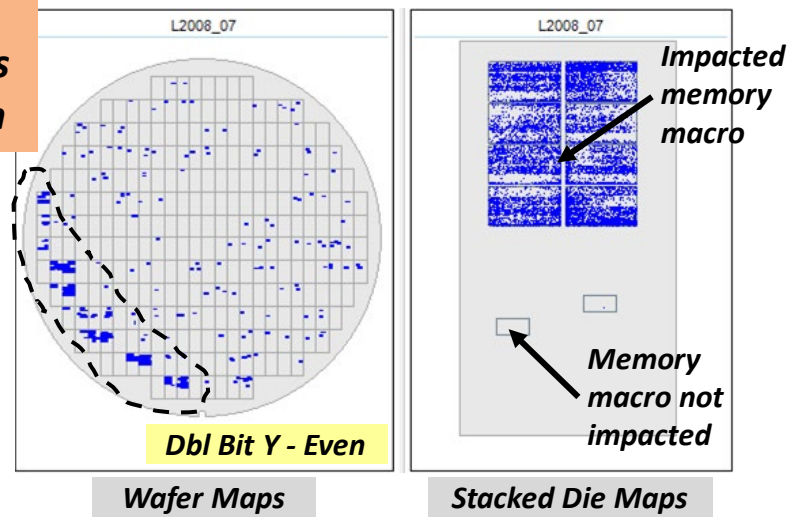
Identify yield-relevant fail signatures and potential failure root causes

Trending



Identify variabilities
Identify excursions
Identify subtle trends

Identify process and memory macro issues with spatial variation

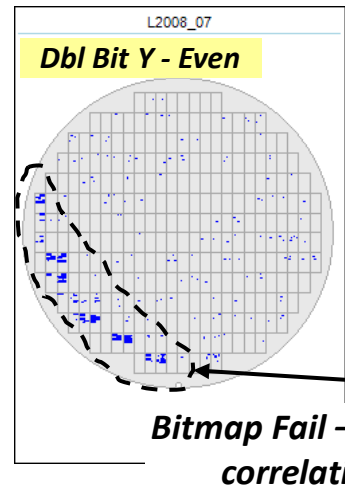


Stacked Maps

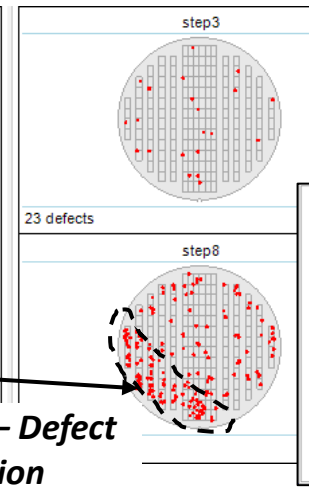
Wafer Maps

Stacked Die Maps

Bitmap Fails



Inline Defects



Correlate with other yield & mfg data to narrow down root causes diagnosis

Bitmap Fail - Defect correlation

Bitmap - Defect overlay hits for PFA submission

Multi-Data Correlations