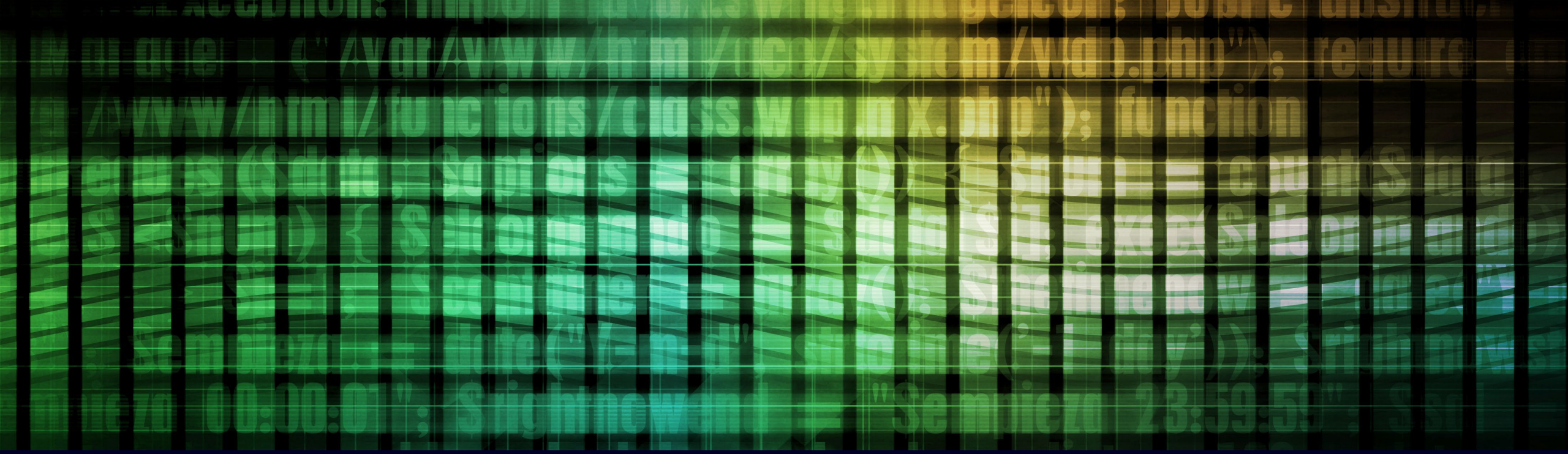

Streaming Scan Network – Fast IO high-level summary

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Disclaimer / Legend

- The information being shown in this presentation is covered under our End User License Agreement (EULA) and is confidential
- The slides contain the following visual legend

General Release

Controlled Release (production ready for select customers only)

Beta Pre-Release

Future beta

Roadmap item

- The material is for discussion & all timelines are subject to change
  - "Beta" may not be available to all customers, may not be released
  - "Future Beta" items may not turn into "Beta" or a "General Release"
  - "Roadmap" items may not be developed at all

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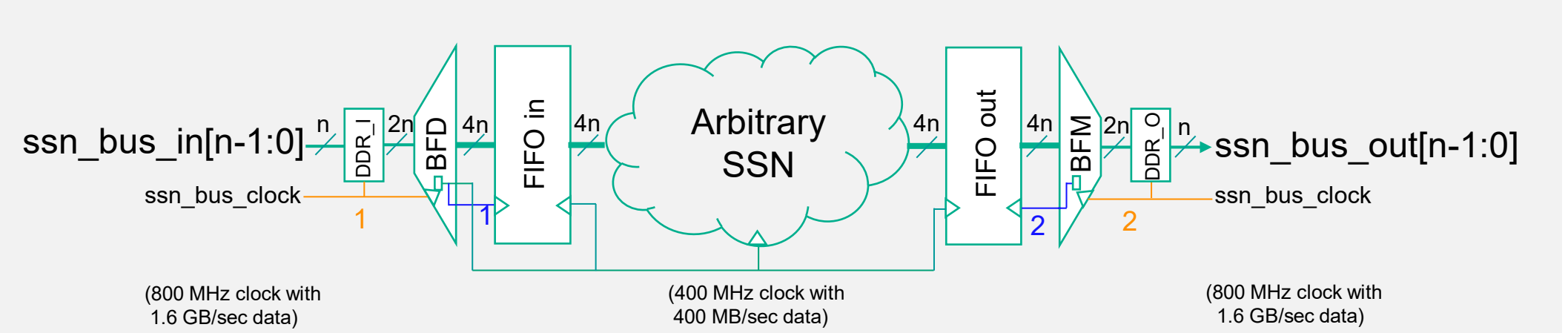
SSN Fast IO at a glance

B
Beta Pre-Release

- SSN with a faster external interface with a slower internal bus
  - Support SDR / DDR external interfaces
- Internal SSN clock created form BFD / BFM
  - Modified existing BFD / BFM
- Faster IO frequencies on ATE may require adaptive timing on input and output of SSN

Example configuration of SSN Fast IO with DDR clocking



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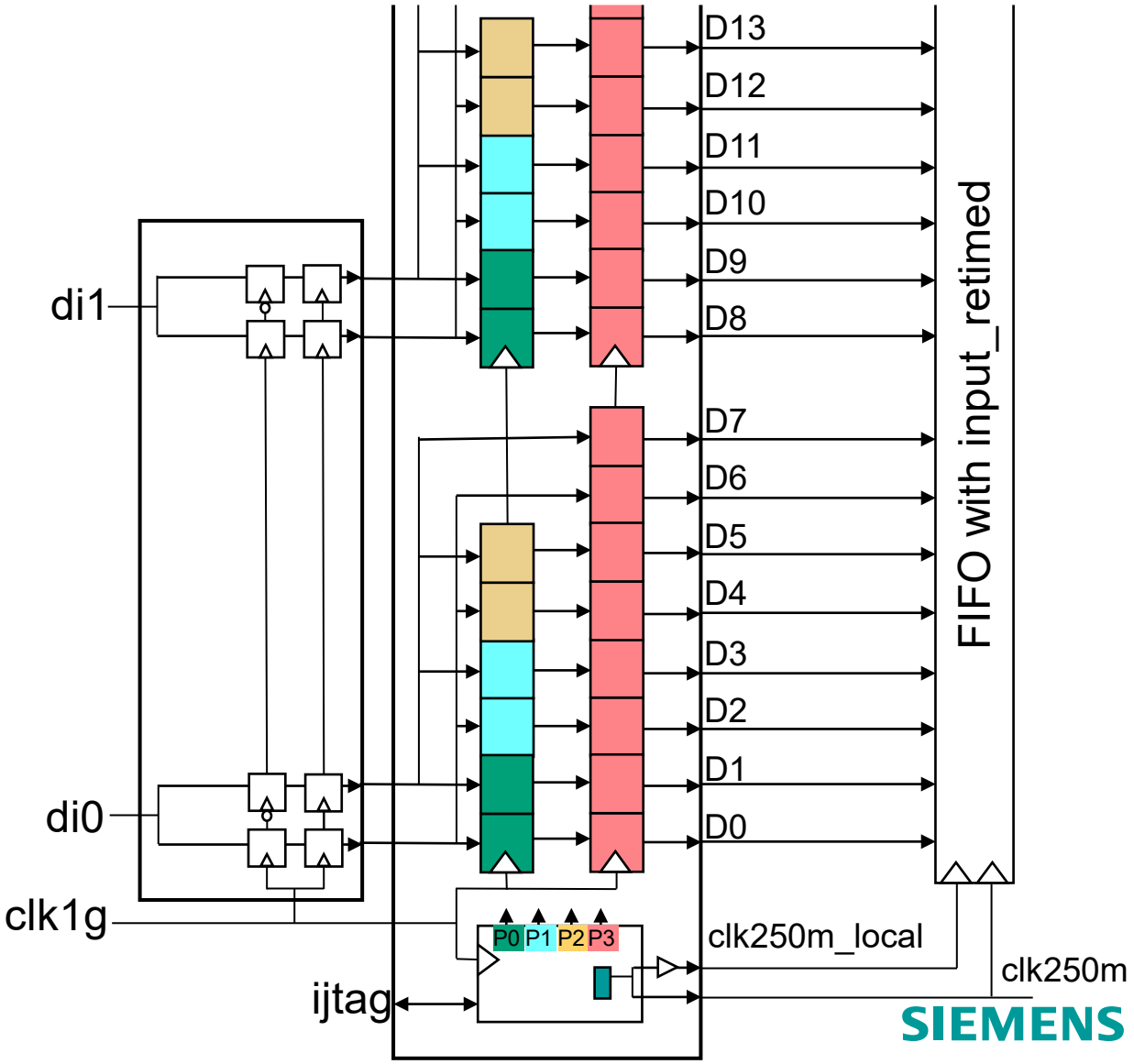
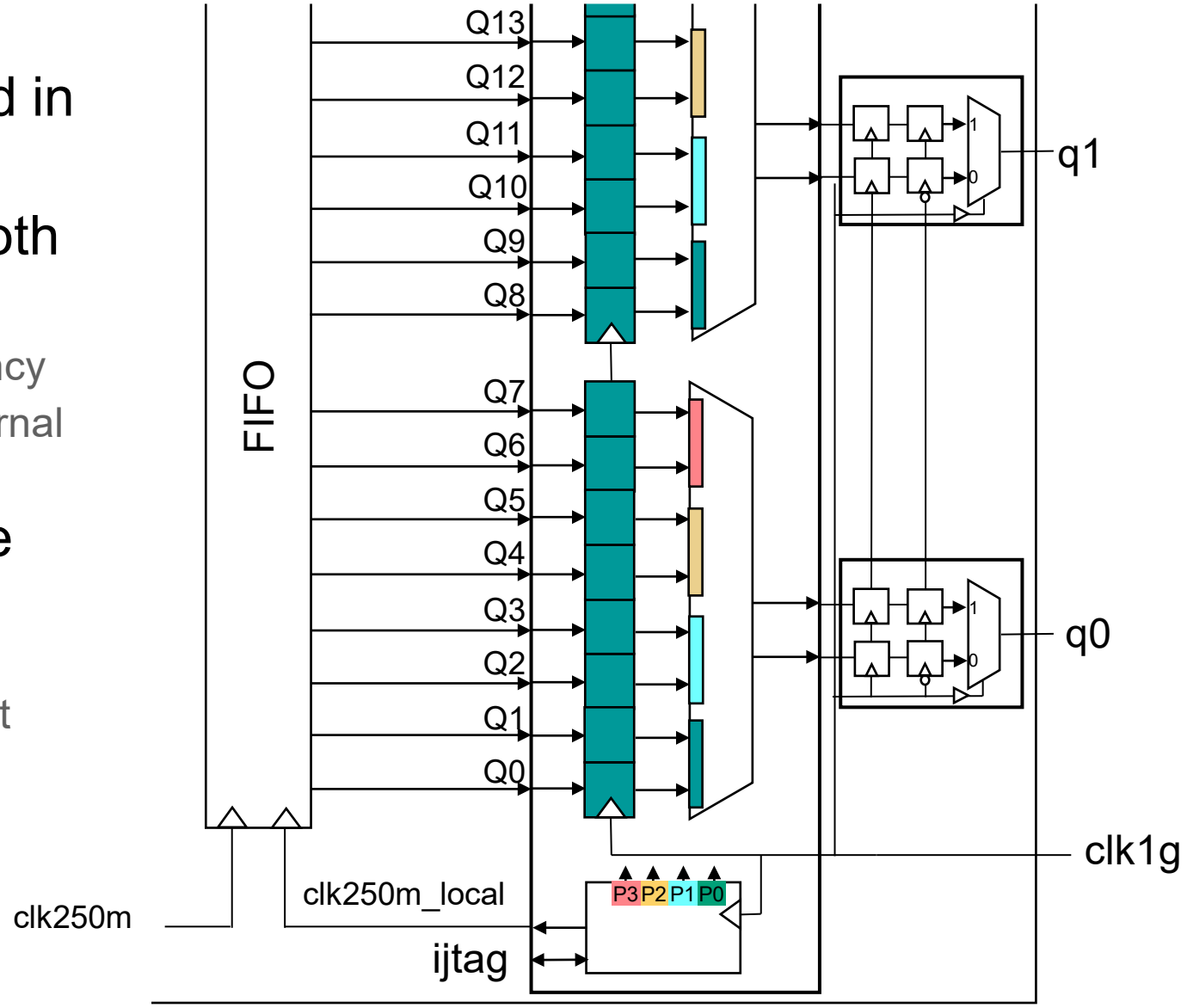
SSN Fast IO with DDR clocking (Input side)

- Same concept as SDR clocking
- Input DDR stage natively modeled in ICL like all other SSN nodes
- Initial DDR stage samples data on both edges
  - Doubling the data rate for same clock frequency
  - For same external bus width, can drive 2X internal bus at same frequency
- Clock has one edge per tester cycle
  - Special 2 cycle shift macro in STIL
  - May affect translation tool



SSN Fast IO with DDR clocking (Output side)

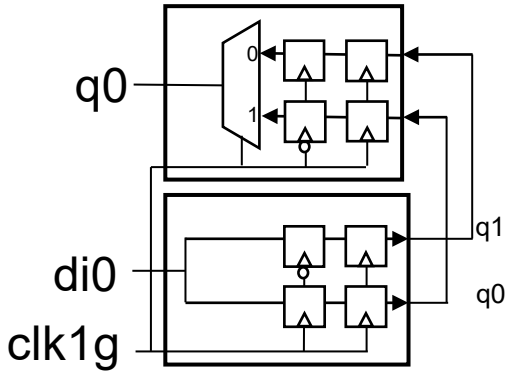
- Same concept as SDR clocking
- Output DDR stage natively modeled in ICL like all other SSN nodes
- Final DDR stage outputs data on both edges
  - Doubling the data rate for same clock frequency
  - For same external bus width, can use 2X internal bus at same frequency
- Clock has one edge per tester cycle
  - Special 2 cycle shift macro in STIL
  - May affect translation tool
  - Shared with input clock when input and output stage in the same physical block

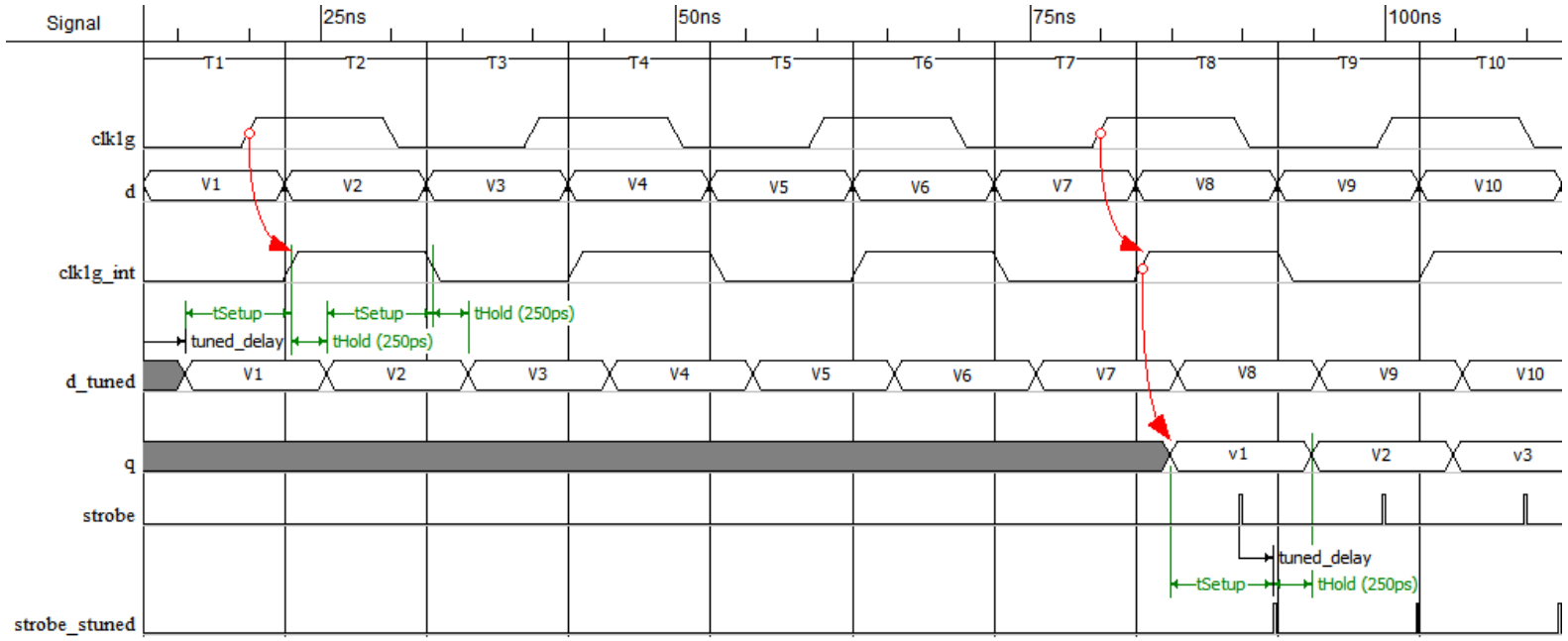


Input tuning performed at reduced rate where end of period output strobing is reliable

Using the SSN continuity pattern set periodx4 and set strobe at periodx4-1ps:
Find location where input delay stops working. Set input delay to (current delay – 750ps)

Restore period and strobe:
Find location where strobe delay stops working. Set strobe delay to (current delay – 250ps)

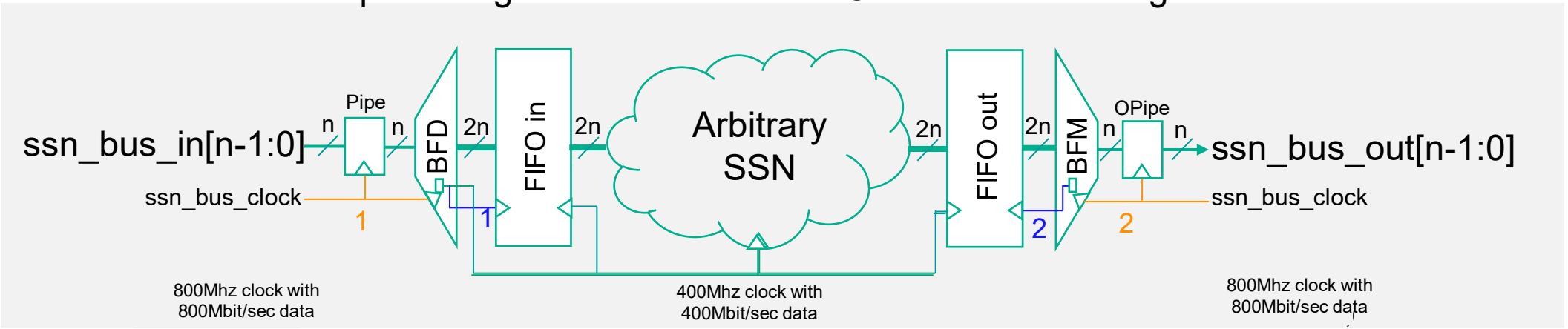




Current status

- Pattern translation companies and ATE partners support DDR patterns
  - Refresh of IEEE 1450 STIL standard for DDR
- First silicon with SSN Fast IO with DDR clocking show test time reduction
- Many high-profile customers adopting SSN with Fast IO with DDR clocking

Example configuration of SSN Fast IO with SDR clocking



SSN Fast IO advantages

- Reduces test time by improving SSN throughput
  - Faster external interface to SSN
  - Support SDR / DDR clocking

External		Data rate	Supported by Advantest / Taradyne
Interface Type	Frequency*		
SDR	up to 800MHz	800Mbs	✓
DDR	800MHz	1.6Gbs	✓
DDR	1.5GHz	3Gbs	✓
DDR	2.5GHz	5Gbs	✓
	*Maximum frequency		

- Test more parts in parallel (multi-site testing)
  - Require fewer number of pads per part

  E.g., 16 pads at 400MHz vs 32 pads at 200MHz

- Simple DDR interface can exploit ATE data rate without the complexity of using functional protocols
  - Maximum logic tested by structural tests

- Customers using GPIO with DDR clocking to improve throughput

Thank you

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