

DFT Clock Generation Methods for Packetized Scan Data Designs

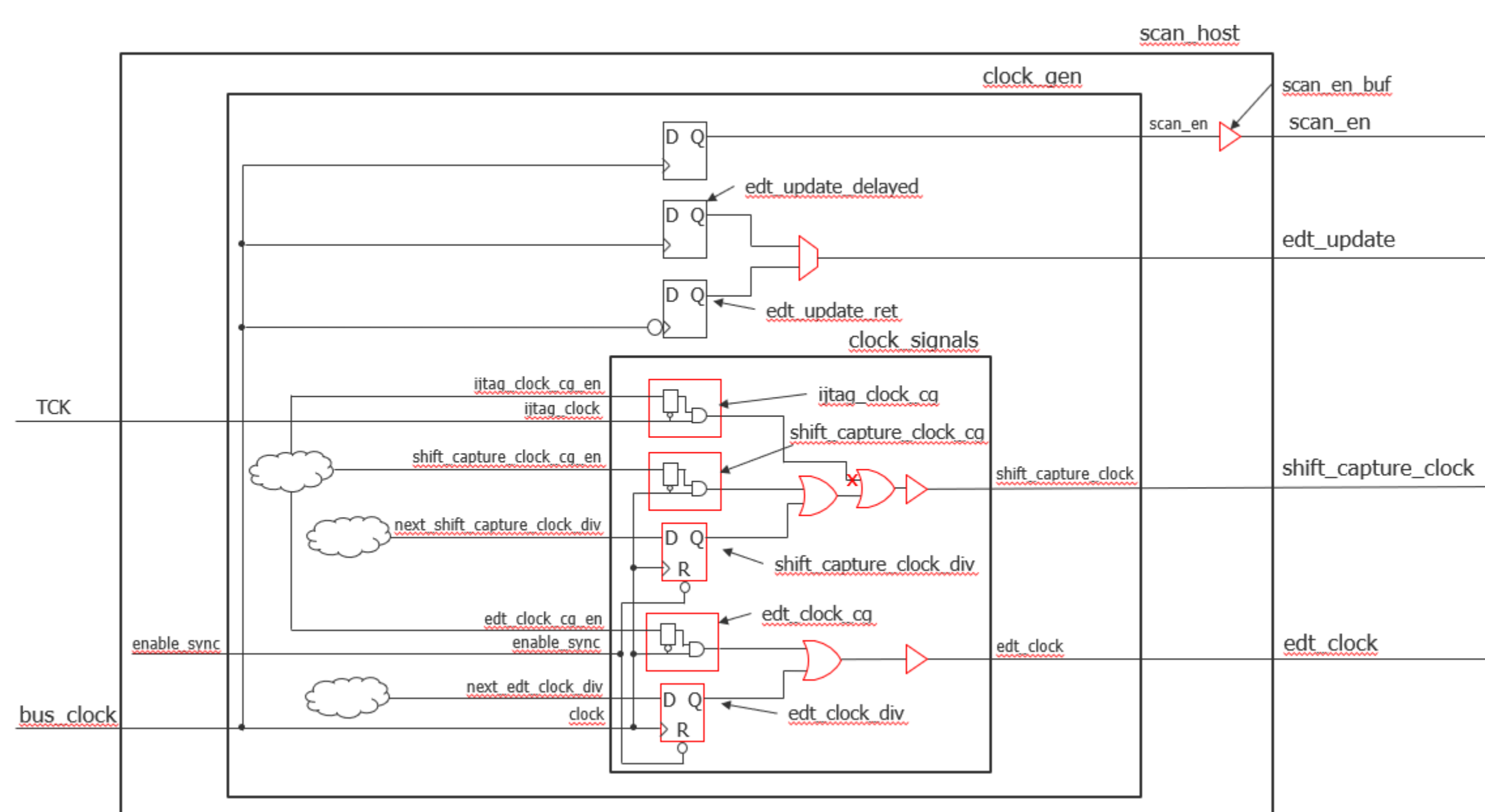
Jagjot Kaur and Ron Press

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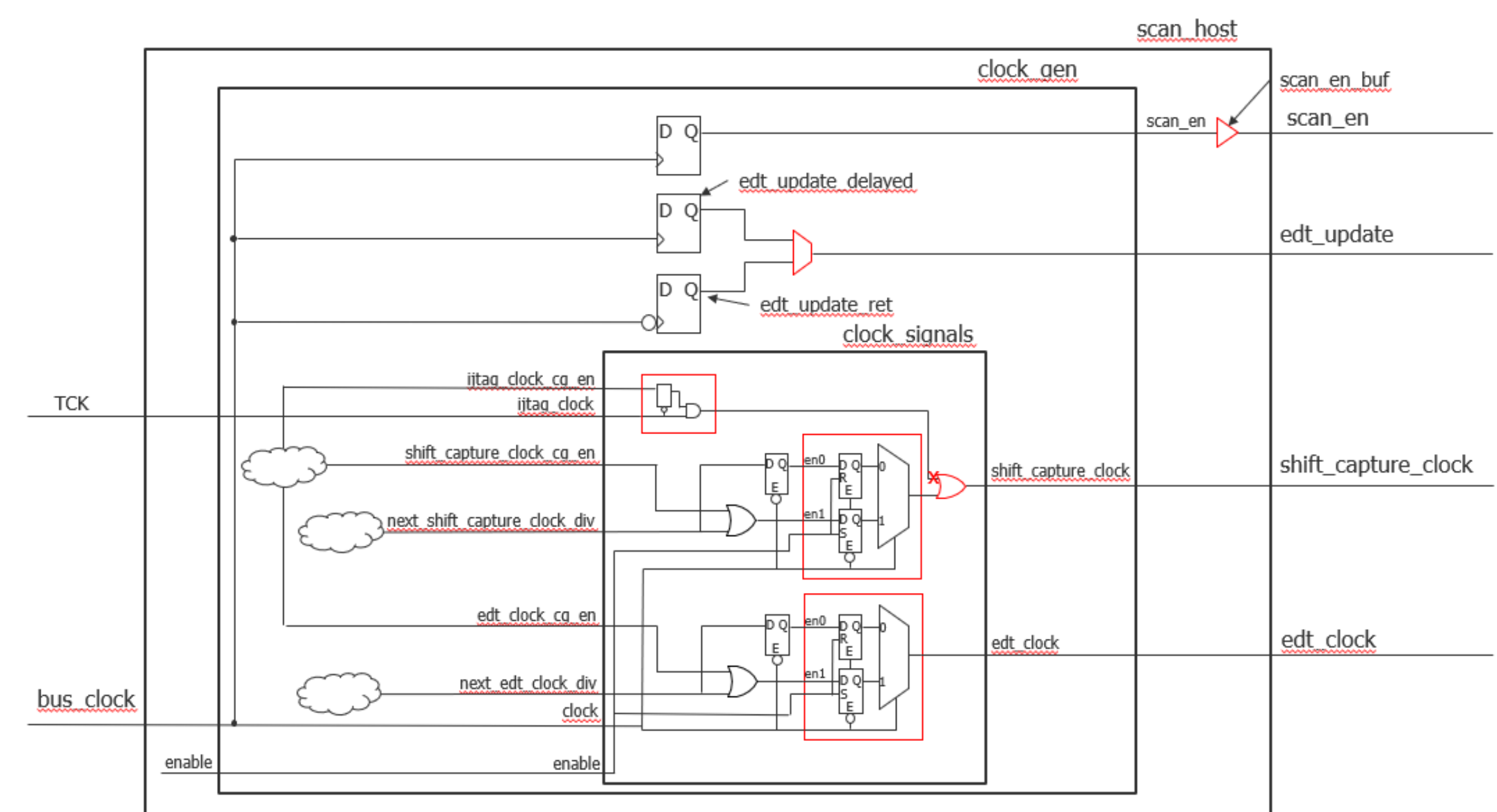
Abstract

Packetized scan data delivery is a trending common practice for efficient delivery of test-pattern data. It addresses the challenges of limited chip I/O, routing and timing closure, test data volume and test time, test planning and implementation in designs with growing complexity. In such designs, it therefore becomes important to support clocking that can achieve these goals. This poster explains four clocking techniques to achieve the goals mentioned above.

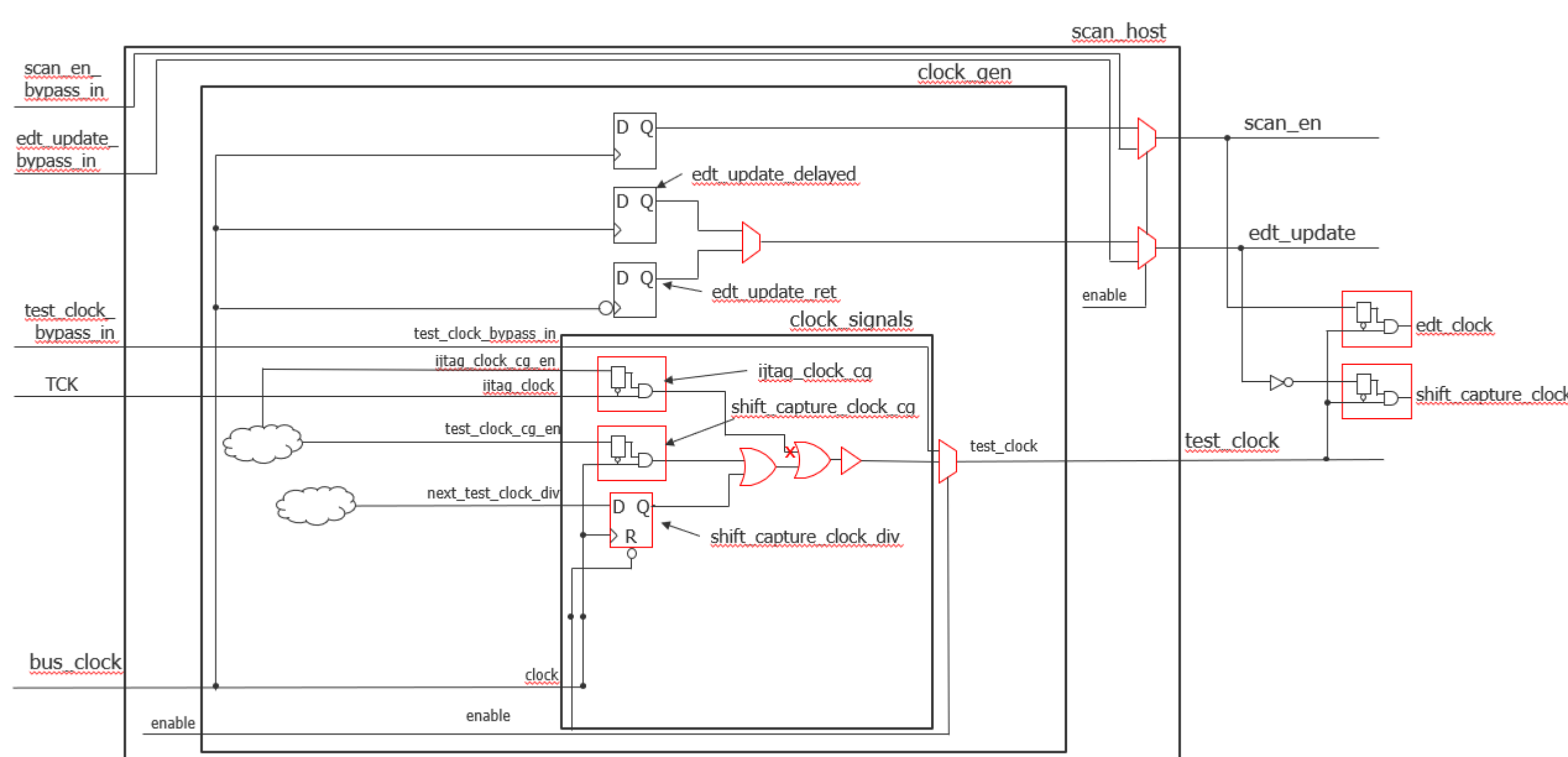
Method 1: Streaming Scan Host using Clock Gaters and Dividers to generate scan clocks



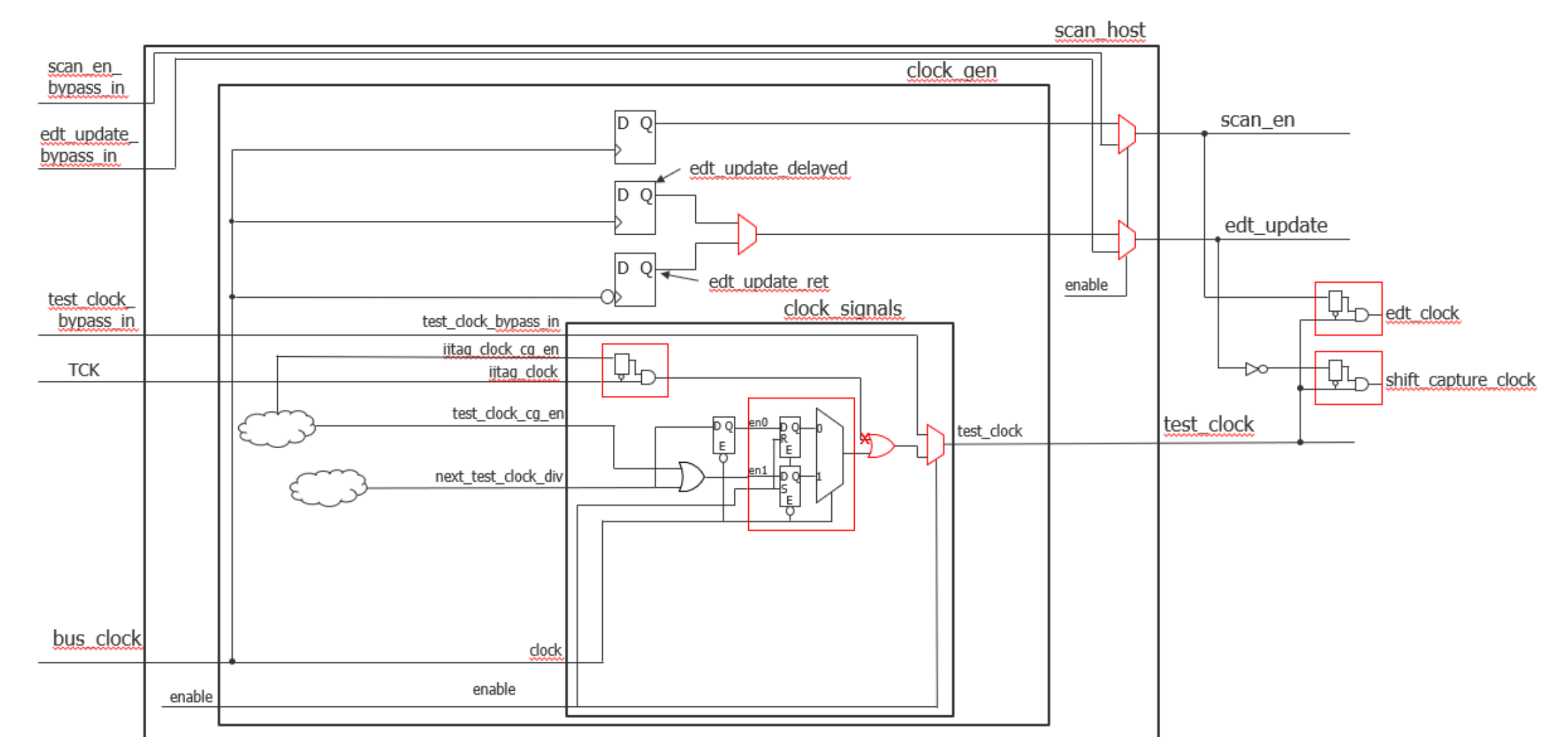
Method 3: Streaming Scan Host using a Clock Shaper Cell to generate scan clocks



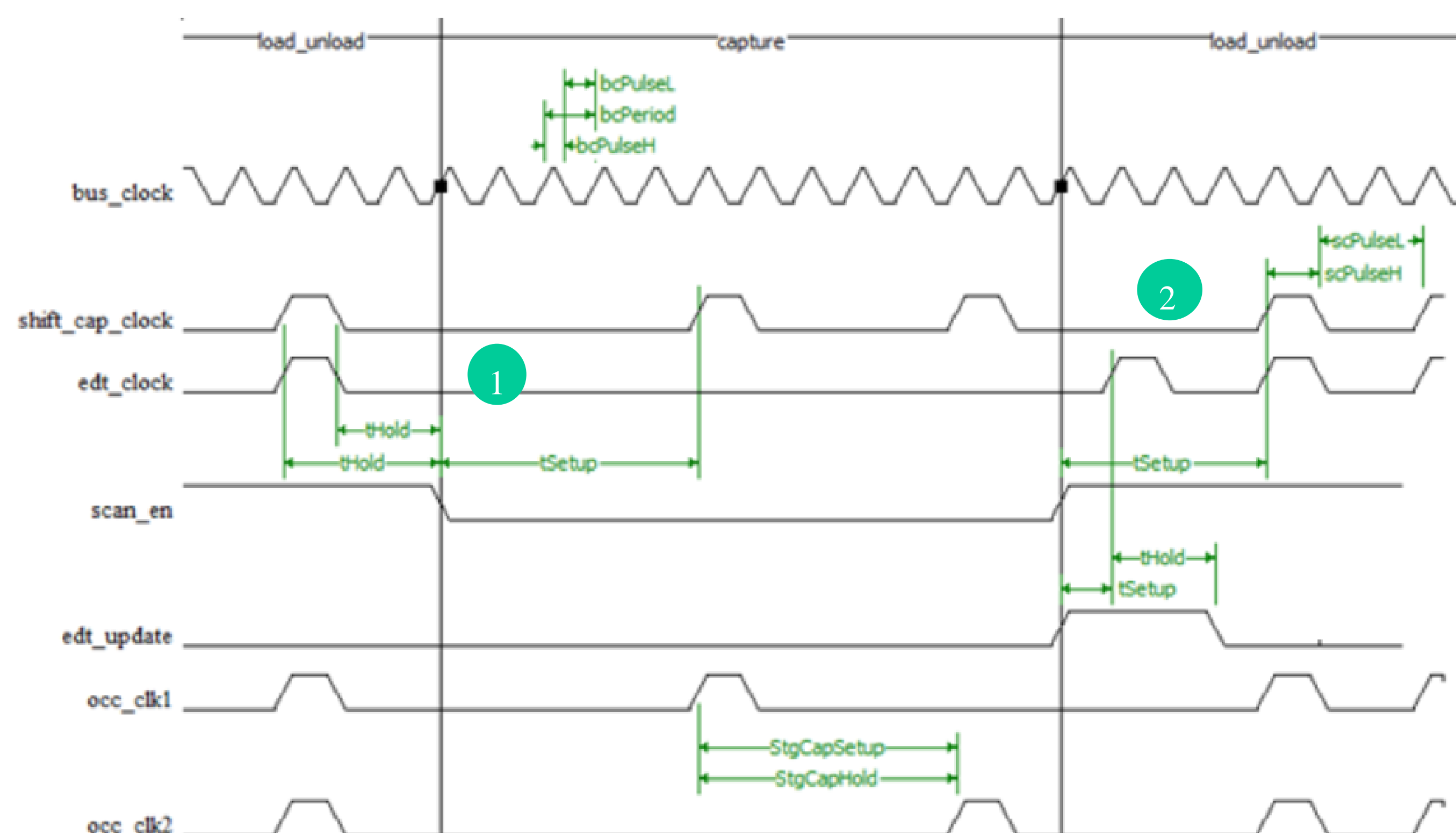
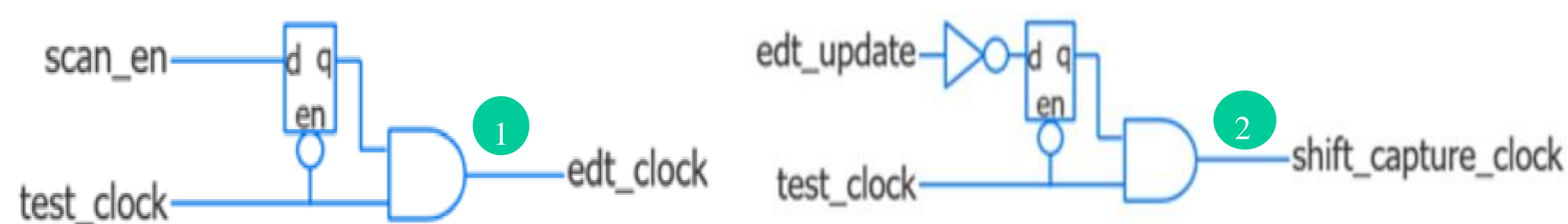
Method 2: Streaming Scan Host using Clock Gater and Divider for test_clock (clock-gaters/scan control signals to generate scan clocks)



Method 4: Streaming Scan Host using Clock Shaper for test_clock (clock-gaters/scan control signals to generate scan clocks)



Using test_clock, clock-gaters and scan control signals to generate scan-clocks



Summary : Clock Generation methods

Method	Clocking Method Description	Advantages/Disadvantages
1	Clock Gaters/Dividers→ shift_capture_clk, edt_clk	<ul style="list-style-type: none"> Simple standard cells used Disadvantage: Reconvergence of clocks
2	Clock gaters/Dividers→ test_clock→ shift_capture_clk, edt_clk	<ul style="list-style-type: none"> Better timing w/ clock gating cells more local Only test clock needs to be balanced Disadvantage: Reconvergence of clocks
3	Clock Shapers→ shift_capture_clk, edt_clk	<ul style="list-style-type: none"> Single timing mode No timing reconvergent paths
4	Clock Shapers→ test_clock→ shift_capture_clk, edt_clk	<ul style="list-style-type: none"> Clock Shaper allows to have any clock waveform for a packetized data delivery mechanism Single timing mode, No timing reconvergent paths Fewer SDC constraints and clock definitions Recommended clocking methodology

Conclusion

Choosing clock shaper over clock gaters and dividers leads to ease of timing closure. Picking a clocking methodology that is most suited for a design need can help maximize the use of scan streaming technology for test data volume and test time reduction without adding challenges to timing closure and implementation.