Accelerated 3D IC DFT Development

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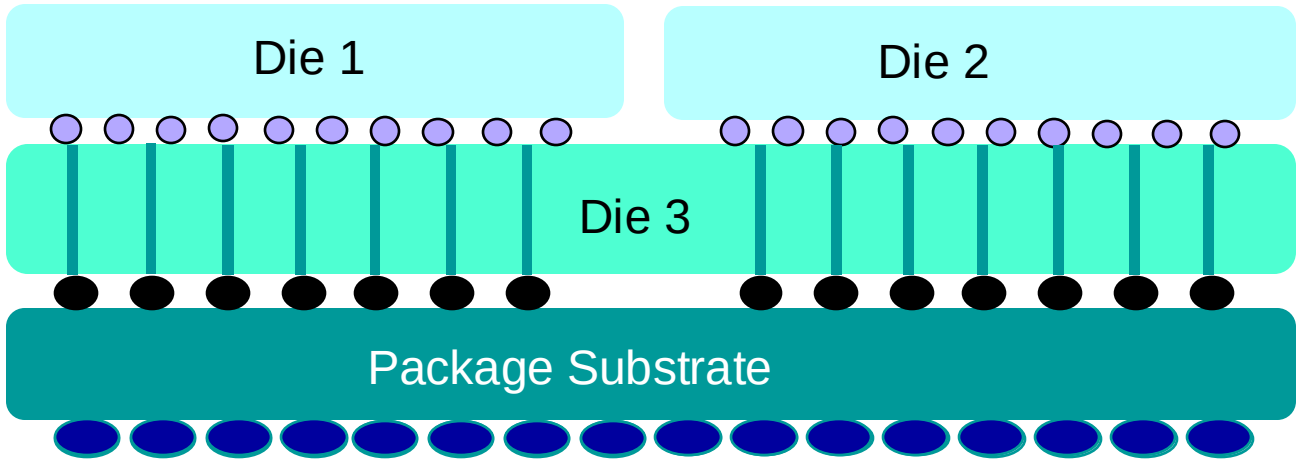
DFT Challenges for 3D Stack Design



New Challenges

- Accessing upper dies in a 3D stack
- Test die-to-die paths in the package
- Known Good Die testing during wafer sort
- Power consideration during testing in a 3D stack package
- Turn Around Time for generation, verification and simulations of ATPG vectors

IEEE 1838 Standard

For test access architecture for 3D stacked IC

New standard for 3D IC DFT architecture

Serial Access Mechanism

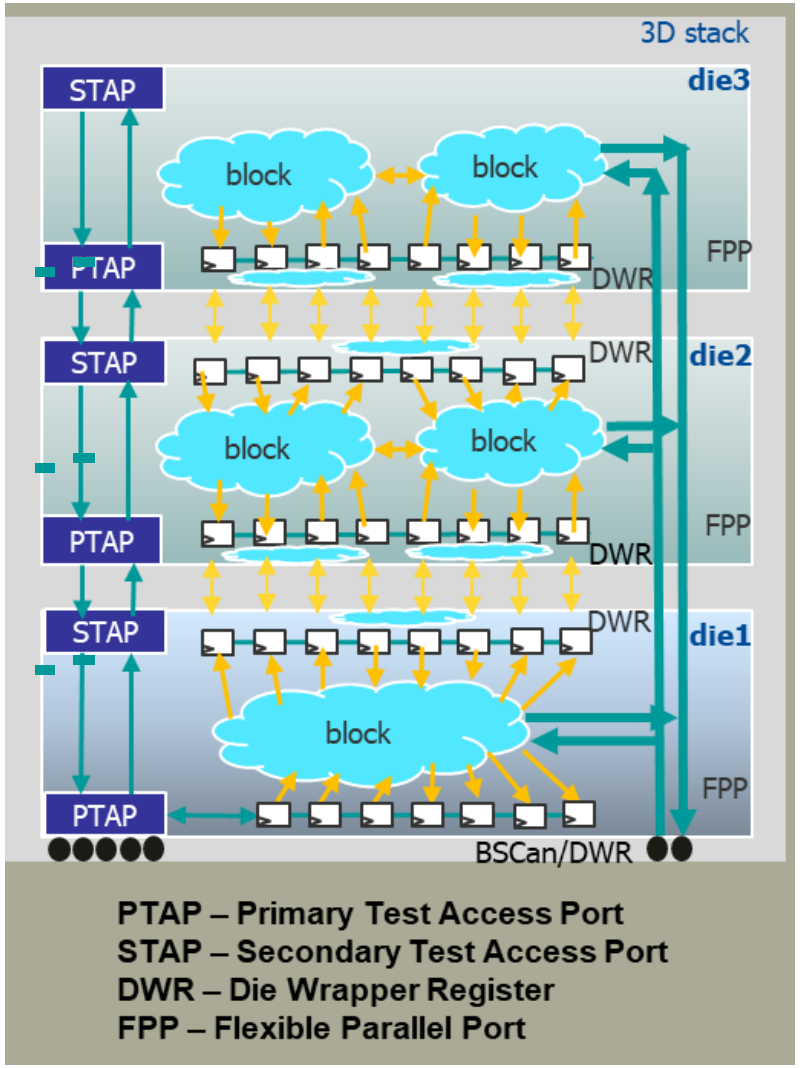
- PTAP – additional instructions and hardware like 3DCR register
- STAP – acts like a gatekeeper for serial access to upper dies
- Optional pipelines to ease timing closure

Die Wrapper Register

- Logic to test the inter-die paths

Flexible Parallel Port (FPP)

- Parallel bus port to load/unload the scan data



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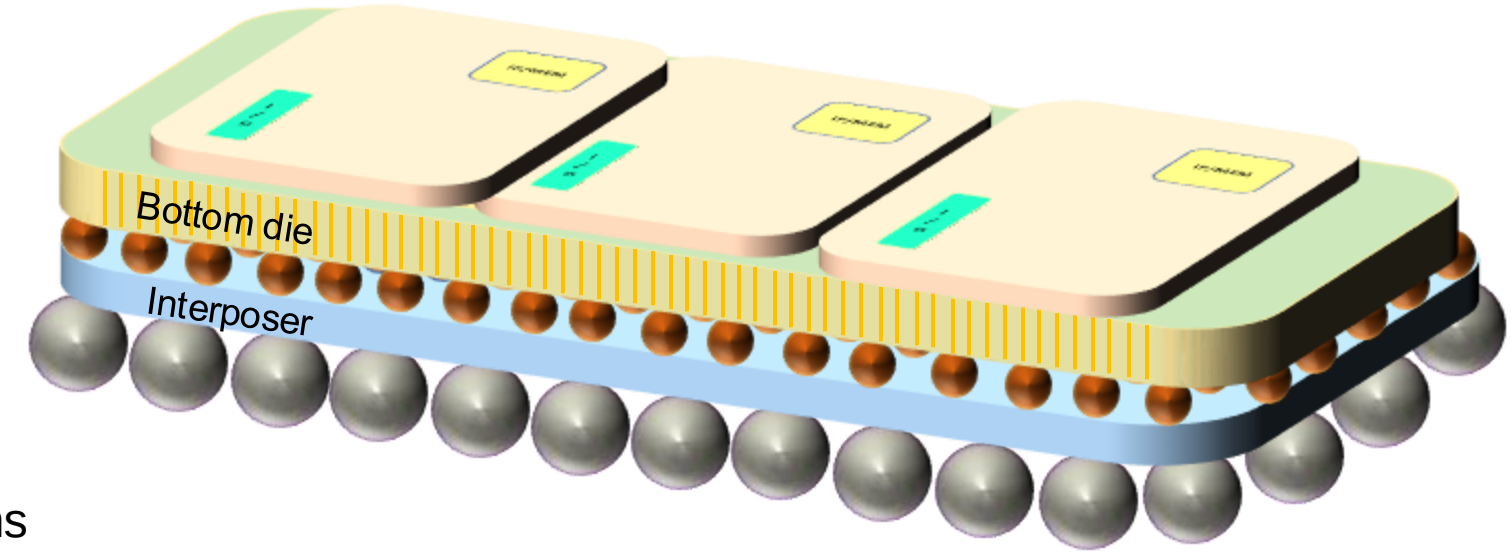
Unified BSDL

For System-in-Package (SiP) testing

Two categories of I/O

- I/O connecting to the other dies
- I/O connecting to the package pins



Unified (single package-level) BSDL

- I/O connected to the package pins
- 1-bit BYPASS register
- 32-bit DEVICE_ID register from the PTAP in the bottom die for the entire package
- IEEE 1149.1 compliance

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Known Good Die

For wafer sort testing

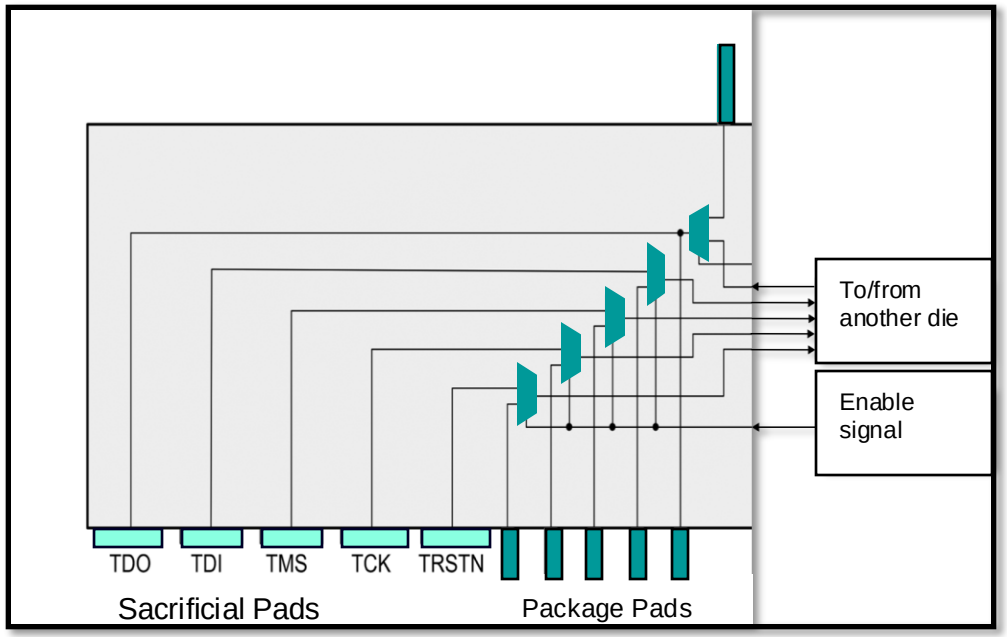
Verify the dies bonded into the package are fully functional

Key challenges

- Fine micro bump pitch used for the chips in multi-die packages
- Noisy and high RLC tester load environment

Sacrificial Pads

- Subset of probe pads with standard spacing
- Unused after wafer sort testing
- Minimum requirement for clocks/resets, JTAG signals, FPP pins to deliver scan data during test
- Careful analysis of package and signal integrity required
- Muxed pad technique automatically inserted by the tool to select wafer or package path



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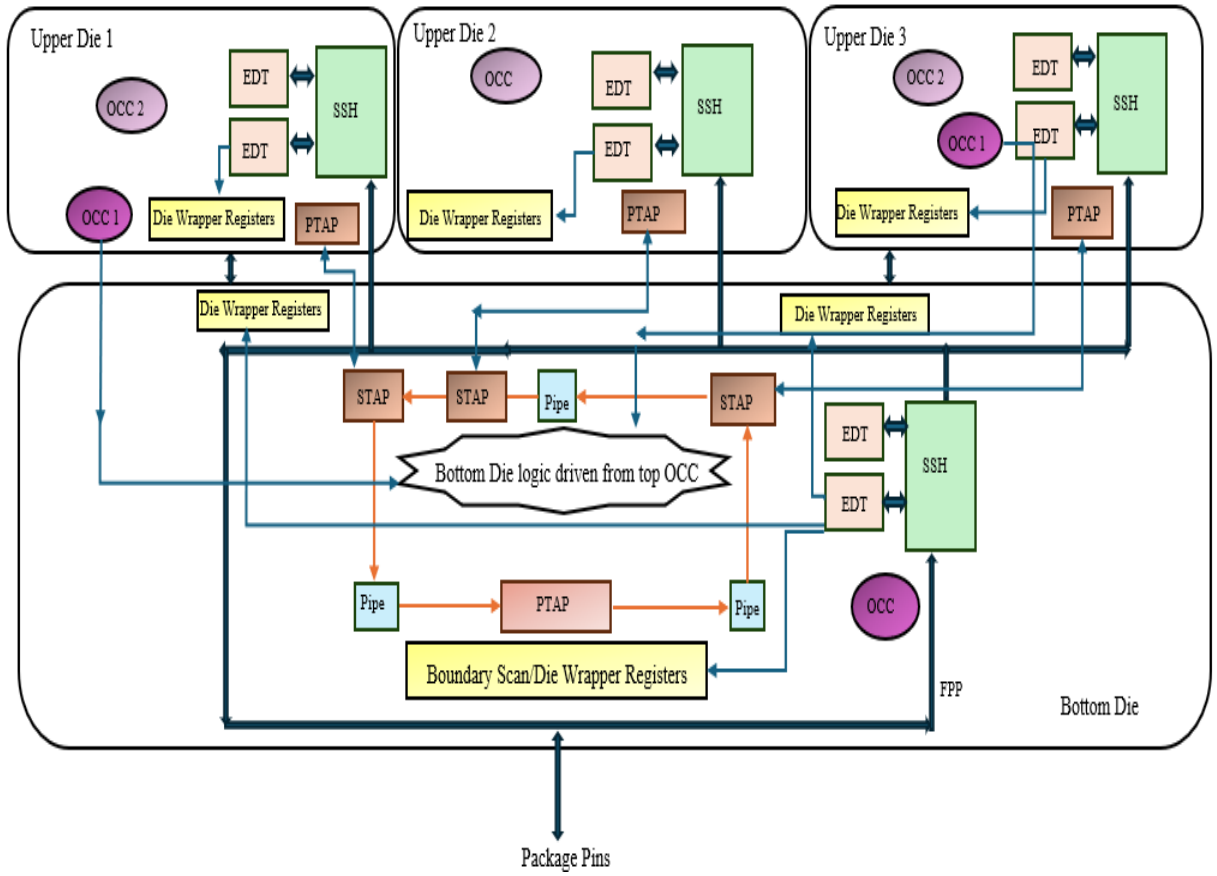
5.5D Stack Design with Tessent Multi-die

Complete solution for any stack configuration

- ✓ Serial access using STAP and PTAP
- ✓ Pipelines in the IJTAG network to ease timing
- ✓ Parallel access using single SSH per die as an FPP
- ✓ Automatic identification of Die Wrapper Registers
- ✓ Unified BSDL for System-in-Package, IEEE 1149.1 compliant
- ✓ Sacrificial probe pads for upper dies
- ✓ Pattern retargeting from core to die to package



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Summary

Tessent Multi-Die significantly boosted productivity and shortened deployment time for 5.5D device

IEEE 1838 standard with packetized scan data delivery mechanism successfully validated on silicon

Packetized data delivery is inherently power friendly along with low power ATPG features

Gray box netlist to significantly reduce pattern generation and simulations runtime

Pattern retargeting from core to die to package

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