Using SSN for 3DIC with Tessent Multi-die

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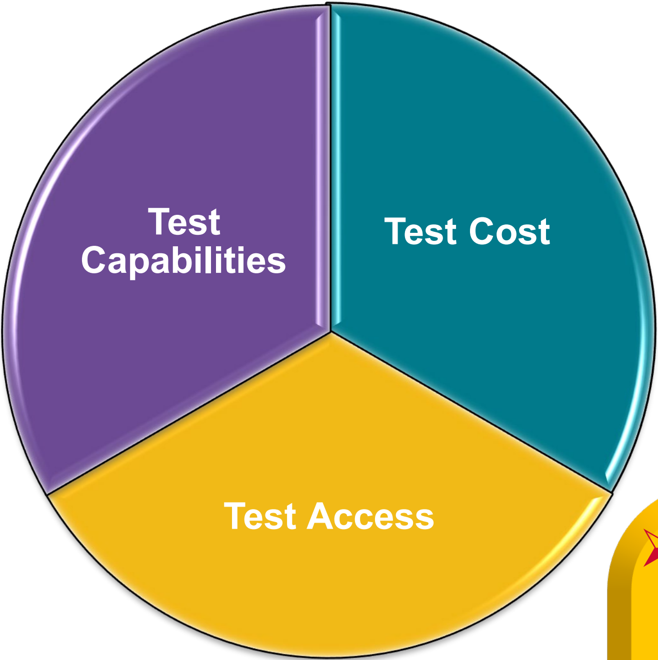
3DIC Test Challenges

- Known-Good-Die (KGD) & Known-Good-Interposer (KGI)
- 3D TSV/Interconnect Testing
- High-speed IO Testing
- Thermal Cooling considerations
- Test & Repair Capabilities
- Failure Diagnostics Capabilities
- Advanced Test methods



- Main concern is YIELD
- Test flow optimization
- Capex for μbump probing?
- Tools to model costs
- End-to-end data analytics

- Inter-Die, Intra-Die & System-in-Package Access
- Reduced Pin-count DFT/Test methods
- Probing challenges
- Security features
- Power Down/Up

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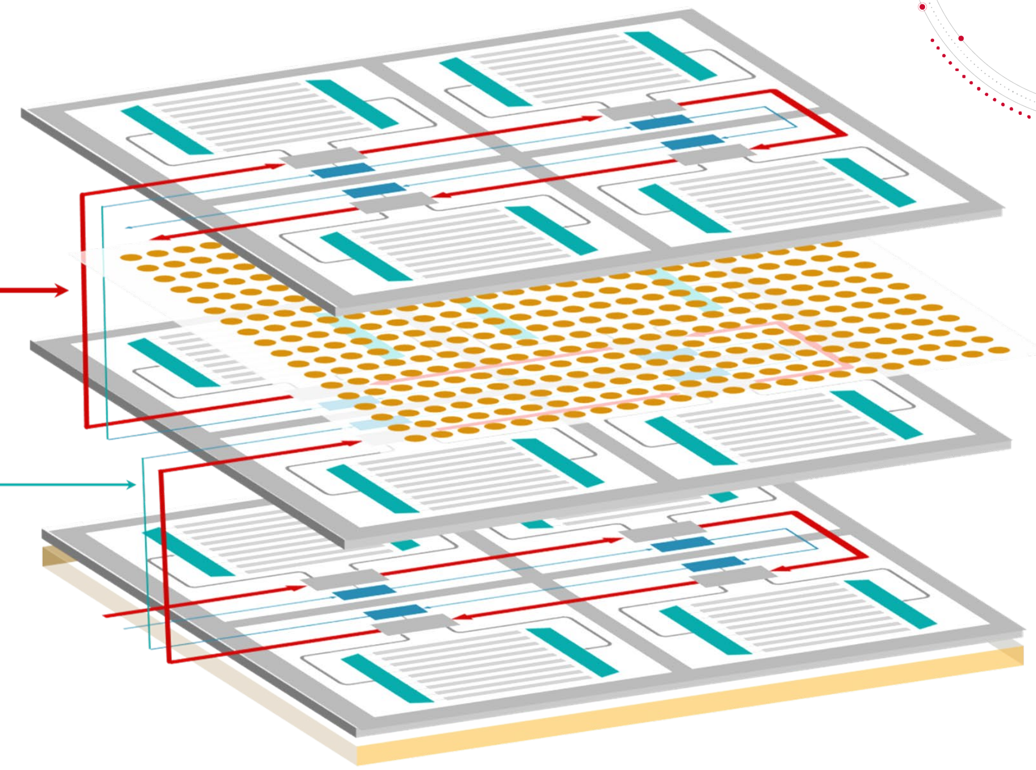
Tessent Solution for 3D IC



- **Improved productivity with 3D IC design scaling**
  - **Hierarchical DFT methodology for reuse and pattern targeting**
  - **Retargeted test setup automation with IJTAG infrastructure**
  - **Soft-programmable test access from package to die via SSN (Streaming Scan Network) bus**

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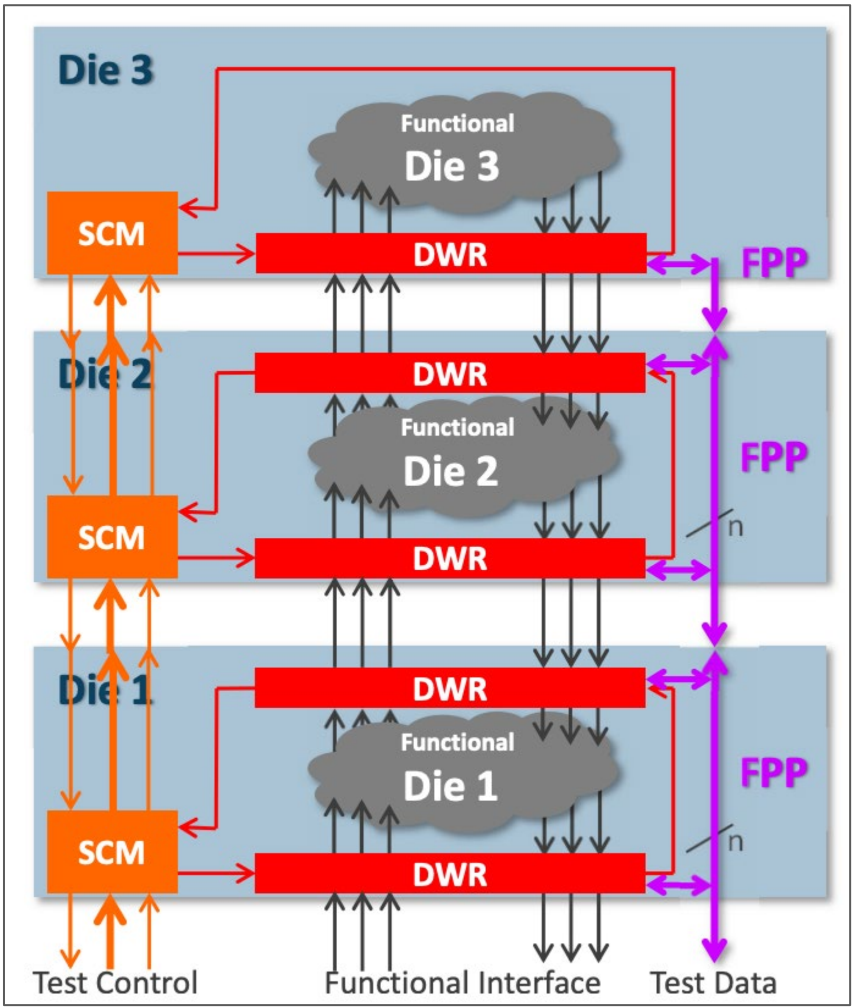
IEEE 1838 – An Introduction

- IEEE 1838 specifies mandatory and optional 3D-DFT features per die
- Enables die and interconnect testing separately
- Compliant dies in a 3DIC stack form a consistent test architecture
- Connect various IP modules under test to external test equipment

DFT Feature	Mandatory/ Optional	Description
SCM (Serial Control Mechanism)	Mandatory	Access to die TAPs from package
DWR (Die Wrapper Register)	Mandatory	Die Isolation similar to core wrapping concept in hierarchical test methodology
FPP (Flexible Parallel Port)	Optional	Useful for control/observe die pins (e.g. scan in/out)



Source: IEEE Computer Society

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SCM – TAP Controllers

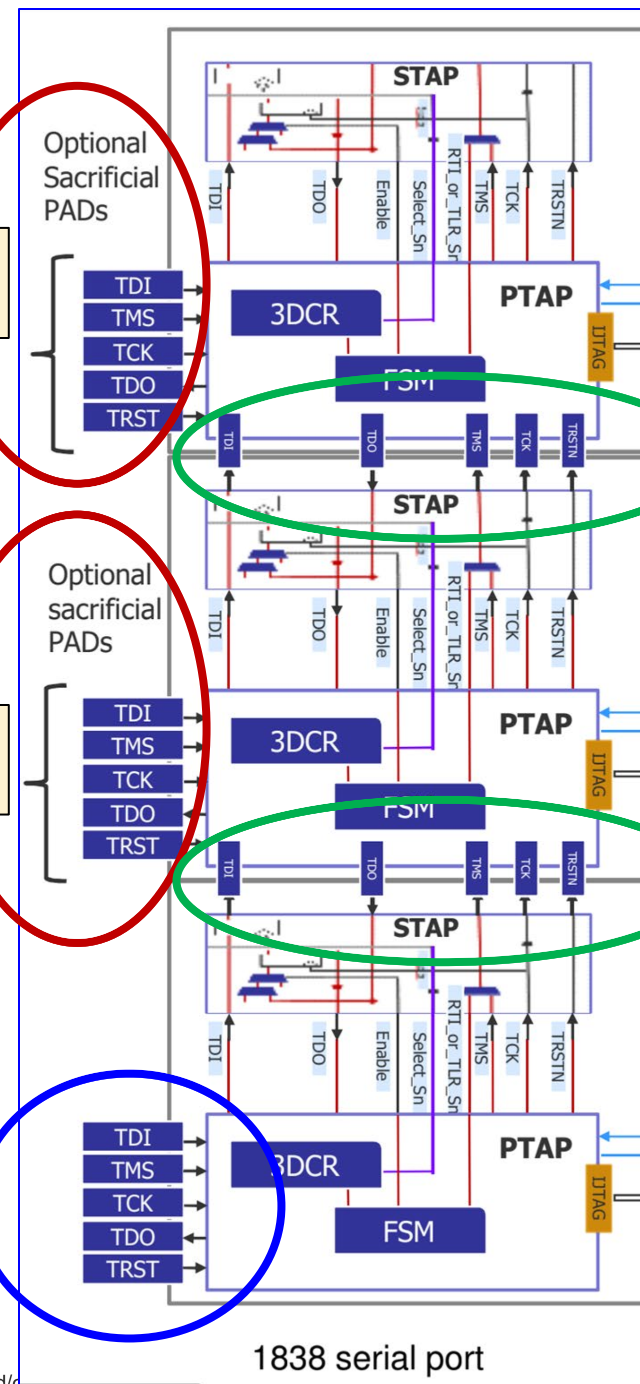
- PTAP and STAP IPs
- PTAP – Augment existing TAP for IEEE1838
  - Existing TAP support IP testing
- STAP – New IP generated using Tessent
- Use of sacrificial pads for wafer level testing

Re-use of TAP as PTAP is achieved using Tessent Multi-die

Wafer Level Access Only

Wafer Level Access Only

Package Level Access



TAP connections b/w chiplets in the stack for package level access – **HCB connections**

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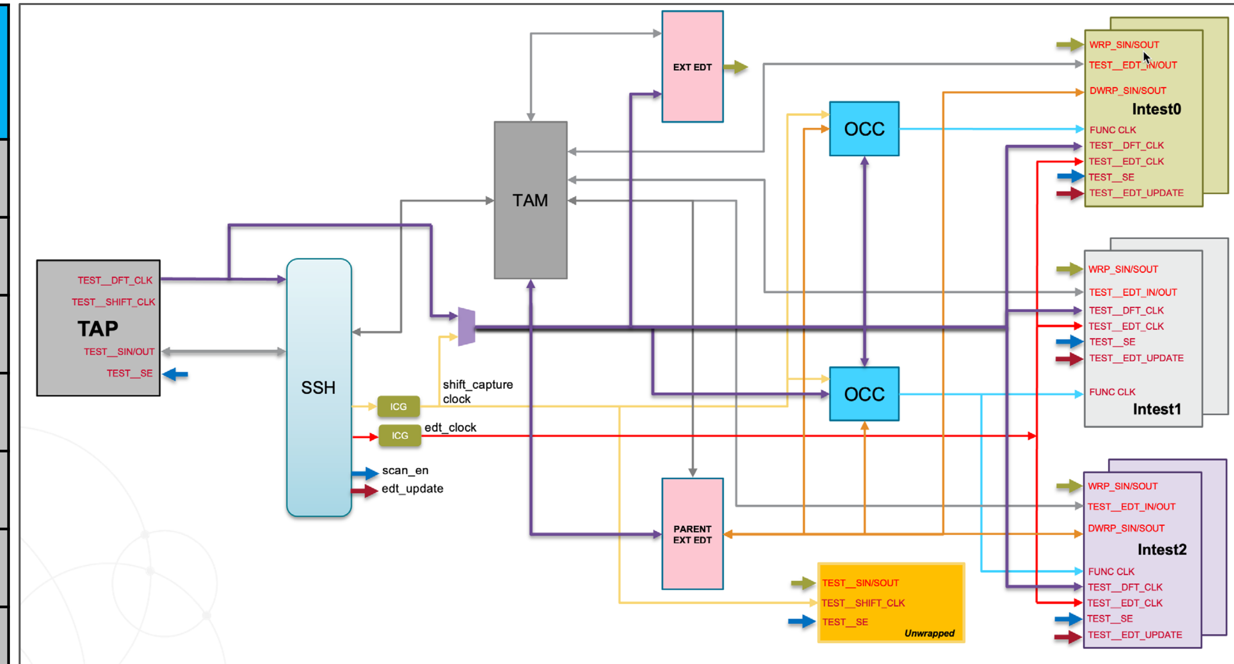
Die Wrapper Register (DWR) and test modes

Scan Configurations	Unwrapped Core	Wrapped Core	Die Top
multi_mode	YES	NO	NO
int_multi_mode	NO	YES	NO
int_edt_mode	NO	YES	NO
int_single_mode	NO	YES	NO
ext_mode	NO	YES	NO
die_ext_mode	YES	YES	YES
extest_multi_mode	NO	NO	YES
edt_mode	NO	NO	YES
single_mode	NO	NO	YES



Core DFT Flow changes for cores interfacing between die-to-die

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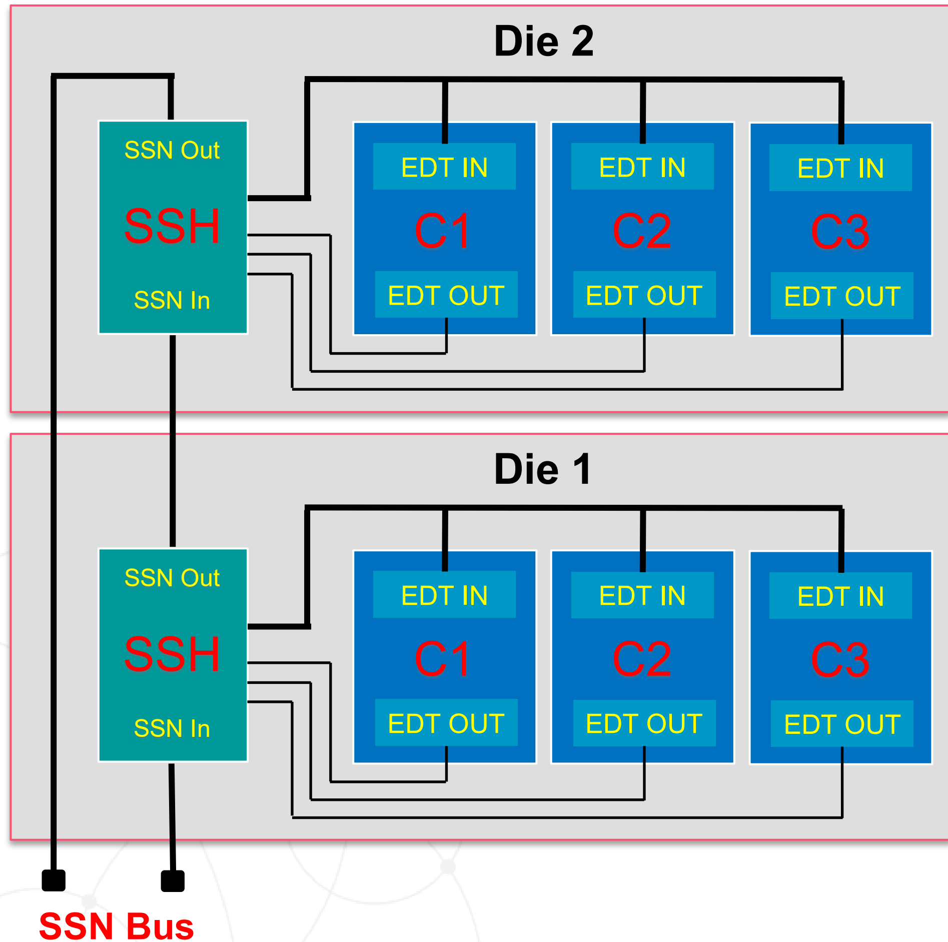
FPP – SSN for Die-level Scan Access



- SSH: Streaming Scan Host
- SSN: Streaming Scan Network
- Single SSH per die: "***SSN-lite***"
- SSH scan broadcast to identical cores
- Separate EDT out from each core
- Pattern retargeting: **Block > Core > Die > Package**
- Reverse failure mapping from package-level SSN Bus to core (core-level diagnosis)
- Wafer and Package testing using separate set of pins on die
  - Wafer level will have sacrificial pads
  - Package level will use the SSN bus path
- Physical design & Static Timing Analysis Considerations

Re-use existing core level DFT flow, core wrapped IPs in 3DIC testing

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Summary

01

3D Stacked SiPs are needed to support Broadcom's Compute Offload products

02

Wider Adoption of 3DIC requires Testing solutions for Enhanced Test Access, Test Capabilities & Managing Test Costs

03

Tessent Multi die product has enabled several key changes in existing DFT flows while re-using majority of IPs to support 3DIC Test Challenges to speed up time to market

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