Efficient test port access to address test time

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Test access background

The introduction of disaggregated architecture, has brought new challenges to High Volume Manufacturing (HVM) that traditional approaches might no longer be capable of managing efficiently. Historically, HVM has relied on either complex IO circuits (i.e., DDR Phy) or simpler GPIO's. Despite success in the past, these test ports carry the following limitations :

- Prevents testing of multiple die concurrently
- Unable to improve the bandwidth in case of GPIO
- Impact functional performance

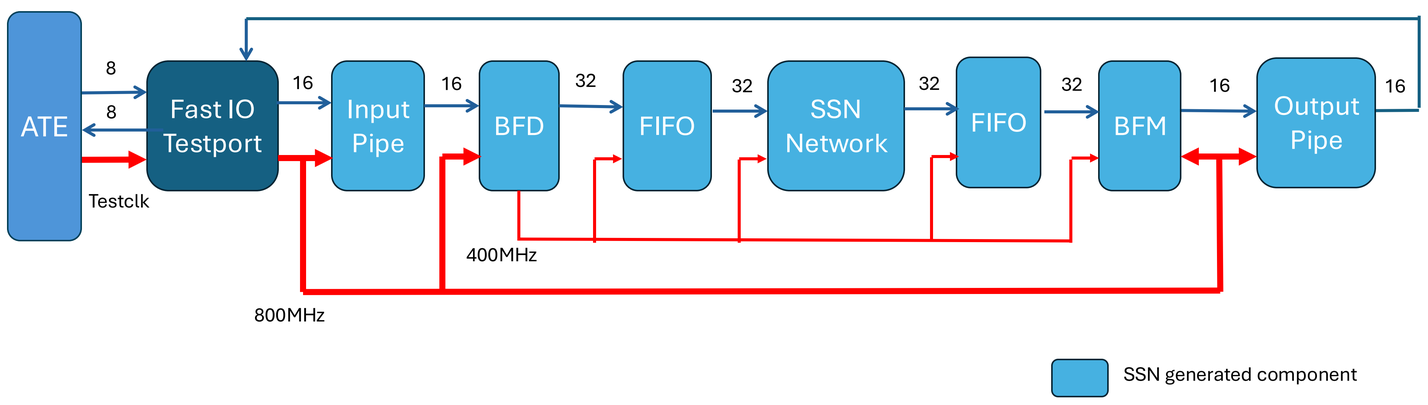
A custom test port can be a viable solution and designed to exceed the bandwidth of traditional GPIOs and have a small IO pad count and minimal die area for affordability.

Existing high-speed interfaces, like PCIe and USB, meets the bandwidth requirements but present issues such as

- large die area cost,
- Complexities using PHY and inability to debug at arbitrary data rates
- Requires non-standard ATE test equipment, or needing costlier capable test cards

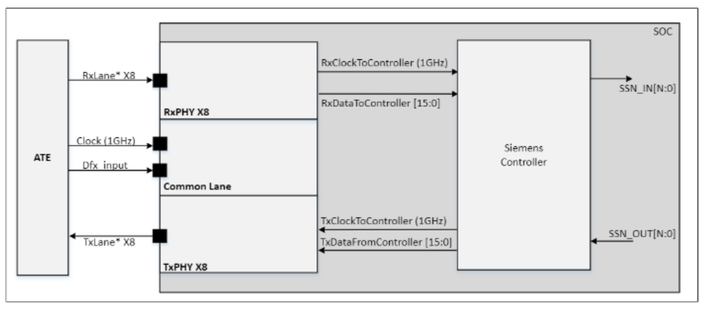
SSN Fast IO – Implementation

- The Fast IO solution uses a dedicated test port that de-couples the previous dependencies.
- A Fast IO can consume around 100 gates per IO and scales from a three pin IO count to any justified width count.
- Speed is targeted to be 5x per IO than previous test port access. The solution relies on existing ATE software capabilities in HVM to train the interface levels and timings to reduce design complexity resulting in far lower DUT die area costs.
  - Example of a Fast IO implementation with 8 data lanes is shown here :



SSN Fast IO – Building blocks

- All Data and Clock signals between the ATE and the SOC are single-ended.
- The channel environment is typically 50Ω, and the Rx and Tx SOC impedances are calibrated for a match.
- Each receiver lane will de-serialize the data stream into a 2-bit word, that will be concatenated along the 8 other channels to form a 16-bit word delivered to the SSN controller alongside the Receiver clock. Similarly, each transmitter lane is expecting a 2-bit word (16-bit for all 8 TX blocks) alongside the clock used in the SSN controller, Tx block will convert each 2-bit word into a serial stream of data.



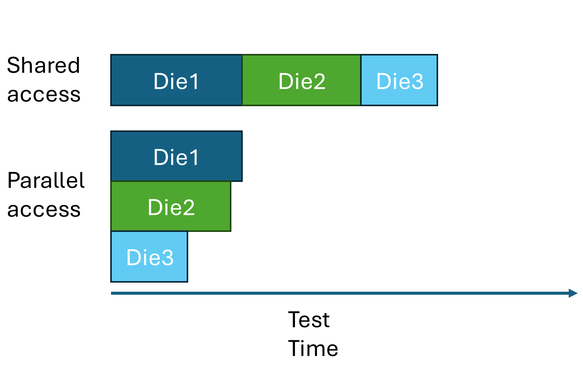
SSN Fast IO – Bandwidth

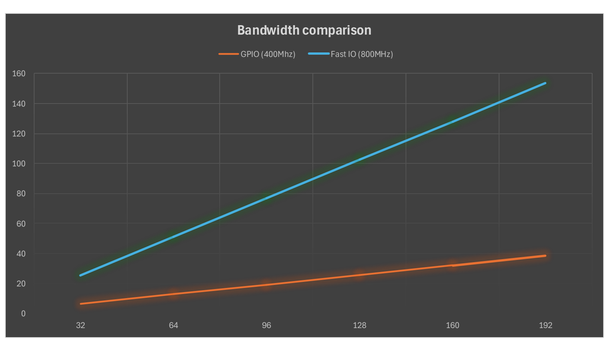
Based on the usage on an Intel chip, the SSN Fast IO test port was designed with 8 data lanes (Tx and Rx) and a common lane for clock reception. The clock signal is driven by the ATE and as such the frequency is limited by the ATE. All data lanes are operating at double data rate (DDR) where data is transferred on both rising and falling edge of the clock, achieving a data rate of 1.6 Gbps per lane (assuming a 800 MHz driven ATE test clock). The bandwidth when compared against a typical GPIO solution :

	GPIO – 200MHz	GPIO – 400MHz	Fast IO
Number of Ports	32 In / 32 Out	32 In / 32 Out	8 In / 8 Out
Speed frequency	200MHz	400 MHz	800MHz
Scan Data Bandwidth	6.4 Gbps	12.8 Gbps	12.8 Gbps

Addressing Test Time

- The test time benefit with the SSN Fast IO solution is attained in either :
  - Dedicated Fast IO access to each die-let, allowing full parallelism vs common test port across all dies
  - Widening the SSN bus width through expanding the Fast IO data lanes. Bandwidth comparison between pin matching count of GPIO and Fast IO :





Summary

The SSN Fast IO concept has been successfully implemented on an Intel chip achieving high bandwidth through fewer pins and DDR clocking. It has also benefitted aspects of :

- Tester reuse : it's architected to work on traditional cheap ATE without need of any specialized hardware or software support.
- Simple IO calibration : A short (~300mS) calibration is done through traditional ATE to compensate for any on-die resistance and timing variations.

SSN Fast IO interface addresses test access complexity particularly in die-let based designs. This interface is solely utilized for test, and due to its low pin count, allows independent test port access to each die-let. As such SSN Fast IO enables parallel testing, maximizing test time benefits and does not require any costly functional ATE test cards.