Deterministic on-chip compare and diagnosis
Tessent Streaming Scan Network

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Siemens EDA

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SSN Successes

Intel

Paper Video Silicon

- 10x productivity gain
- 50% scan test cost reduction
- Multi-die (2.5D) proven

SSN Pilot Study

Glenn Colon-Bonet

Sr. Principal Engineer
Intel Corporation, Design Engineering Group

Available for Q&A
Wednesday 2:00PM-2:20PM EST
In Mentor's Streaming Scan Network ITC booth

SSN implementation on a large multi-die SOC

Dave Dehnert
Principal Engineer
Intel

Broadcom

Video Silicon

- SSN enables 2X shift frequency
- 30mV favorable difference in shmoo
- Reduced test cost for identical cores

Enhancing test on 3GHz designs with SSN

Srinu Alampally
Master Engineer
Broadcom

Qualcomm

Silicon

- Meets scalability requirements
- Successful in silicon

Scalable DFT Architectures for 5G SoCs

Jais Abraham

Director – Engineering
Qualcomm India Pvt. Ltd

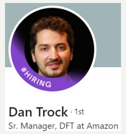
Available for Q&A
Wednesday 11:00AM-11:20AM EST
In Mentor's Streaming Scan Network ITC booth

- 9 of top 10 Tessent customers adopting / evaluating SSN
- 12 designs in silicon
- 11 additional tape-outs

Amazon

Quote Silicon

- Graviton3 server chip
- SSN bus at 370 MHz
- Huge step on performance, power efficiency, and cost



Dan Trock · 1st
Sr. Manager, DFT at Amazon

TSMC

PR

- DFT reference flow leveraging SSN for TMSC 3DFabric
- OIP partner of the year award

Arm

- SSN reference flow for Arm Neoverse subsystem
- Presented at ITC 2021, available from Siemens or Arm

Samsung

Video PR

- Significantly reduces effort to make complex designs highly testable
- Design Solution Kit (reference flow) with SSN

Sangyun Kim
VP Design Technology
Samsung Foundry

Overview

- SSN ATPG modes
- Recommended test patterns
- Deterministic on-chip compare
- Identical cores

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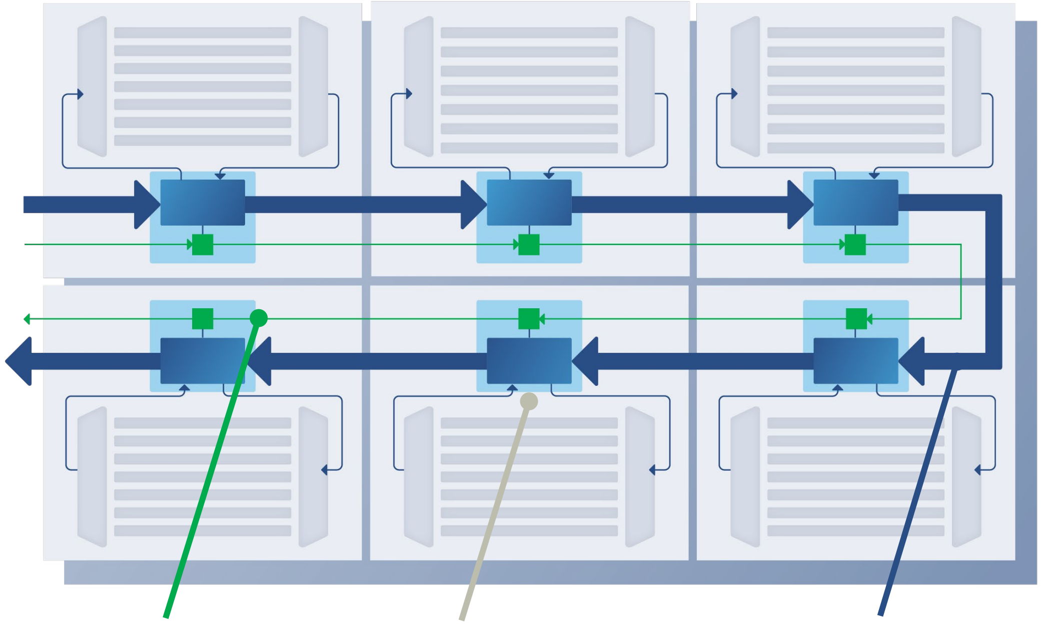
Tessent Streaming Scan Network (SSN) ATPG modes: Taking Plug-and-Play to the Next Level



Configuration or streaming through IJTAG

Locally generated DFT signals

N-bit wide high speed SSN bus for packetized scan data

☑ Silicon proven

- Cut DFT development time in half or more
  - Decouple core and chip level DFT
  - Define core grouping at retargeting time
  - Bus can be any width, even 1 bit
- Eases routing and timing closure
  - Eliminates top-level test mode muxing
  - Supports tile-based design with abutment
- Up to 4X test time and volume reduction
  - Packets are 100% scan data payload
  - Virtually eliminates scan vector padding
  - Optimal core compression
  - Time multiplexing
  - All compressors can run simultaneously
  - Identical cores tested at constant cost
  - Full diagnosis support

SSN Manufacturing Patterns

Recommended SSN simulations and manufacturing patterns

Order of priority

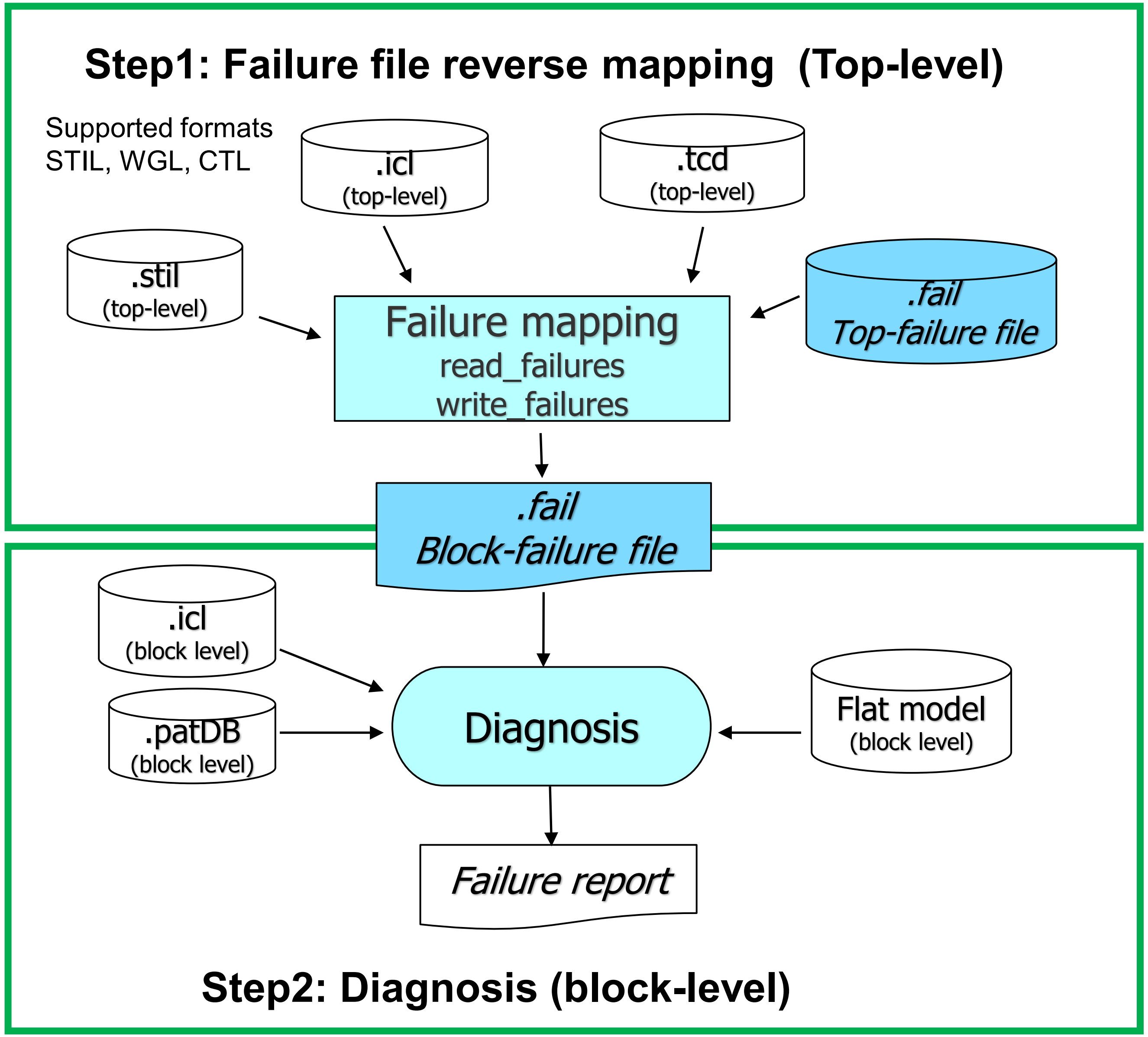
	**ICLNetwork Verify patterns	Continuity pattern	OCComp Self-Test Pattern	Loopback pattern	Retargeted SSN patterns	Top-level ATPG SSN patterns
1st silicon test	✓	✓	✓	✓	✓(chain test) ✓(scan test)	✓(chain test) ✓(scan test)
Production test	*	*	✓	*	✓(chain test) ✓(scan test)	✓(chain test) ✓***(scan test)

*Optional pattern and can be used to identify the cause of failure

**Includes verification of streaming-through-IJTAG

***SSN Retargeting parallel testbench is used only to verify clocking during scan pattern retargeting

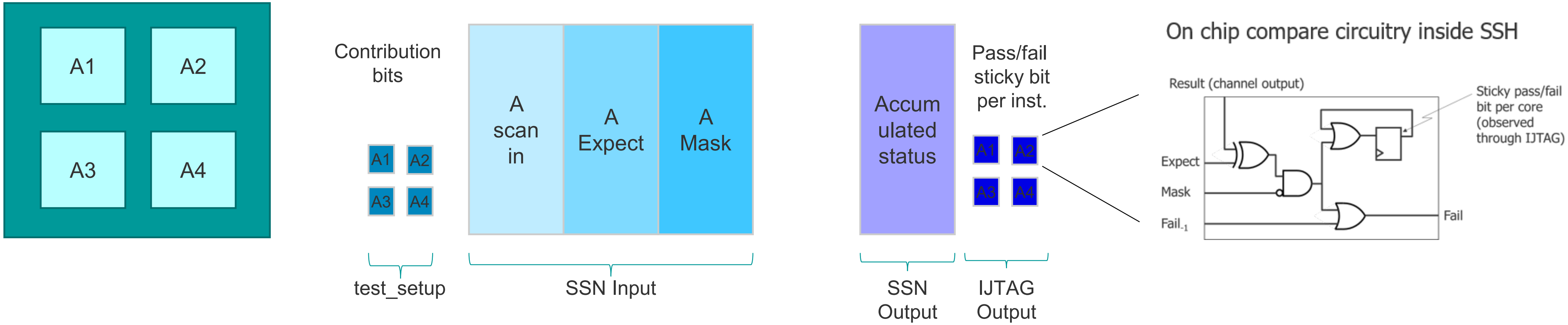
Reverse failure mapping and Tessent Diagnosis



- Step 1: Map top level failures to the block
- Step 2: Diagnose/correct the block failures
- Step 3: Regenerate block vectors/retarget to top

- Quick to respin/retarget vectors for a single block
- SSN packet format fully understood by Tessent diagnosis
- Can add physical data for further fault resolution

On-chip compare: Optimizing test for identical cores



- Fail data measured in two locations for our example
  - One pass/fail “sticky” bit per core scanned out through IJTAG at the end of pattern set
  - ssn_bus_out can be deactivated for reduced tester memory in volume production test
  - Accumulated “status” scan responses from all core instances from SSN bus
- Modify a bit in test_setup to determine which core(s) contributed to accumulated unload status
  - By default, all cores contribute
    - Full diagnosability if a single core fails or nonidentical cores fail
    - Step through each core individually and diagnose for identical cores failing

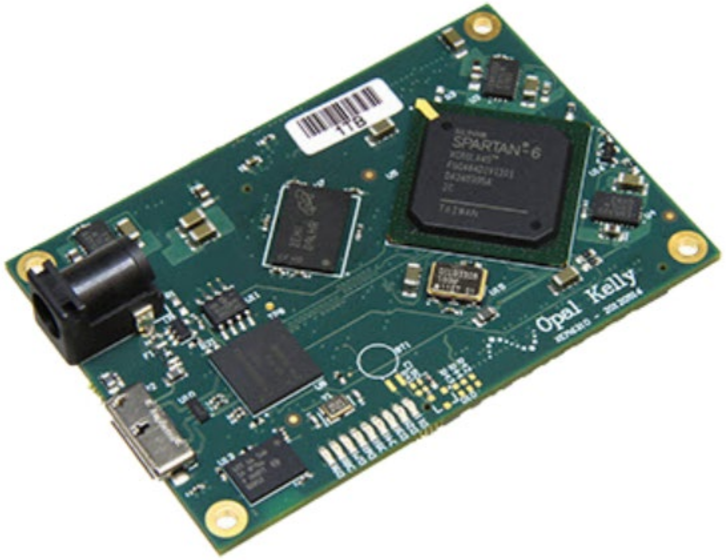
Summary

- On-chip comparison of deterministic ATPG data.
- A single sticky-bit is generated per block or EDT channel
- Saves tester volume and even test time for volume production test
- Additional capabilities can be derived for yield improvement
- Scan shift is much faster when SSN bus outputs are masked
- Failing identical blocks can be diagnosed by selecting the blocks one-at-a time
- Tessent diagnosis is fully compatible with SSN packet data.
- Reduced scan volume from reusing identical core patterns
- On-chip compare can be run on just part of the chip, standard compare on the rest.

Thank You

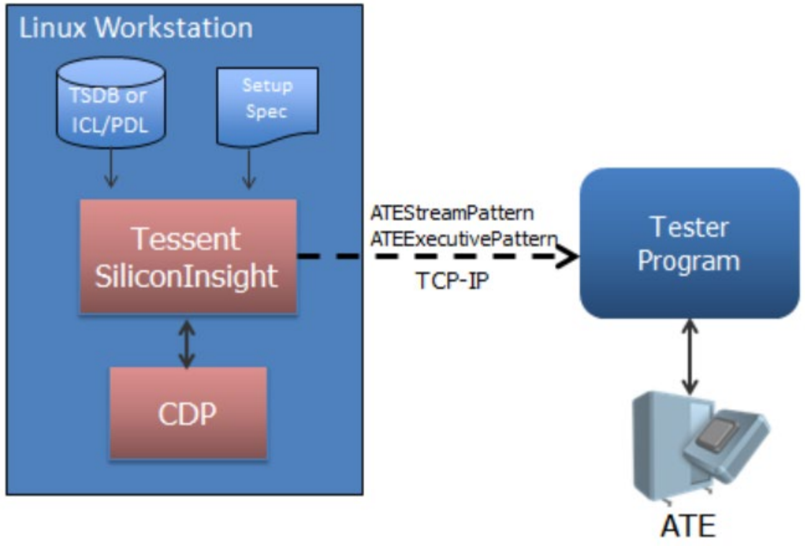
SiliconInsight bench testing

- Opal Kelly XEM 6310 board – currently up to 120 IO's
  - IO will more than double in near future
  - MBIST/LBIST/ATPG
- OpenOCD TAP interface boards – restricted for MBIST/LBIST
- Bench board/socket for DUT.
- GPIB support for power supplies, ancillary test equipment, etc.



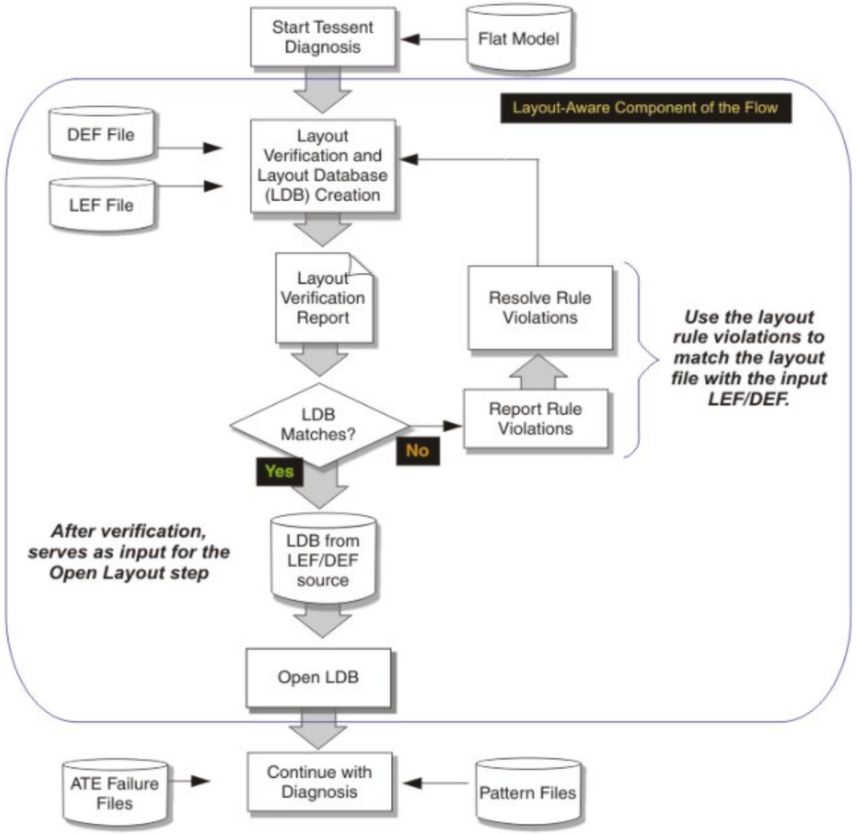
SiliconInsight ATE-Connect

- Allows remote SiliconInsight access and control of ATE for silicon bring-up, characterization, and debug.
  - Does not require ATE pattern translation step
- IJTAG to ATE program
- Advantest and Teradyne supported interfaces
  - API interface for other testers



Diagnosis

- MBIST/LBIST can be diagnosed in SiliconInsight
- ATPG diagnosis is accomplished with Tessent Diagnosis.
- A scan “failure file” is generated by SiliconInsight or ATE/datalog translation.
  - feeds forward into Tessent Diagnosis
- Tessent Diagnosis validates consistency for ICL, TSDB, Failure File and vectors.
- Can read LEF/DEF for “Physically aware” diagnosis
- Results in accurate fault classification for failing silicon.
- Tessent Diagnosis also understands SSN scan packet format, as will SiliconInsight in 2021.2



Start Tessent Diagnosis

Flat Model

Layout-Aware Component of the Flow

DEF File

LEF File

Layout Verification and Layout Database (LDB) Creation

Layout Verification Report

Resolve Rule Violations

Use the layout rule violations to match the layout file with the input LEF/DEF.

LDB Matches?

No

Yes

Report Rule Violations

After verification, serves as input for the Open Layout step

LDB from LEF/DEF source

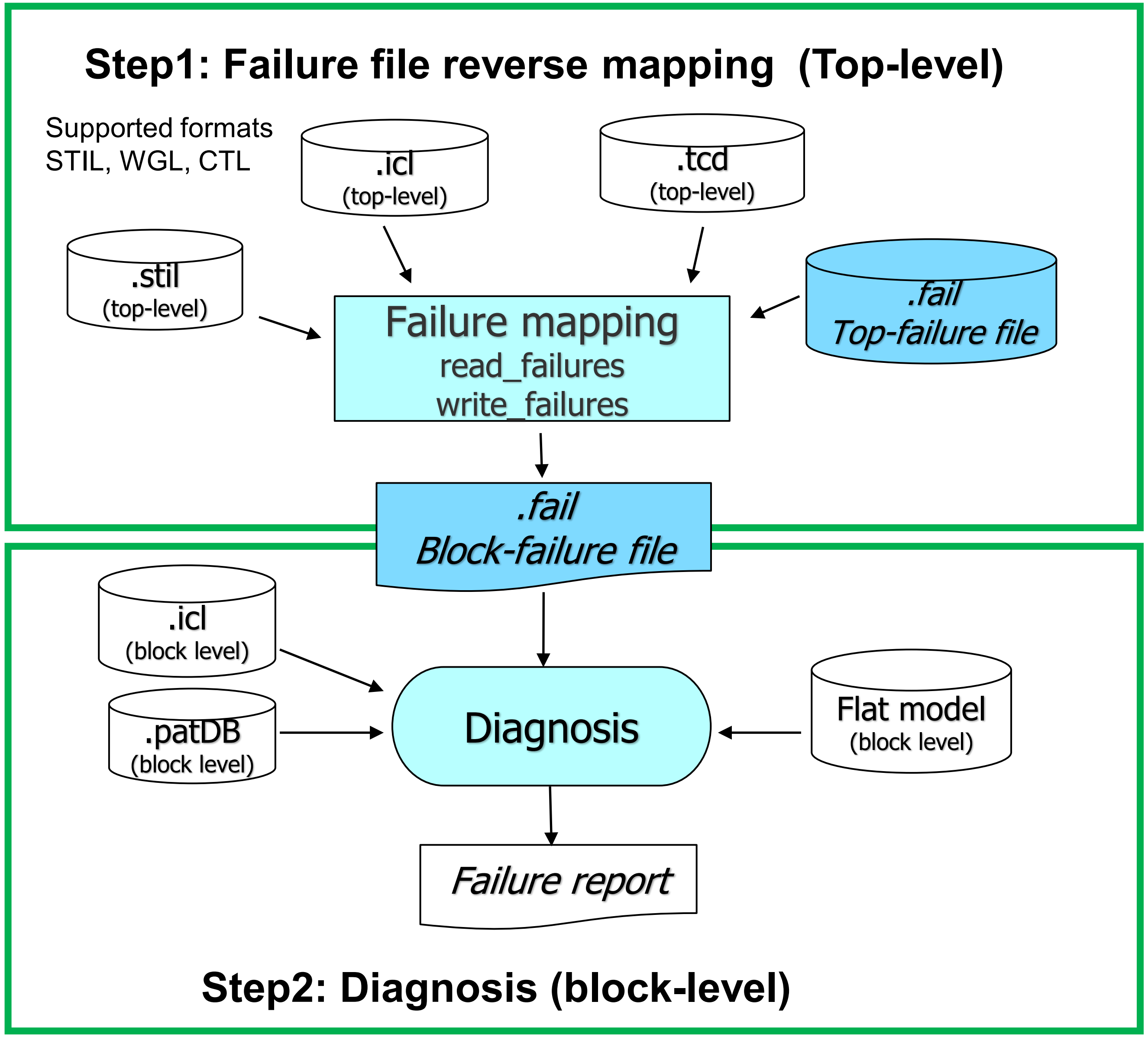
Open LDB

ATE Failure Files

Continue with Diagnosis

Pattern Files

Reverse failure mapping and Tessent Diagnosis



Step1: Failure file reverse mapping (Top-level)

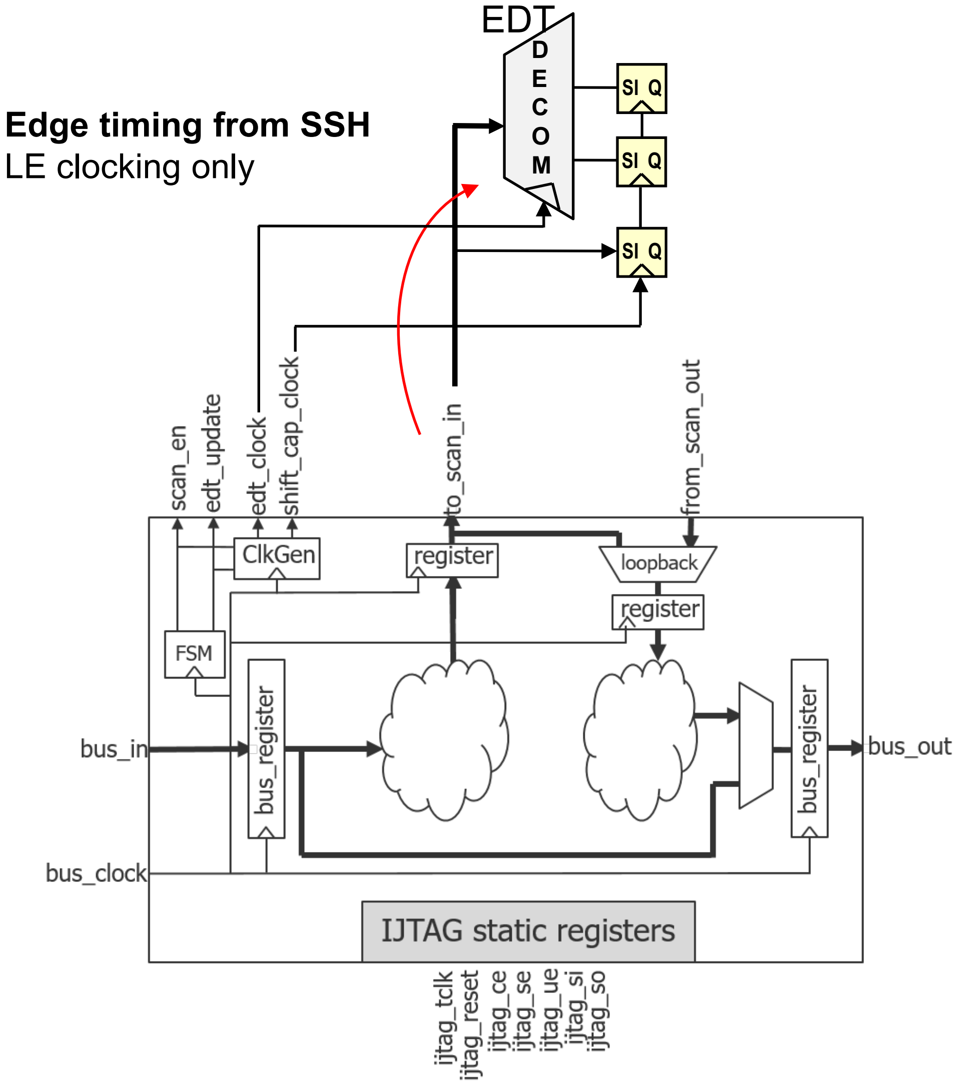
Step2: Diagnosis (block-level)

```
set_context patterns -failure_mapping
read_core_description top.tcd
set_current_design top
set_system_mode analysis
read_patterns top.stil
read_failures top.fail
write_failures <Block-failure file>_prefix
##above command generates block.fail##
report_failures -unmapped
```

```
set_context pattern -scan_diagnosis
open_tsdb ../block/tsdb_outdir
read_flat_model -design_name block \
 -mode stuck_atpg1 –design_id block_scan
read_patterns -fault_type stuck_at
diagnose_failure block.fail
```

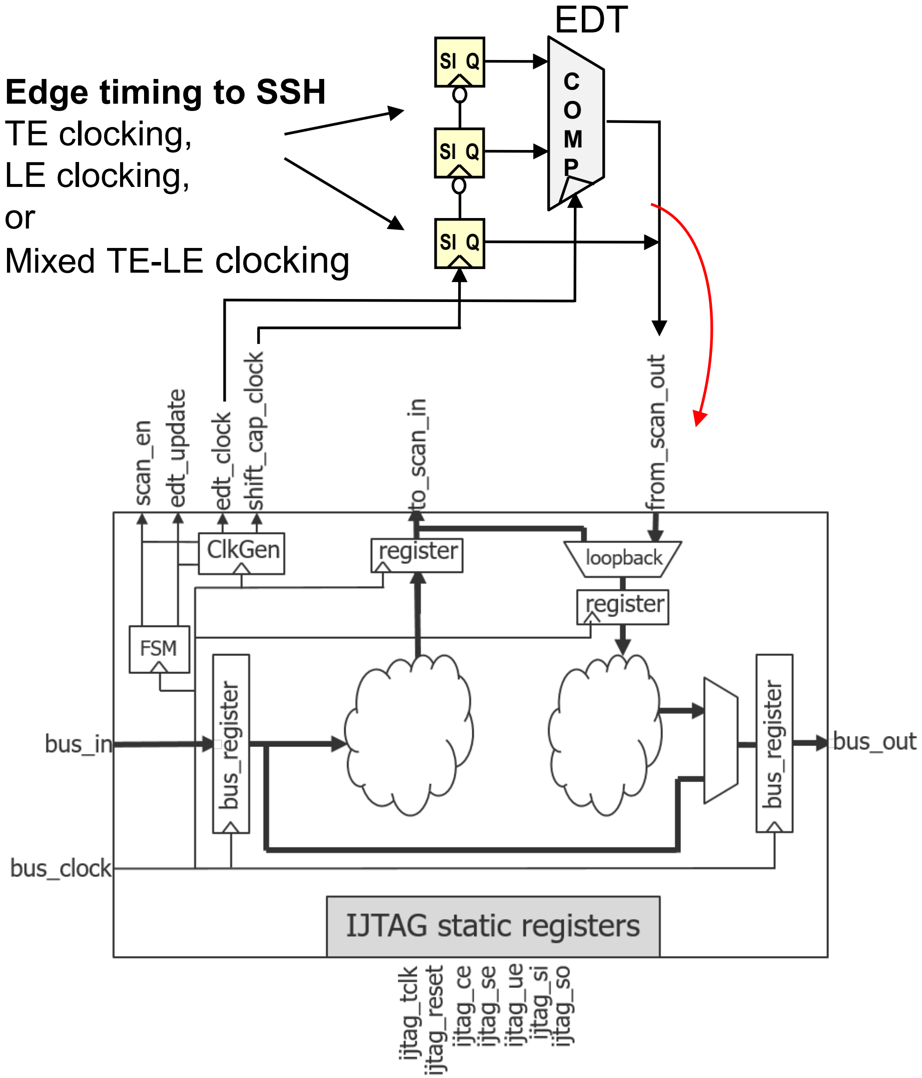
Backup

Understanding SSN Timing
From SSH to scan chains


Edge timing from SSH
LE clocking only

- Path from SSH can be any combination of compressed and uncompressed scan chains
- Timing from the SSH must be LE timing
  - Error is reported if violated
- Shift_capture_clock guaranteed later then bus_clock
  - One full clock cycle from SSH to the scan logic
  - Gated or divided version of bus_clock

Understanding SSN timing
Channel and chain timing to SSH

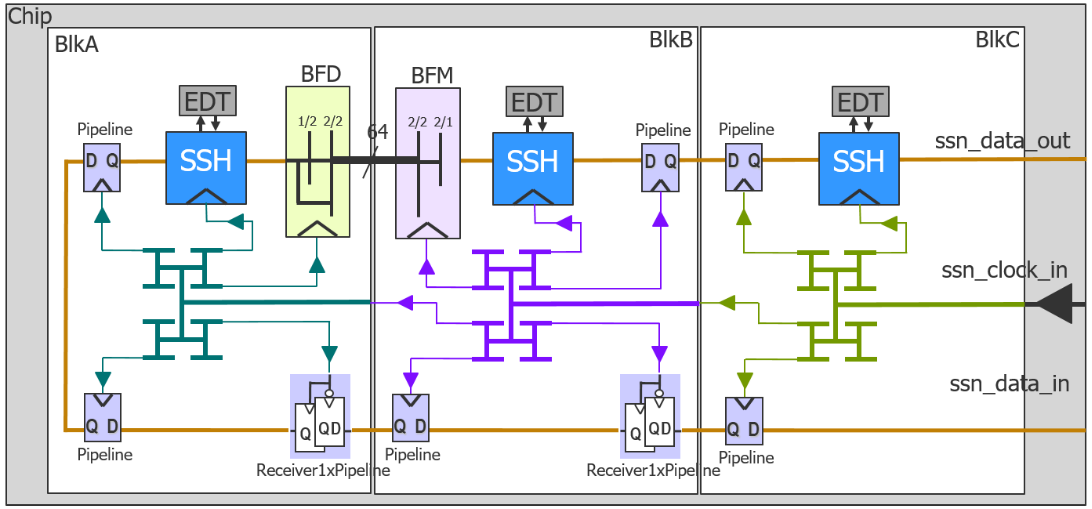


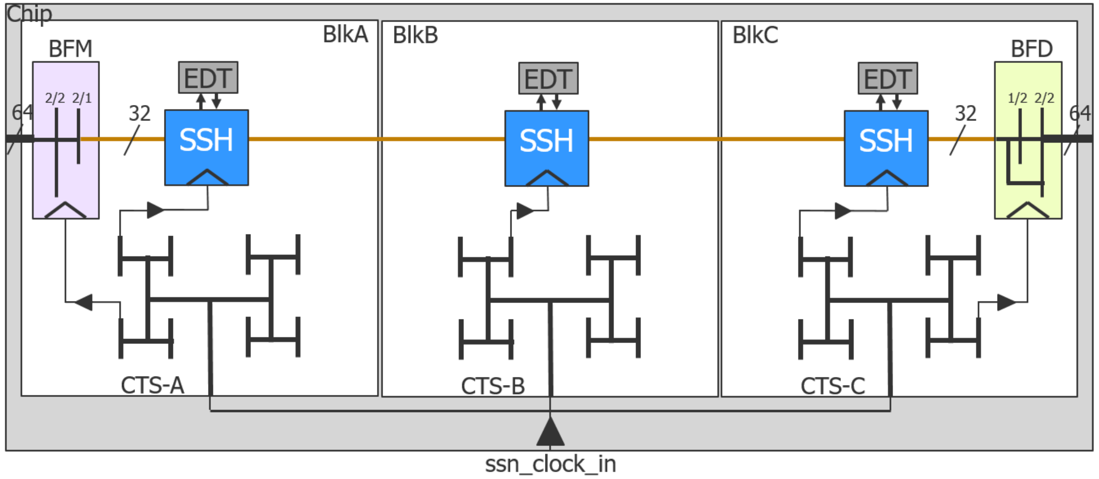
Edge timing to SSH
TE clocking,
LE clocking,
or
Mixed TE-LE clocking

- Path to SSH can be any combination of compressed and uncompressed scan chains
- Scan chain clocking to the SSH can be TE, LE, and mixed TE-LE
- For TE clocking
  - SSH strobe is on TE
  - Allowing full clock cycle to SSH
- For LE clocking
  - SSH strobe is on LE
  - Allowing full clock cycle to SSH
  - SSH requires additional hardware to support LE strobing
    - Enabled by default
      - SSH DftSpecification property, support_from_scan_out_le_strobing
    - Recommend keeping enabled – no affect on TE clocked scan sources
  - Error when LE strobing is required but doesn't exist.
- For mixed TE-LE clocking
  - SSH Strobe is on LE
  - Same additional hardware in SSH is required to support LE strobing
  - Warning of half-cycle path to SSH from TE scan sources

Advanced Topics
Managing timing of SSN datapath (1)

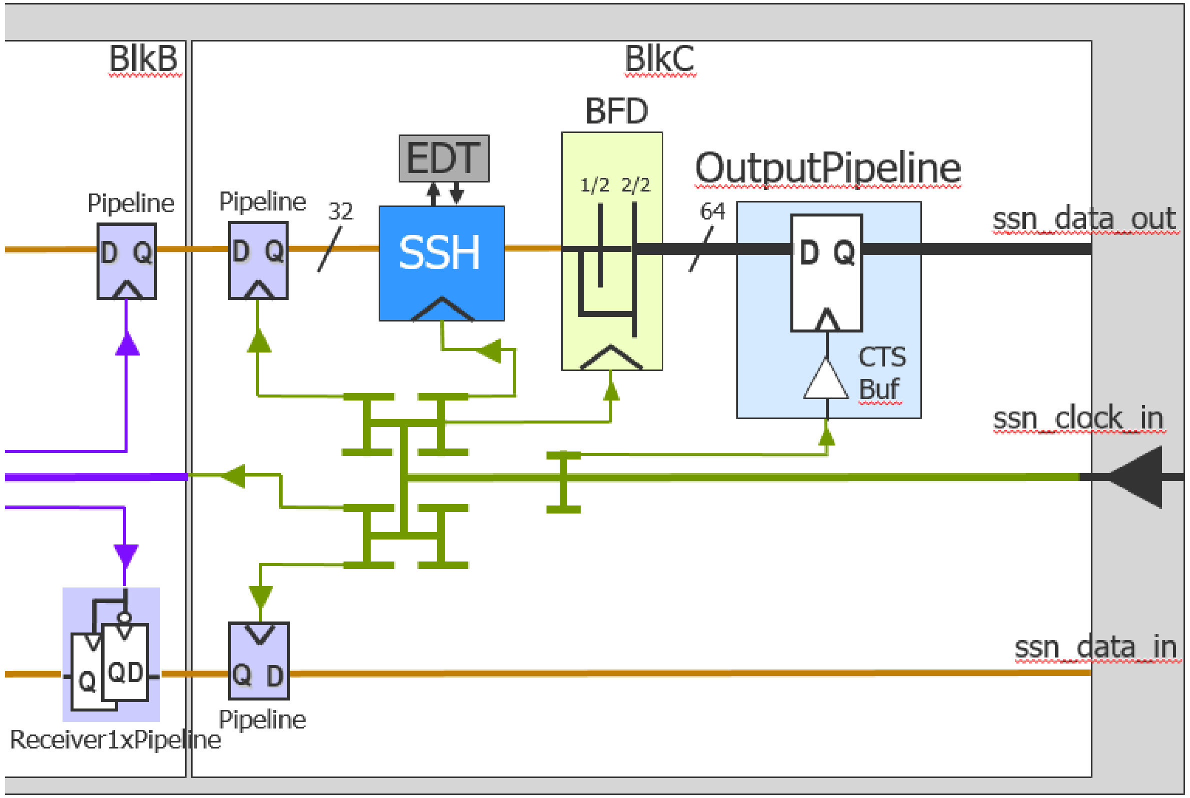
- Time multiplexing of SSN bus
  - Optional time division / multiplication of SSN bus
- BusFrequencyDivider
  - Slow down bus frequency and widen by factor of N
    - e.g. N=2 divide a 64 bus @400MHz to 128 bus @200MHz
- BusFrequencyMultiplier
  - Speed up bus frequency and narrow by factor of N
    - e.g. N=2 multiply a 128 bus @200MHz to 64 bus @400MHz
- Modify the timing of the SSN bus
  - Use to absorb arbitrary amount of skew between CTS regions
    - Meet setup/hold timing
  - Modify the bus frequency at the chip-level IO
    - At input narrow and speed up internal bus
    - At output widen the bus and return to IO frequency



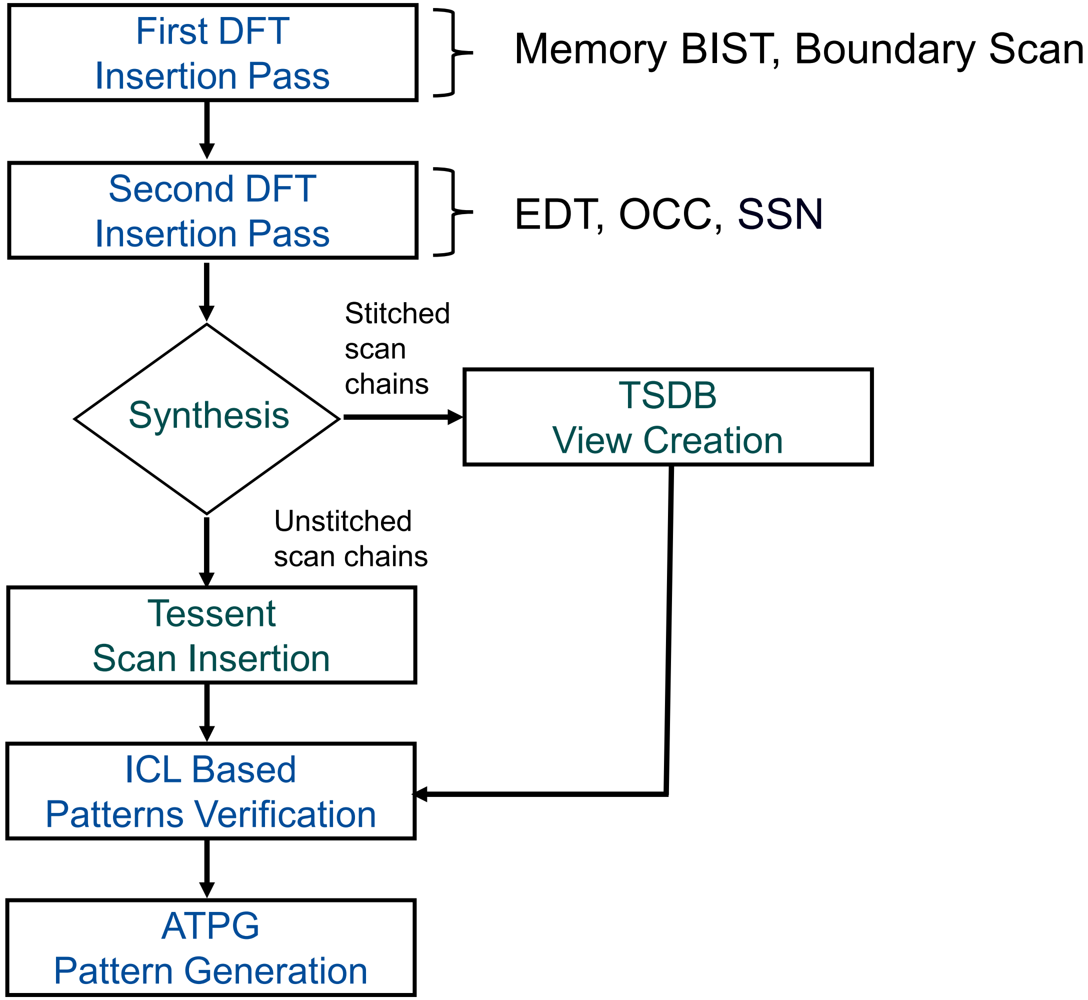


Advanced Topics
Managing timing of SSN datapath (2)

- OutputPipeline node
  - Optionally inserted SSN pipeline node
- Use this node to help meet timing
  - Minimize loop timing path between last node and IO
  - Contains persistent clock buffer
    - Instruct CTS to drive with early branch of clock
- Last node on datapath at top-level before IO
  - Dftspec semantic rule check
  - Not an ICL extraction error
  - Additional pipeline nodes to be added before



SSN Flow (Core Level)



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Backup 2

Backup 3