

ITC 2023 PO 2: BIST for Arm's 3nm Multi-Port Register Files

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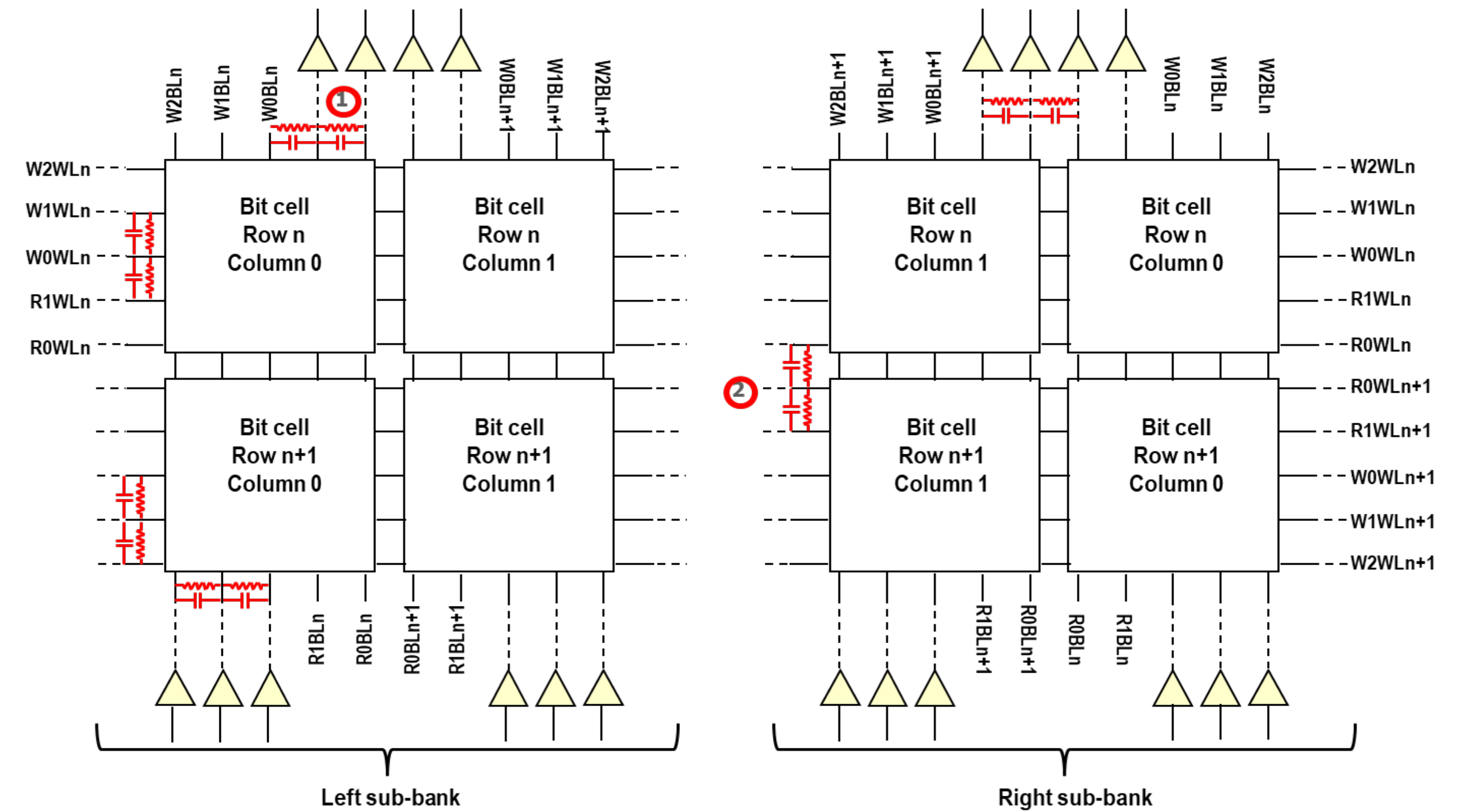
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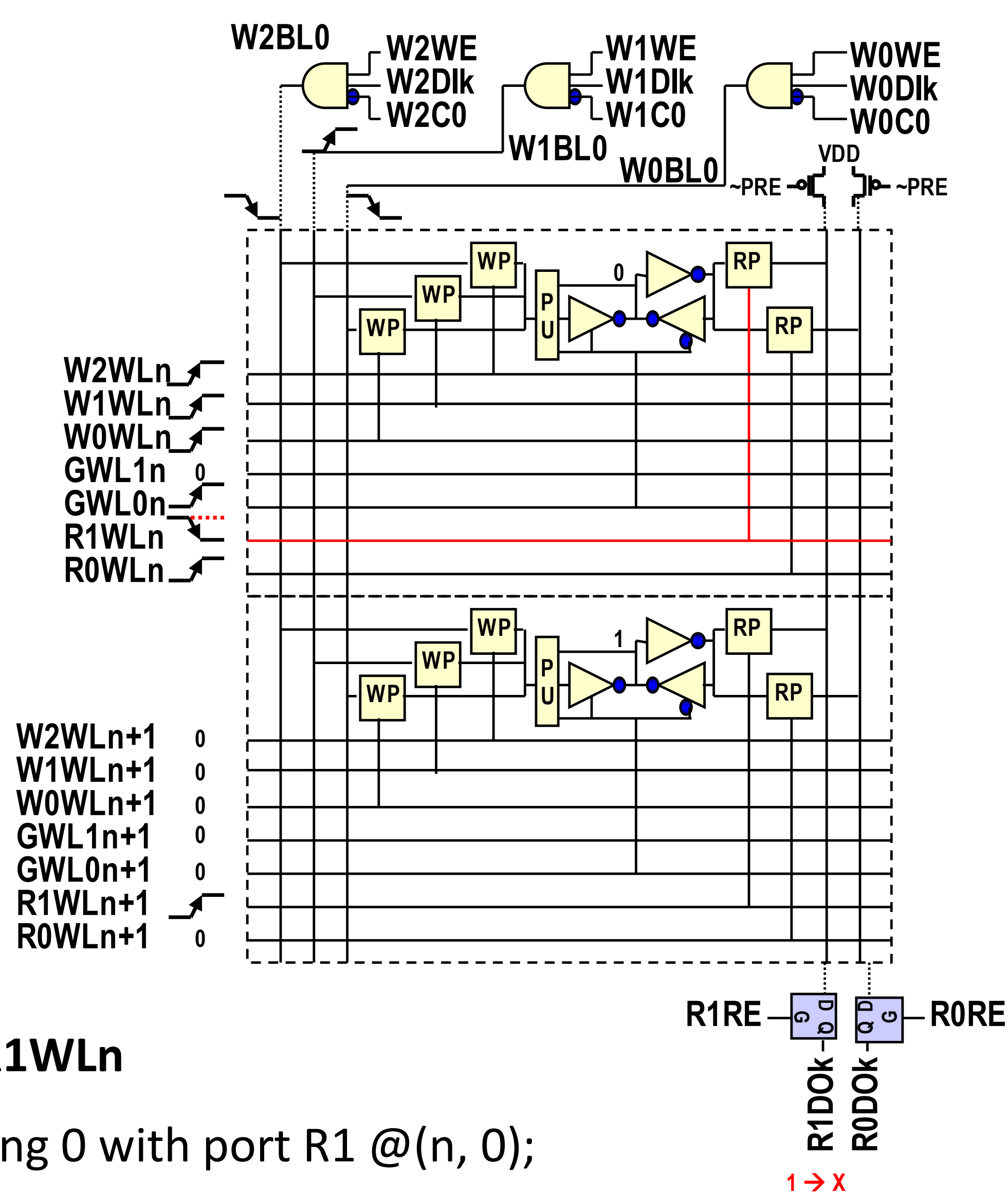
Test challenges of multi-port register files (MPRF)

1. The number of ports is large
2. Providing independent control and observation to each port requires a lot of circuitry
3. Coding test algorithms is very complex, especially considering coupling faults between word lines of different ports and coupling faults between bit lines of different ports
4. The number of possible test sequences grows rapidly with the number of ports and the number of aggressors considered, especially if the memory layout is not known

General architecture of MPRF



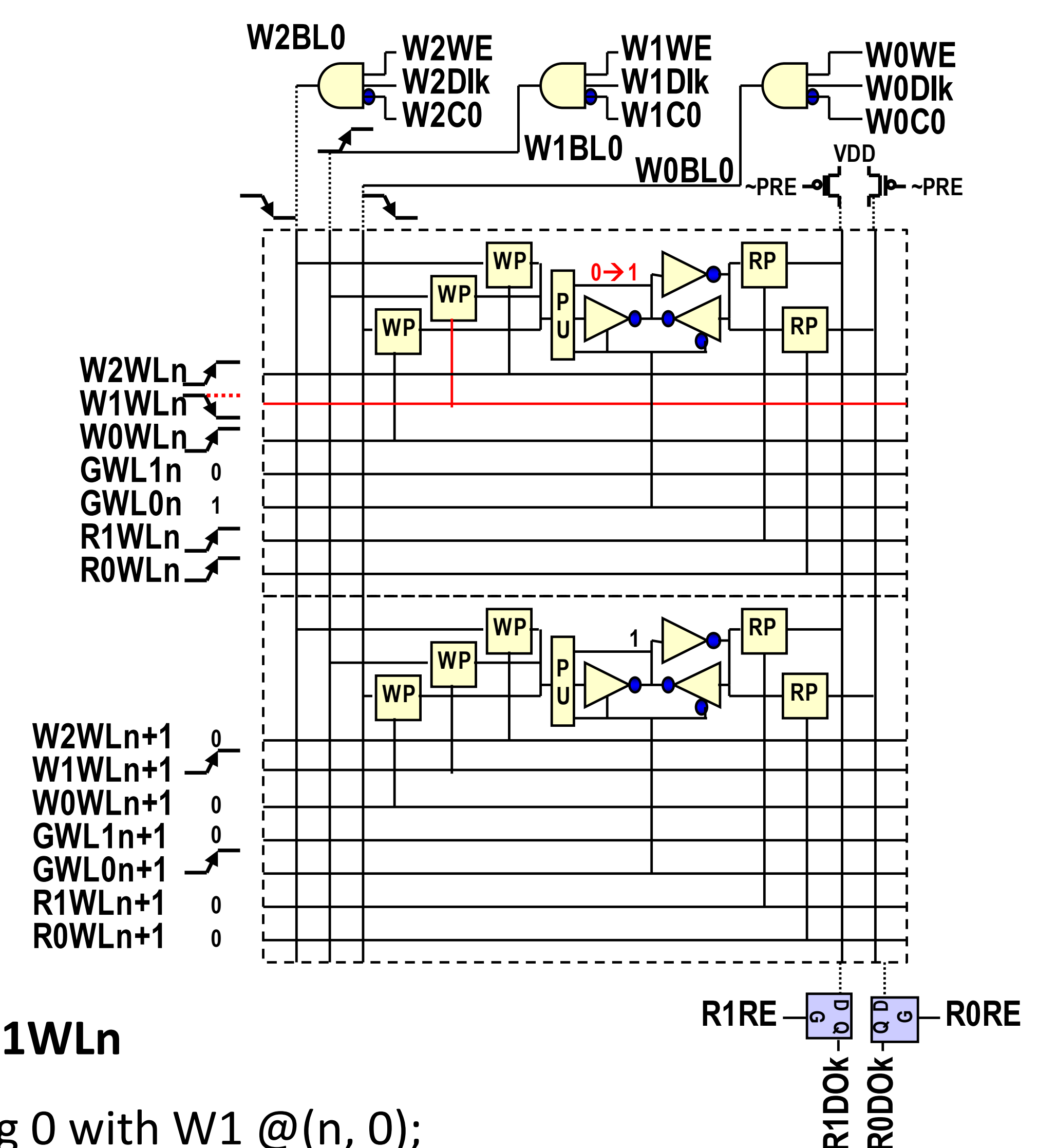
Detection of RWL coupling faults



Victim: R1WLn

- 1) reading 0 with port R1 @ (n, 0);
- 2) reading 1 with port R1 @ (n+1, 0) while writing 0 @ (n, 0) with all write ports and reading @ (n, 0) with all read ports except R1.

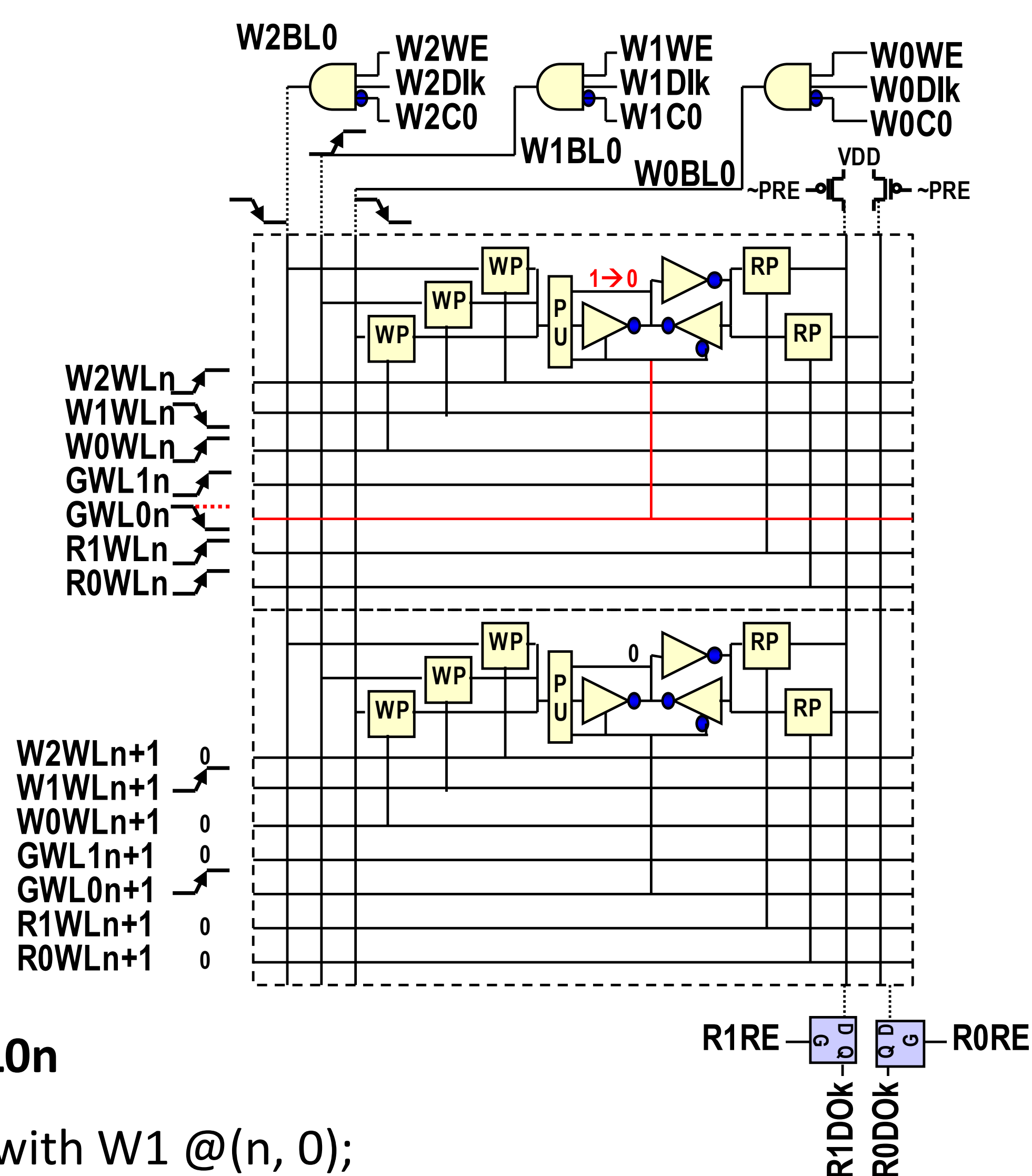
Detection of WWL coupling faults



Victim: W1WLn

- 1) writing 0 with W1 @ (n, 0);
- 2) writing 1 with W1 @ (n+1, 0) while writing 0 @ (n, 0) with all write ports except W1 and reading @ (n, 0) with all read ports;
- 3) reading 0 with the read port of the current test port @ (n, 0).

Detection of GWL coupling faults



Victim: GWL0n

- 1) writing 1 with W1 @ (n, 0);
- 2) writing 0 with W1 @ (n+1, 0) while writing 0 @ (n, 1) with all write ports except W1 and reading @ (n, 0) with all read ports;
- 3) reading 1 with the read port of the current test port @ (n, 0).

Detection of WBL coupling faults

Victim: W1BL0

- 1) writing 1 with W1 @ (n, 0).
- 2) writing 0 with W1 @ (n, 0) while writing 1 @ (n-1, 0) with all write ports except W1 and reading @ (n-1, 0) with all read ports.
- 3) reading 0 with the read port of the current test port @ (n, 0).

Detection of RBL coupling faults

The process is the same as the one used to detect RWL coupling faults.

Conclusion

Concurrent read and write operations performed in the same row - or even at the same address - allow testing for all possible combinations of two aggressors on a victim word line or bit line without increasing test time.