Tessent Hierarchical DFT

Meeting Time to Market, Cost, and Quality Challenges

For Multi-billion Transistor Designs

Saket Goyal

Master Engineer
ASIC Products Division

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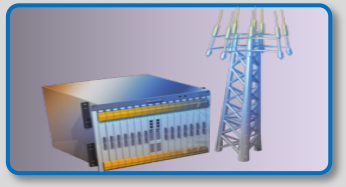
BROADCOM ASIC PRODUCTS DIVISION: Markets, Products

Markets	Products	Key Tech/IP Trends, Challenges
Wired Networking: Switching & Routing 	• 50GE/100GE/400GE Switches • 400G/800G Network Processors • 28G/56G/112G Switch Fabric	• 5nm, 3nm • 100G -> 200G SerDes • 3.2G+ HBM2E -> 6.4G+ HBM3
Compute Offload 	• ML Inference & Training • Video offload • Smart NIC • Security	• 5nm, 3nm • PCIe Gen5 -> PCIe Gen6 • More on-die, on-package memory • Power Density (W/mm2)
Wireless Infrastructure 	• Analog Front End, Digital Front End • Baseband Processor	• Integrated RF ADC-DAC • Thermal dissipation
Storage Controllers 	• Hard Disk Drive (HDD) Controllers • Solid State Drive (SSD) Controllers	• PCIe Gen6, SAS4 • Low-cost, low-power solution

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DFT - Trend and Challenges

Characteristics	Trend	DFT Challenges
Technology Scaling	• 5nm -> 3nm	• Defect Density, New type of defects, Faults/mm^2
IP Integration	• 100G -> 200G SerDes • PCIe Gen5 -> PCIe Gen6 • DDR5 -> DDR6 • 3.2G+ HBM2E -> 6.4G+ HBM3	• Concurrent IP & Design development • Integration, Coverage, and Verification
Packaging	• 2.5D -> 3D	• Known Good Die • Ability to test dies at 3DIC package
Low Power	• Lower Core Voltage • Low functional activity	• Multi Voltages • ATPG & Functional activity correlation
Product Design Cycles	• 12 -18 months -> 9-12 months	• Design Feedback to meet Test coverage • DFT Verification before Tape out
Ramp to Production	• 6 months -> 2 months	• Test Quality at Production
System Scaling	• Lifecycle Management, Embedded Analytics	• Re-use of DFT Infrastructure for In-system Test, Monitor, Diagnosis • Secure DFT Access

Broadcom and COPD Flow – DFT Perspective

Customer

- Integrate IPs in RTL
- Synthesis
- IP DFT Integration
- DFT Insertion
- ATPG – DRC & Coverage
- Physical Design

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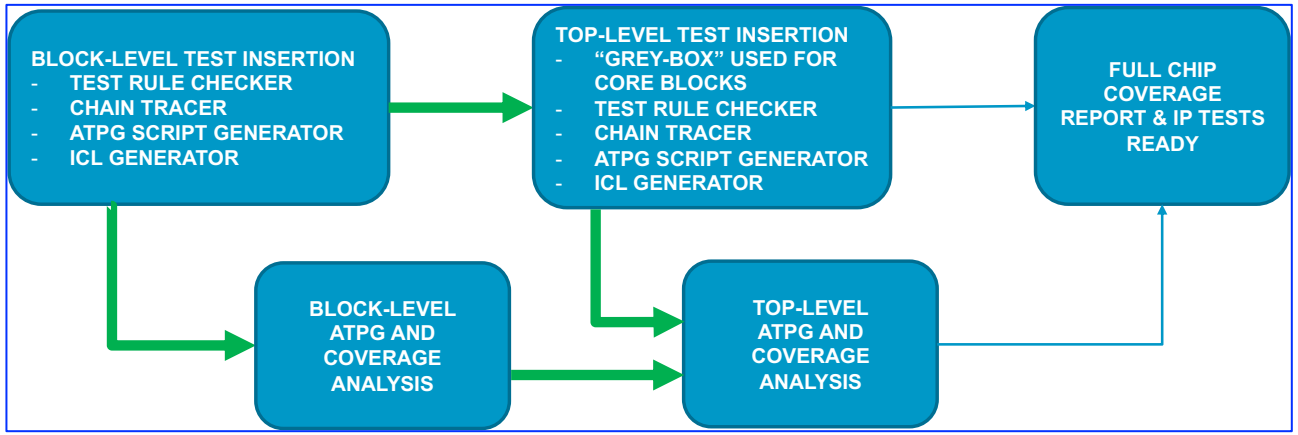
- Post-layout verification
- Test Rule Checker
- ATPG DRC & Coverage
- IP DFT Verification

ATE

- Test vectors development for Silicon Bring up

IP Hierarchical DFT Models

- **Plug-n-Play**
- **DFT Integration**
- **Re-targetable Test Vectors for ATE**

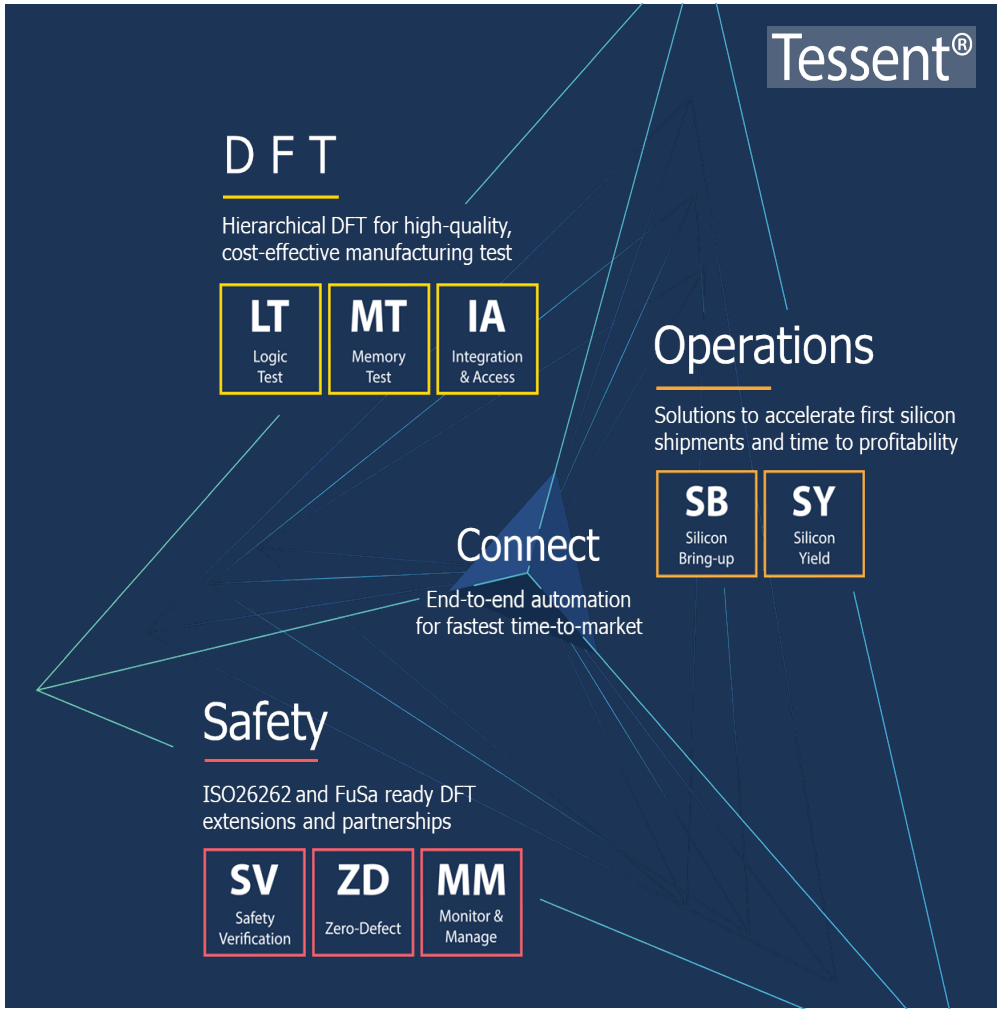


Broadcom Tessent Hierarchical DFT Flow

Tessent Hierarchical DFT Provides Plug-n-Play with High Predictability in Execution and Si Bring up

Broadcom Integrated Flow with Tessent Connect

- ✓ **Specification-based Hierarchical DFT for all IP**
- ✓ **IP Retargetable Pattern Generation**
- ✓ **IJTAG insertion, extraction and control for third-party and Tessent IPs**
- ✓ **Fully Integrated Tessent MBIST**
- ✓ **Integration of Mission Mode Controller for In-System Test**
- ✓ **Cell Aware ATPG**
- ✓ **Diagnosis Driven Yield Analysis**
- ✓ **Common database across the entire flow**
- ✓ **Flow customization with introspection and design editing**



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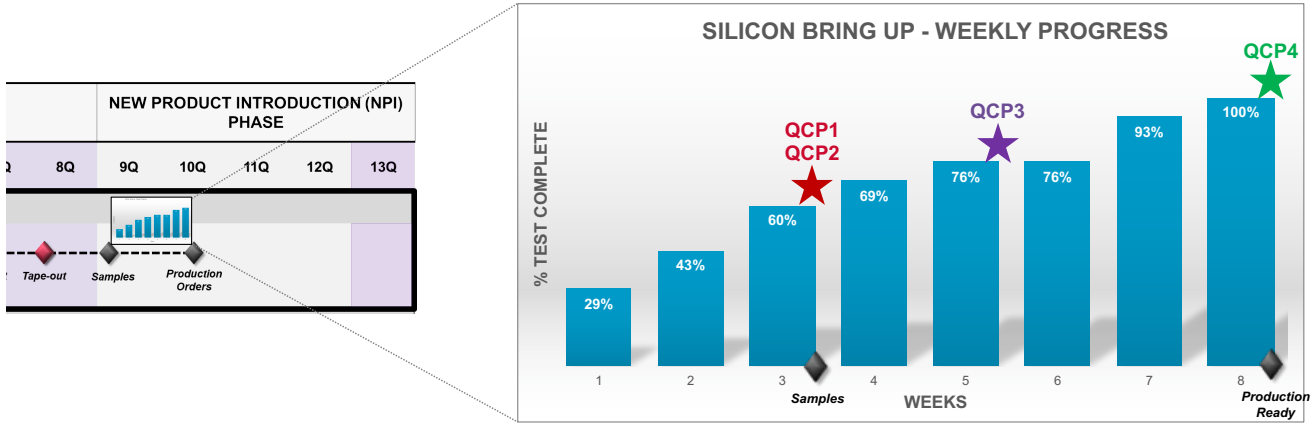
Tessent Hierarchical DFT Flow Benefits



- ✓ **Complete DFT Insertion with ATPG DRC and Coverage on whole design in 1 week**
- ✓ **<150G compute RAM required**
- ✓ **SSA → 1 to 2 days, TDF → 2 to 3 days, Cell Aware → 5 to 7 days**
- ✓ **Achieve High Test coverage achieved for Initial samples (SSA ~99.3%, TDF ~93%)**
- ✓ **High Test Coverages for IP**
- ✓ **Silicon debug & production readiness in ~8 weeks**
- ✓ **Minimal effort to support In-System Test deliverables**

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Summary

Increasing High Performance Computing application demands chip-makers to have **aggressive release timelines** for highly complex 2.5D SoCs

Advanced DFT Automation using **Tessent Connect** has enabled Broadcom to ship high quality prototypes and samples to production test readiness in ~2 months for ASIC and COPD customers

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Thank You


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