Tessent Hierarchical DFT
Meeting Time to Market, Cost, and Quality Challenges
For Multi-billion Transistor Designs

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# Broadcom ASIC Products Division: Markets, Products

<table>
<thead>
<tr>
<th>Markets</th>
<th>Products</th>
<th>Key Tech/IP Trends, Challenges</th>
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</thead>
</table>
| Wired Networking: Switching & Routing | • 50GE/100GE/400GE Switches  
• 400G/800G Network Processors  
• 28G/56G/112G Switch Fabric | • 5nm, 3nm  
• 100G -> 200G SerDes  
• 3.2G+ HBM2E -> 6.4G+ HBM3 |
| Compute Offload | • ML Inference & Training  
• Video offload  
• Smart NIC  
• Security | • 5nm, 3nm  
• PCIe Gen5 -> PCIe Gen6  
• More on-die, on-package memory  
• Power Density (W/mm²) |
| Wireless Infrastructure | • Analog Front End, Digital Front End  
• Baseband Processor | • Integrated RF ADC-DAC  
• Thermal dissipation |
| Storage Controllers | • Hard Disk Drive (HDD) Controllers  
• Solid State Drive (SSD) Controllers | • PCIe Gen6, SAS4  
• Low-cost, low-power solution |
## DFT - Trend and Challenges

<table>
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<tr>
<th>Characteristics</th>
<th>Trend</th>
<th>DFT Challenges</th>
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<tbody>
<tr>
<td><strong>Technology Scaling</strong></td>
<td>5nm -&gt; 3nm</td>
<td>Defect Density, New type of defects, Faults/mm^2</td>
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<tr>
<td><strong>IP Integration</strong></td>
<td>100G -&gt; 200G SerDes, PCIe Gen5 -&gt; PCIe Gen6, DDR5 -&gt; DDR6, 3.2G+ HBM2E -&gt; 6.4G+ HBM3</td>
<td>Concurrent IP &amp; Design development, Integration, Coverage, and Verification</td>
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<td><strong>Packaging</strong></td>
<td>2.5D -&gt; 3D</td>
<td>Known Good Die, Ability to test dies at 3DIC package</td>
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<td><strong>Low Power</strong></td>
<td>Lower Core Voltage, Low functional activity</td>
<td>Multi Voltages, ATPG &amp; Functional activity correlation</td>
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<td><strong>Product Design Cycles</strong></td>
<td>12 - 18 months -&gt; 9-12 months</td>
<td>Design Feedback to meet Test coverage, DFT Verification before Tape out</td>
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<td><strong>Ramp to Production</strong></td>
<td>6 months -&gt; 2 months</td>
<td>Test Quality at Production</td>
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<td><strong>System Scaling</strong></td>
<td>Lifecycle Management, Embedded Analytics</td>
<td>Re-use of DFT Infrastructure for In-system Test, Monitor, Diagnosis, Secure DFT Access</td>
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Broadcom and COPD Flow – DFT Perspective

**Customer**
- Integrate IPs in RTL
- Synthesis
- IP DFT Integration
- DFT Insertion
- ATPG – DRC & Coverage
- Physical Design

**Broadcom**
- Post-layout verification
- Test Rule Checker
- ATPG DRC & Coverage
- IP DFT Verification

**ATE**
- Test vectors development for Silicon Bring up

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**Broadcom Tessent Hierarchical DFT Flow**

**IP Hierarchical DFT Models**
- Plug-n-Play
- DFT Integration
- Re-targetable Test Vectors for ATE

**Tessent Hierarchical DFT Provides Plug-n-Play with High Predictability in Execution and Si Bring up**
Broadcom Integrated Flow with Tessent Connect

- Specification-based Hierarchical DFT for all IP
- IP Retargetable Pattern Generation
- IJTAG insertion, extraction and control for third-party and Tessent IPs
- Fully Integrated Tessent MBIST
- Integration of Mission Mode Controller for In-System Test
- Cell Aware ATPG
- Diagnosis Driven Yield Analysis
- Common database across the entire flow
- Flow customization with introspection and design editing
Complete DFT Insertion with ATPG DRC and Coverage on whole design in 1 week

<150G compute RAM required

SSA → 1 to 2 days, TDF → 2 to 3 days, Cell Aware → 5 to 7 days

Achieve High Test coverage achieved for Initial samples (SSA ~99.3%, TDF ~93%)

High Test Coverages for IP

Silicon debug & production readiness in ~8 weeks

Minimal effort to support In-System Test deliverables
Increasing High Performance Computing application demands chip-makers to have aggressive release timelines for highly complex 2.5D SoCs.

Advanced DFT Automation using **Tessent Connect** has enabled Broadcom to ship high quality prototypes and samples to production test readiness in ~2 months for ASIC and COPD customers.
Thank You