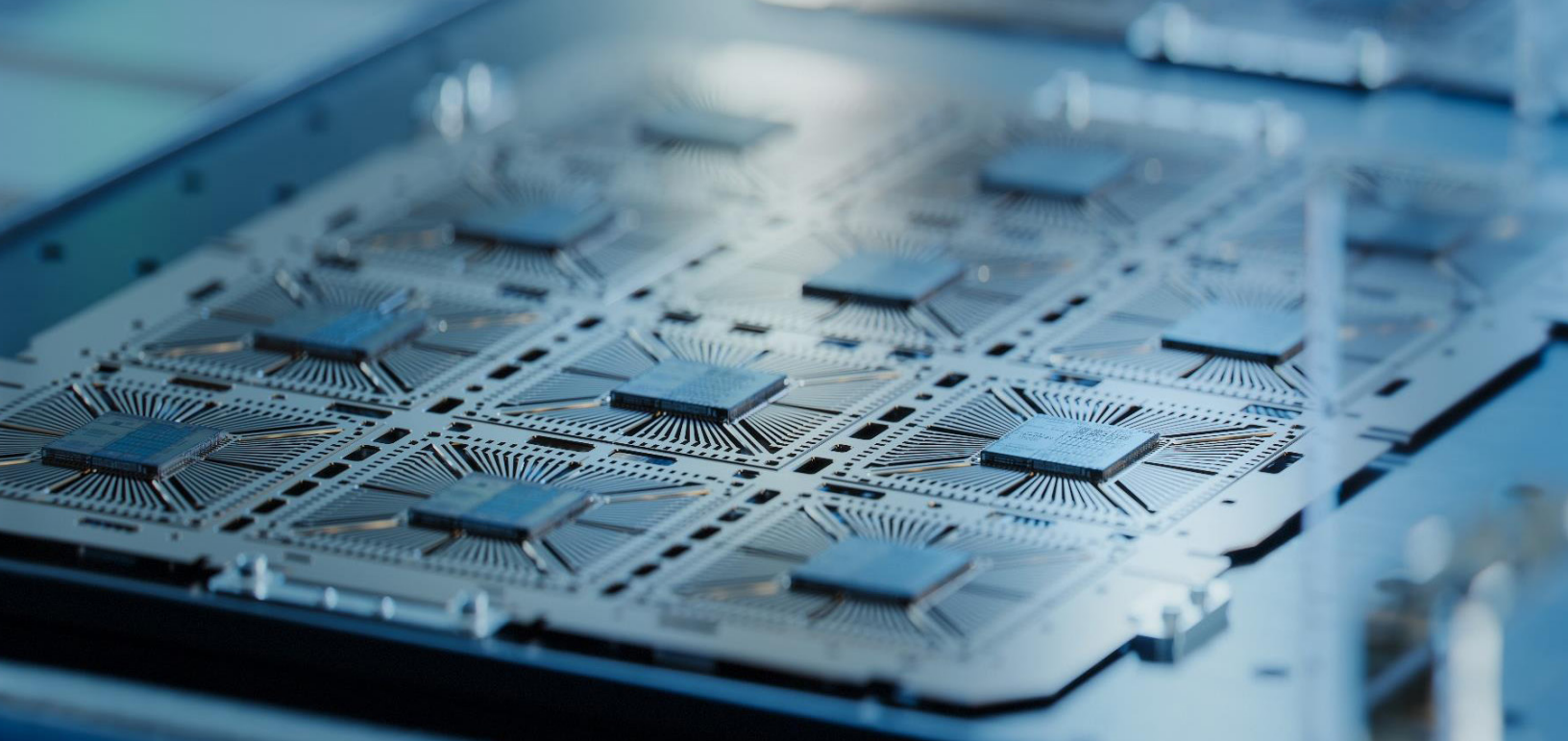




DIGITAL INDUSTRIES SOFTWARE

Solido Layout Analyzer

AI-powered measurement-aware analysis for parasitics and layout effects

Benefits

Generative and Agentic AI

- Fully integrated Solido Fuse makes setting up, running, and debugging jobs intuitive using natural language prompts

Comprehensive parasitic effects coverage across multiple analysis flows

- Investigates parasitics interactively
- Checks device placements and LDE effects
- Interacts with schematic and layout
- Runs both static and dynamic simulation-in-loop analyses

Faster debug in fewer iterations

- What-if analysis for updated layout constraints
- Gain insights into better parasitic estimation

Introduction

Post-layout results frequently diverge from pre-layout simulations, a challenge exacerbated by the exponential growth of layout effects and parasitic elements in advanced nodes. Investigating post-layout failures and performance degradation is a time-consuming process that can lead to production delays.

Solido Layout Analyzer provides a comprehensive solution for understanding and resolving these complex issues. The tool delivers wide-ranging insights into parasitics and layout-dependent effects (LDEs) through both static and dynamic analyses, enabling the identification, understanding, and resolution of these challenges before they escalate into production delays. Integration with Solido Fuse further speeds up layout debugging workflows by utilizing generative and agentic AI to accelerate tool ramp up, workflow setup, results analysis, and report generation. Workflows are further streamlined by Layout Analyzer's tight integration between schematic and layout, which makes it easy and straight-forward to incorporate analyses feedback into both design and layout cycles. It is integrated with Siemens' S-Edit and L-Edit, in addition to 3rd party environments.

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Benefits *continued*

- Precise identification of largest LDE sources post-layout

Advanced capacity and performance

- Handles large DSPF files
- Real-time insights with schematic and layout cross-probing
- Low memory footprint

Easy to use and deploy

- Intuitive GUI for interactive design and analysis or streamlined command line interface
- Works with all process technologies
- Integrates with leading simulation environments
- Works with all parasitic extraction tools

Layout Analyzer's comprehensive, measurement-aware analyses offer precise identification of the largest LDE sources and improved parasitic estimation—ensuring critical post-layout refinements meet design goals and specifications—while accelerating debug, reducing iteration cycles and saving design time.

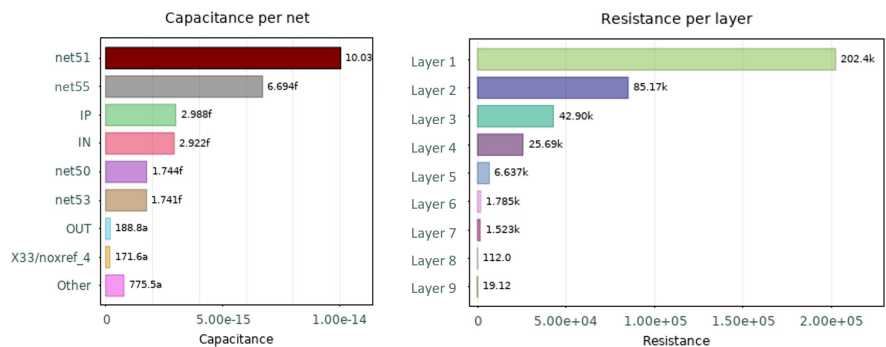
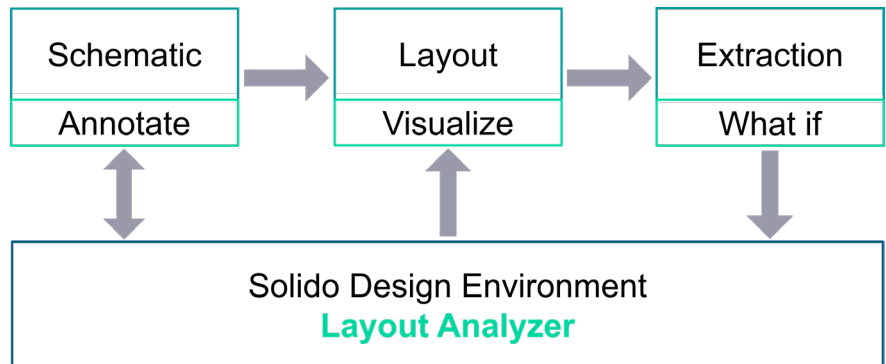


Figure 1 and 2: Results from Explore Parasitics flow summarizing resistance and capacitance data.

Solido Layout Analyzer specifications

Simulator support

- Full integration with Solido Simulation Suite
- Supports most 3rd party commercial and in-house SPICE simulators

Cloud readiness

- Cloud-ready and optimized
- Partner with major cloud platforms

Grid computing support

- Supports leading computing cluster management platforms

Key flows in Solido Layout Analyzer:

- Solido Fuse:** Fully integrated generative and agentic AI capabilities that boost engineering productivity, accelerate production schedules, and bridge the talent gap. Solido Fuse for Layout Analyzer can answer questions, make tool recommendations, summarize and debug logs, generate job reports and analyze results from parasitics exploration.
- Explore Parasitics:** Provides intuitive, efficient exploration and visualization of parasitics, allowing the user to understand where the parasitics are and how to fix them. DSPF files are analyzed in a streamlined display table that's easy to read, filter and sort, providing P2P and timing data for all net paths in the design and guidance on which nets may be of interest for further analysis and debugging. Detailed resistance and capacitance analyses enable quick insights into design features like symmetry, routing, coupling, etc.
- Explore LDEs:** Enables a better understanding of Layout Dependent Effects (LDEs) between pre- and post-layout that cause spec failures. Simulation-in-the-loop analysis provides the ability to investigate the variation in operating points and compare the operating points between pre- vs. post-layout and post- vs. post-layout.

Solido Layout Analyzer specifications

continued

Operating platform support

- Arm
- x86

Operating systems

- Linux®

- **Impacts on Outputs:** AI-powered sensitivity analysis that varies resistances and capacitances to determine cause-and-effect between parasitics and design goals. Can be used to identify sensitive nets for further investigation in static exploration. Choose to explore which outputs were most affected by a selected net, or which nets had the greatest impact on a select measurement.
- **Experiments:** Explore different layout scenarios independently, prior to implementing the optimal solution. Able to set up unlimited “What if?” scenarios modifying Rs, CCs, and/or GCs to uncover potential ways to improve design performance or directly investigate parasitics effects on any net in the design.

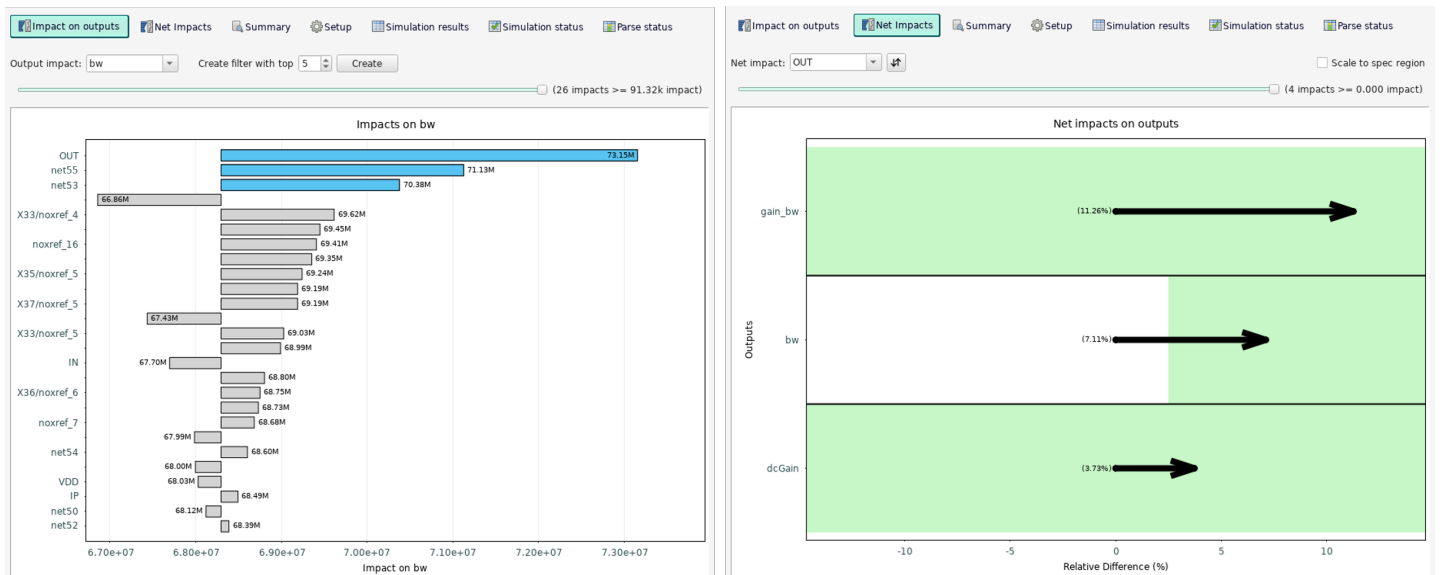


Figure 3: Impacts on Outputs interface showing which nets have a significant impact on a selected output, and the direction of impact a specific net has on all the measures to visualize trade-offs

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