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Horizon Robotics

Journey 5, from Horizon Robotics the 1st ISO 26262 certified ASIL-B AI chip in China

SH SOC Platform- Victor Wang

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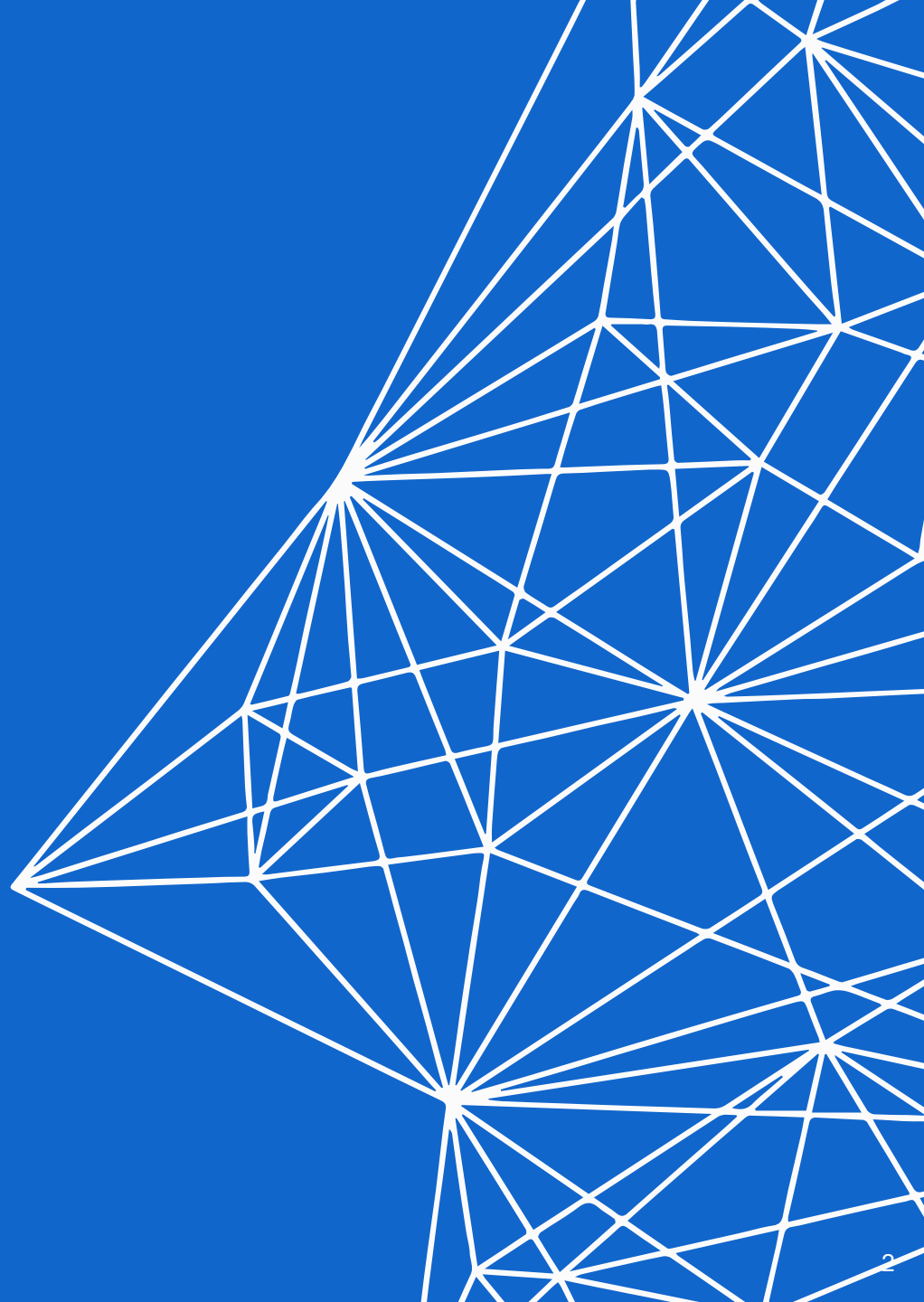


J5 SOC introduction

The third-generation automotive-grade AI processor of Horizon Robotic

- The first AI chip in China certified to have met ISO 26262 ASIL-B functional safety standards.

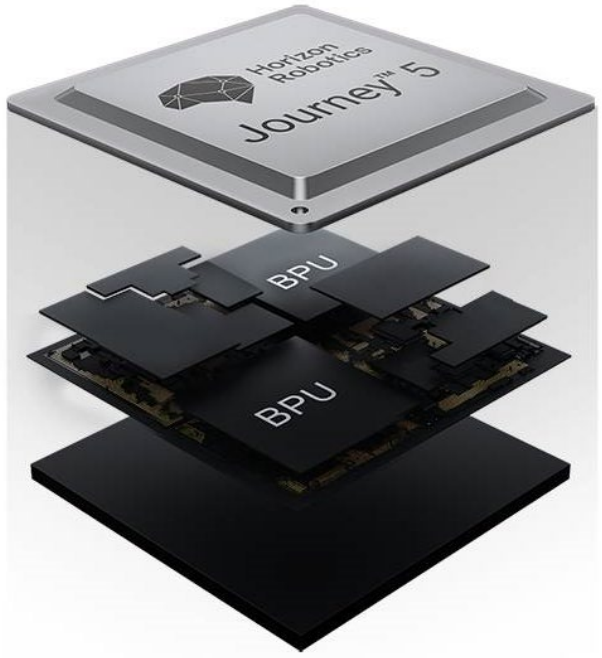
Based on the latest horizon BPU ® Bayesian architecture design

- Features up to 128 TOPS (Trillion Operations Per Second) processing capabilities for a single processor,
- One of the most powerful in the world, supporting neural computing from 16 sensors.

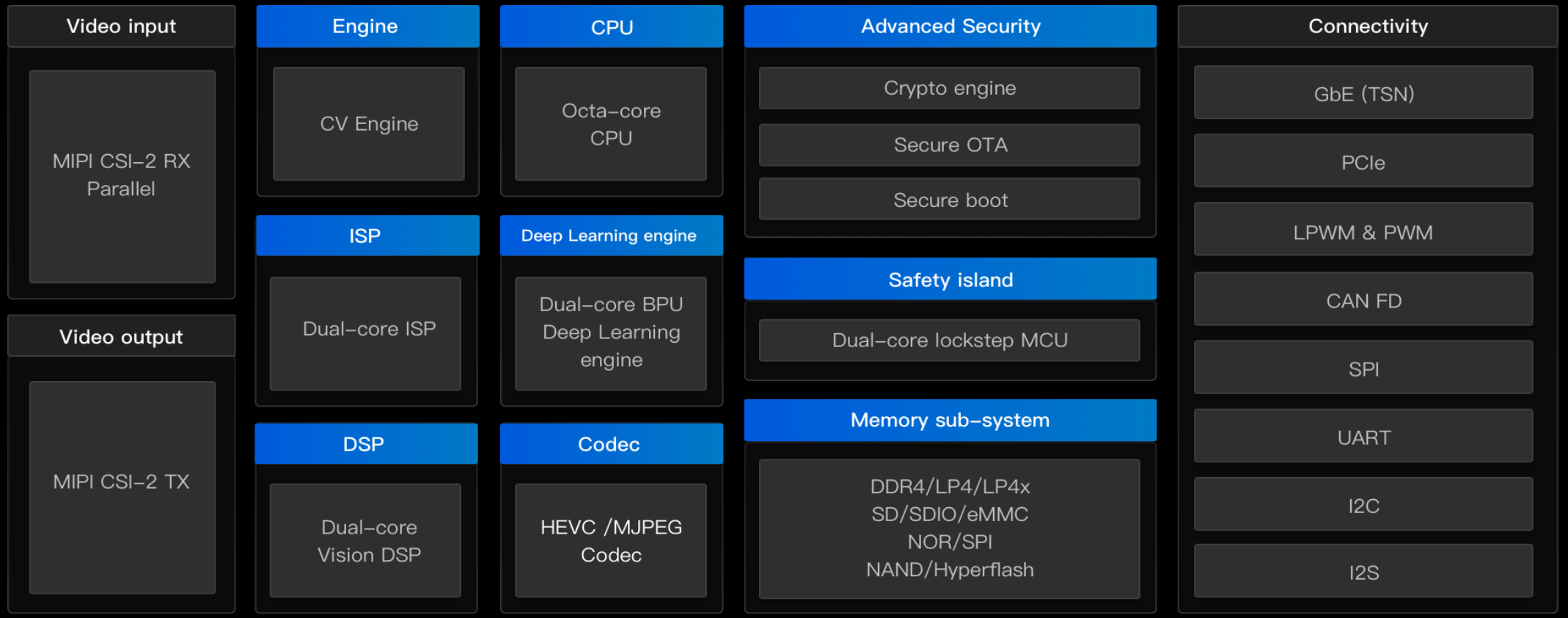
Relying on rich and diverse computing

- J5 is applicable to the acceleration of the most advanced image sensing algorithm
- Also supports multi-sensor fusion such as laser radar and millimeter wave radar, as well as prediction planning and H.265/JPEG real-time coding and decoding.

An ideal product for high-level automatic pilot and intelligent cockpit.



J5 SOC Implementation

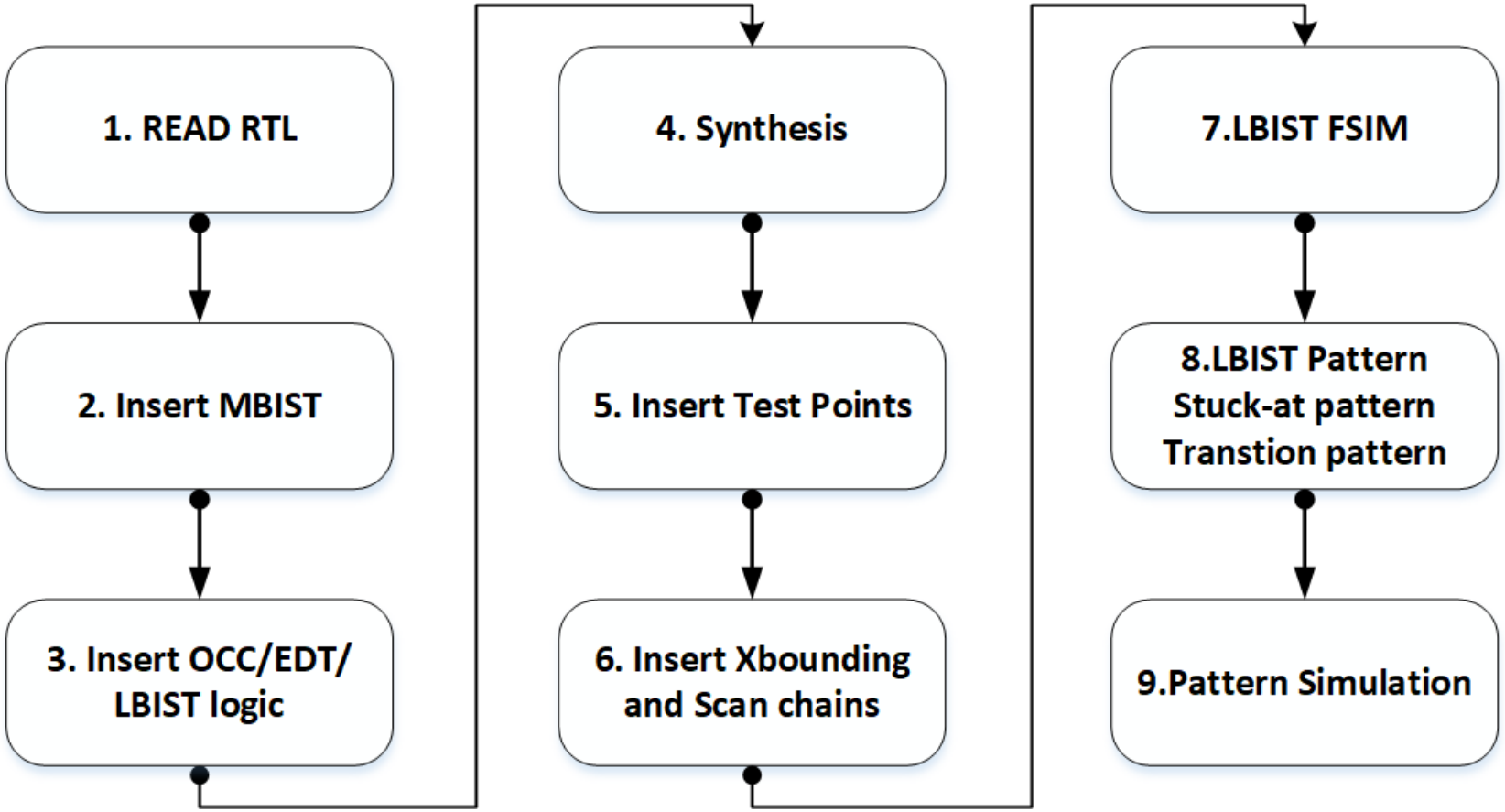


- TSMC 16nm FinFET
- 27×27mm HFCBGA
- AEC-Q100 Grade 2
- ASIL-B

POST for random & latent faults - MissionMode DMA architecture for BIST operation
IST periodic testing - MissionMode CPU-based architecture

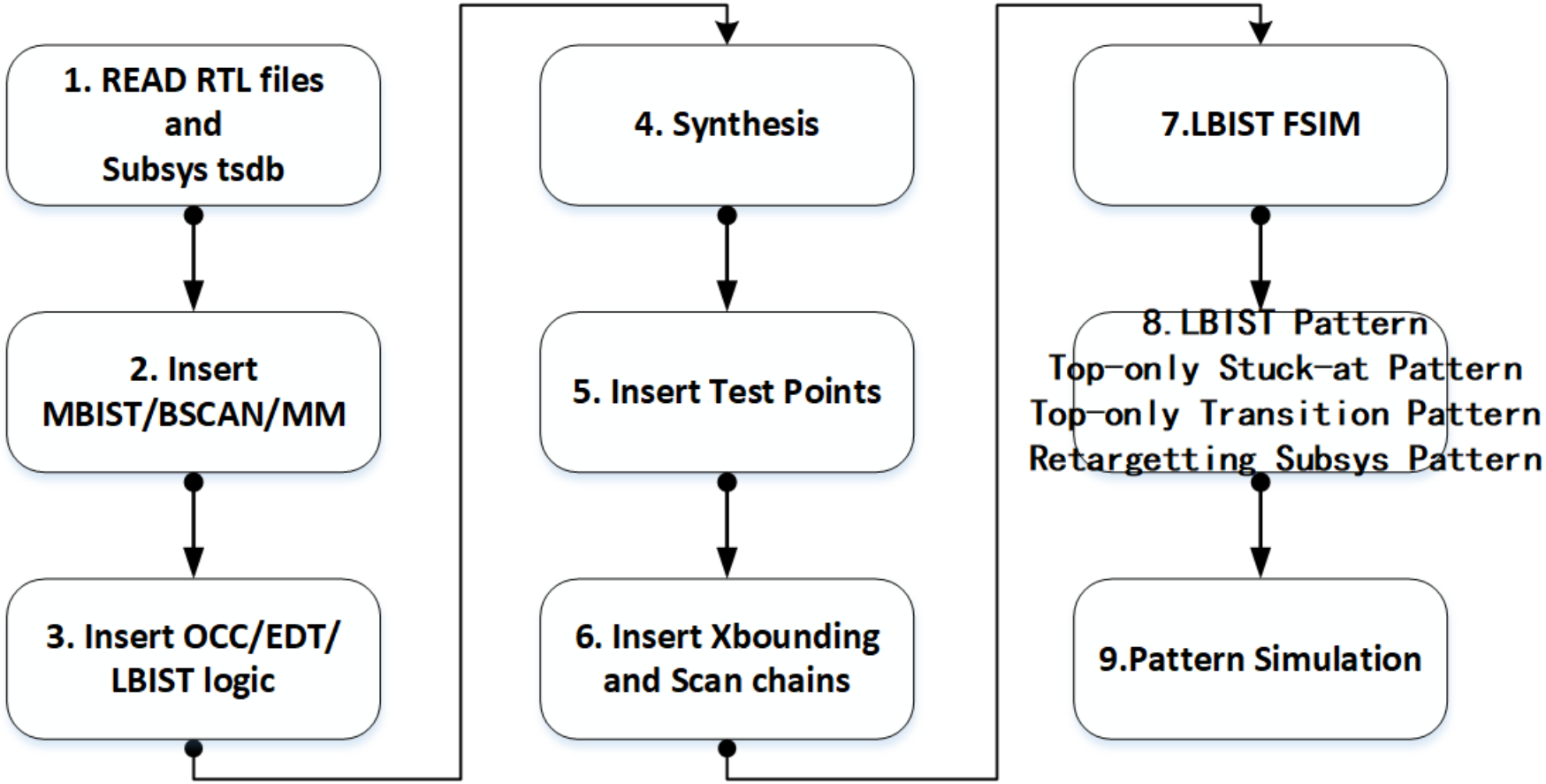
J5 DFT flow – block level

J5 use Siemens EDA tool -Tessent DFT products to implement DFT insertion to reach ISO26262 ASIL-B level, The DFT flow is shown below:



J5 DFT flow – top level

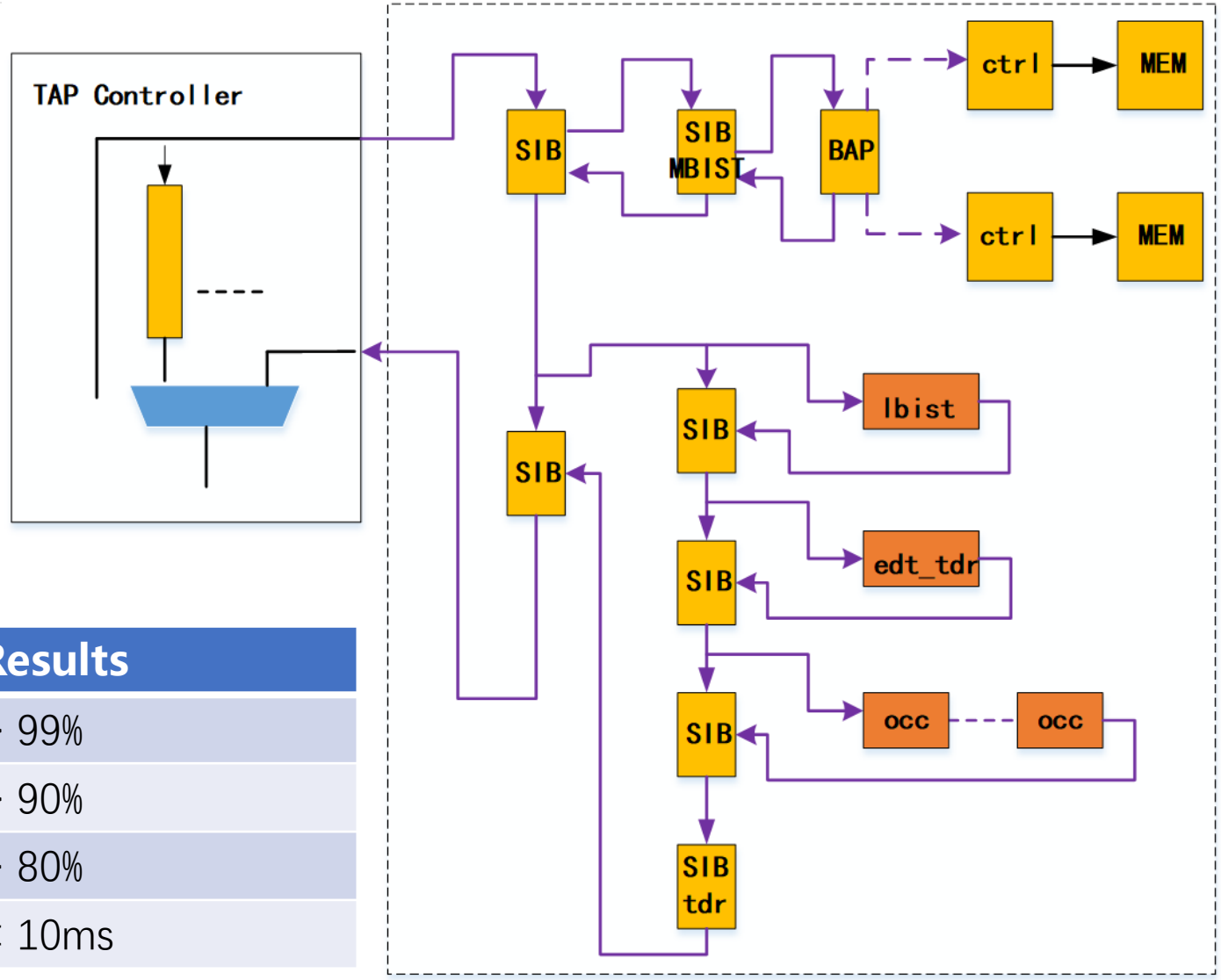
J5 use Siemens EDA tool -Tessent DFT products to implement DFT insertion to reach ISO26262 ASIL-B level, The DFT flow is shown below:



J5 DFT Implementation

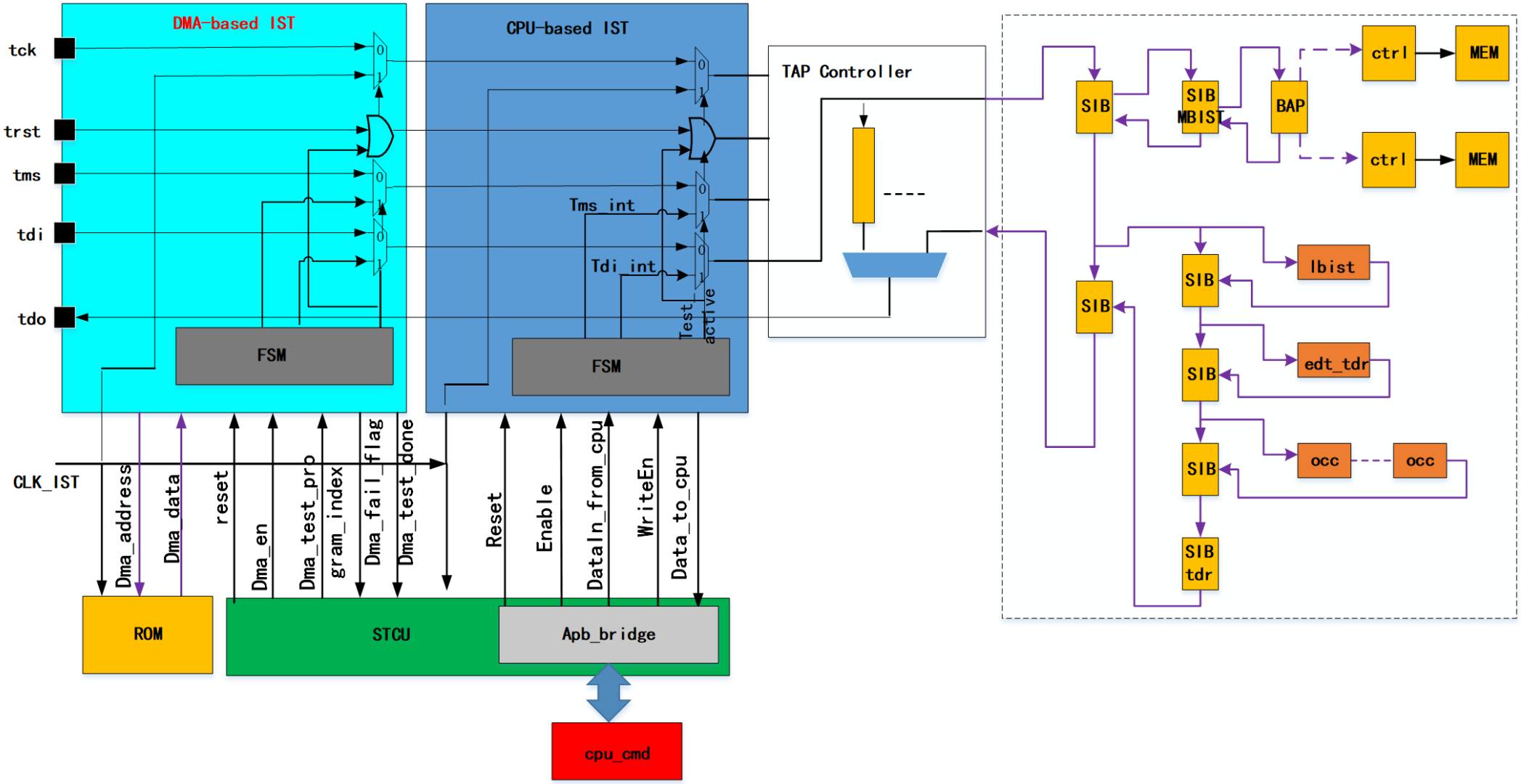
In J5, IEEE1687 IJTAG network is employed to implement the sub-sys/block level DFT configuration and enable/disable the related MBIST/LBIST/Scan test easily.

DFT Hierarchy View
Top + 10 sub-sys levels
Gate count is more than 0.5 Billion in total



	Requirements	Results
DC Coverage	> 99%	> 99%
AC Coverage	> 85%	> 90%
LBIST Coverage	> 60%	> 80%
POST Time	< 15ms	< 10ms

J5 DFT DMA and CPU-based IST architecture

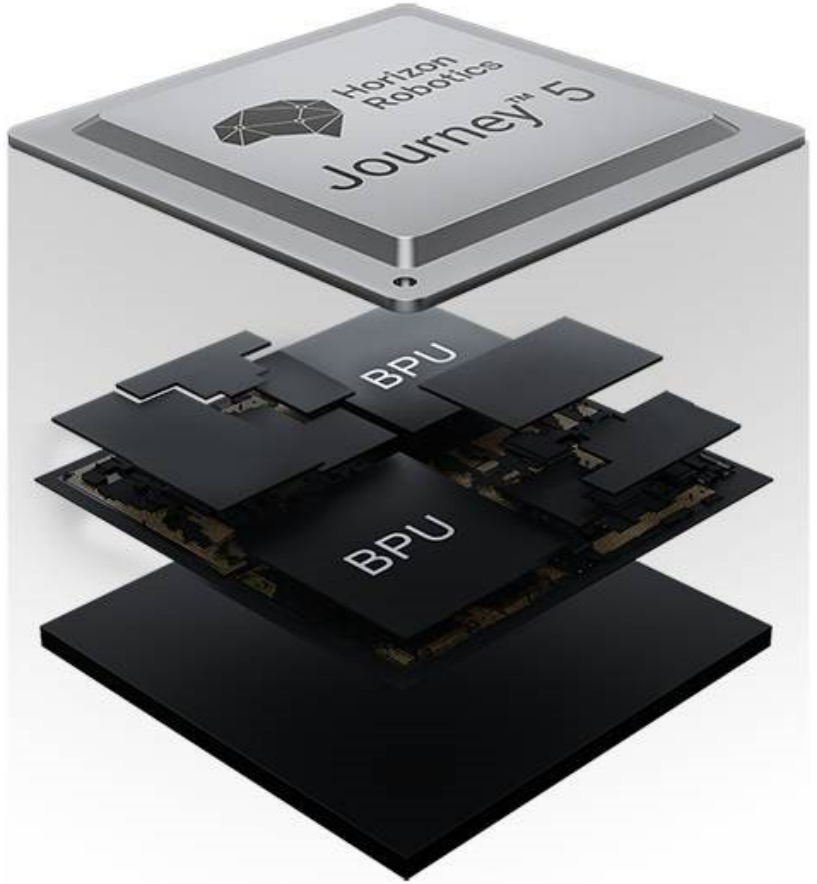


Summary

1. Siemens Tessent DFT flow makes the DFT insertion easily for Soc design
2. Siemens Tessent DFT flow makes the DFT integration efficiently for more IP integration when IJTAG network is employed
3. Siemens Tessent hierarchical-DFT flow accelerates DFT ATPG pattern generation and reduce the ATPG time at least 2X~4X times for bigger Soc design
4. Siemens Tessent In-System-test architecture makes Soc design work in-field testing for ISO 26262 ASIL requirement.
5. Siemens Tessent DFT flow provides the method to verify and validate the pattern quality for ATE TEST and in-field TEST

THANK YOU!

J5 SOC with BPU core



J5 DFT test in function mode

In function mode, We need run BIST at power-on-power-off phase to check the circuitry for random or latent faults . Tessent MissionMode provides the direct memory access (DMA) DFT architecture to make it

In function mode, We use CPU-based architecture for in-System-test to implement the periodic testing