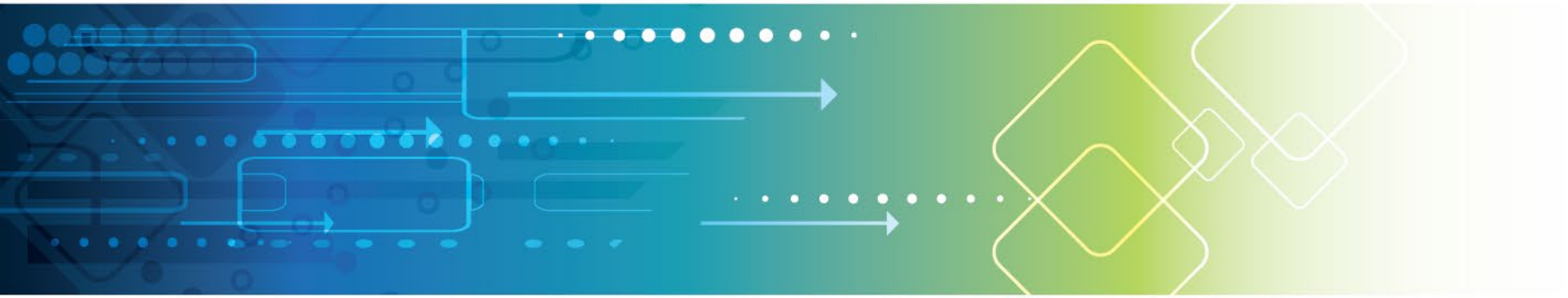
TERADYNE

# Teradyne enabling Siemens SSN



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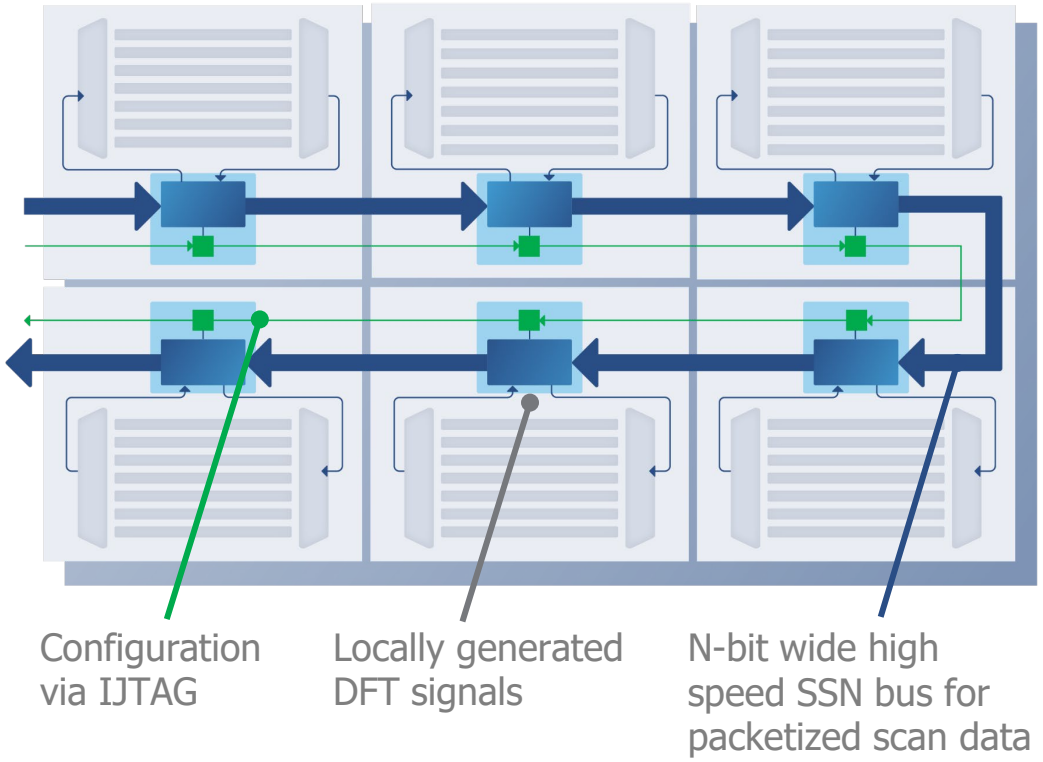


- Several Customers have implemented SSN into their designs
- SSN approach has several new capabilities
- New capabilities create test requirements for both SSN and ATE that need to be solved
- Goal of the presentation is to review requirements we have seen as of today



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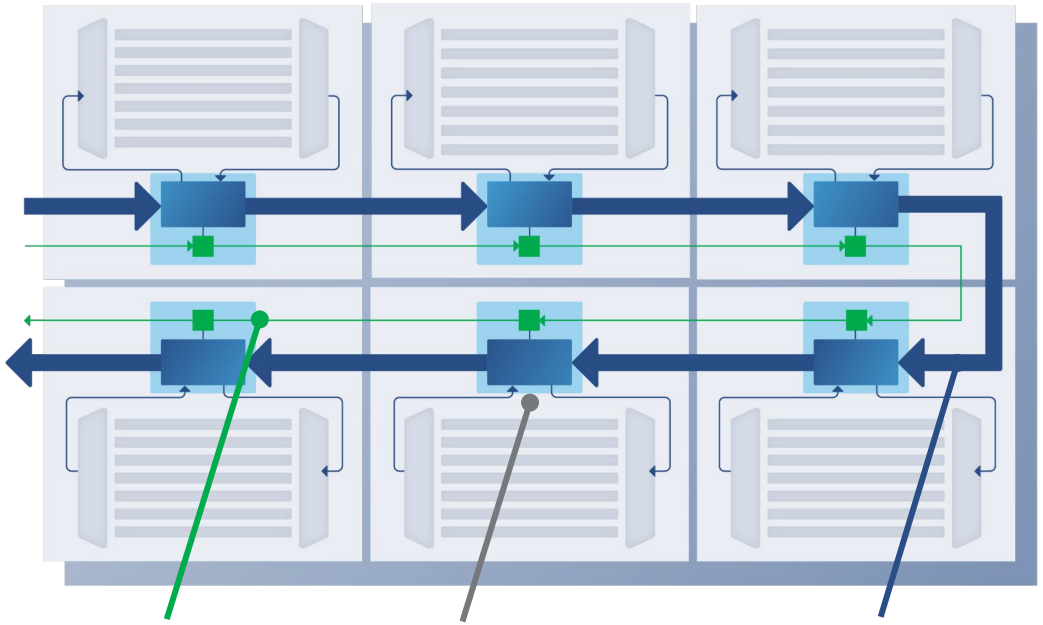
# Teradyne enabling Siemens SSN – Use Cases




| Use Cases |
| --- |
| **SSN Tester Compare with a Single Core**<br>The most basic case |
| **SSN Tester Compare with Multiple Unique Cores**<br>Requires binning by core and core masking |
| **SSN On-Chip Compare for Multiple Identical Cores**<br>Requires binning by core and core selecting for diagnosis |
| **(+) IEEE 1149.10**<br>Requires PEDDA initialization, KeepAlive, etc |
| **(+) DDR high-speed IO for SSN** |

Will discuss in this presentation



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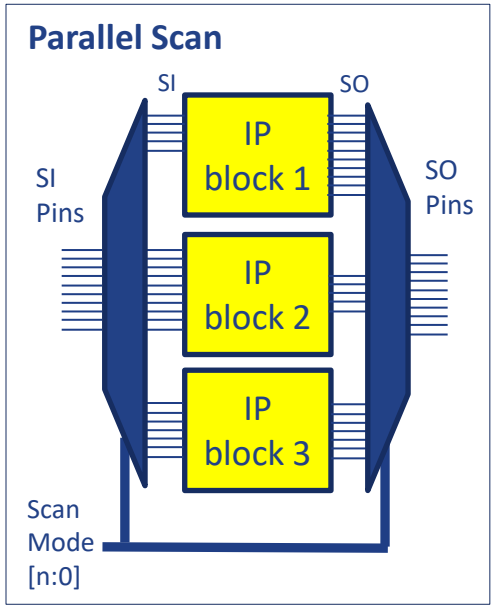
# Teradyne enabling Siemens SSN

## - Tester Compare with multiple cores




- Many external pins (32 – 128+ chains)
- 1:1 external to internal resource mapping during burst

Each ext pin will have data from multiple Blocks/Cores

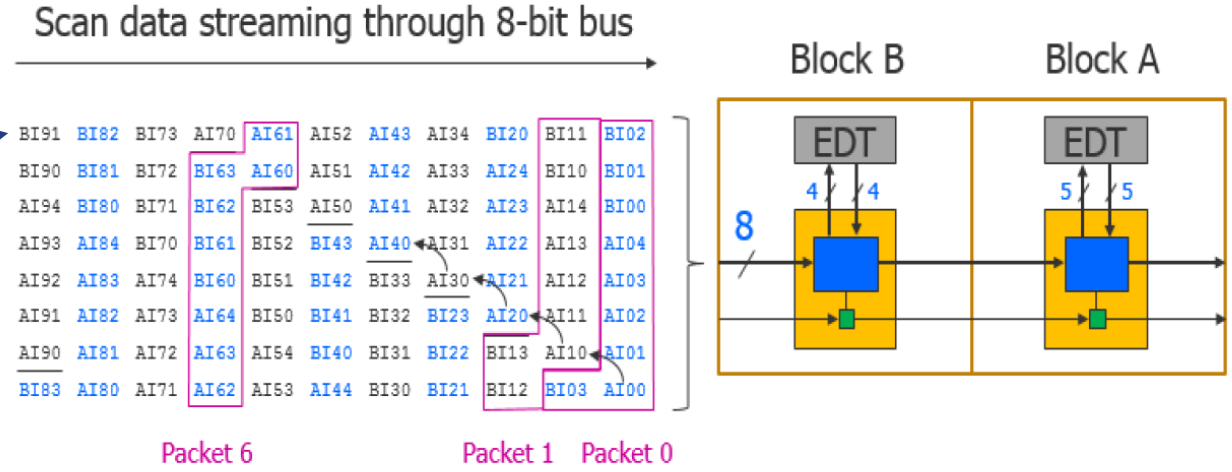



Fig. 2: Streaming scan packets

- Less pins, but data muxed on external pins
- Identify fail-per-core (quickly!)
- Reburst with core(s) masking (efficiently!)
- Debug/characterization with per-core info

Requires system, hardware, and software optimizations to be multisite production test time efficient!



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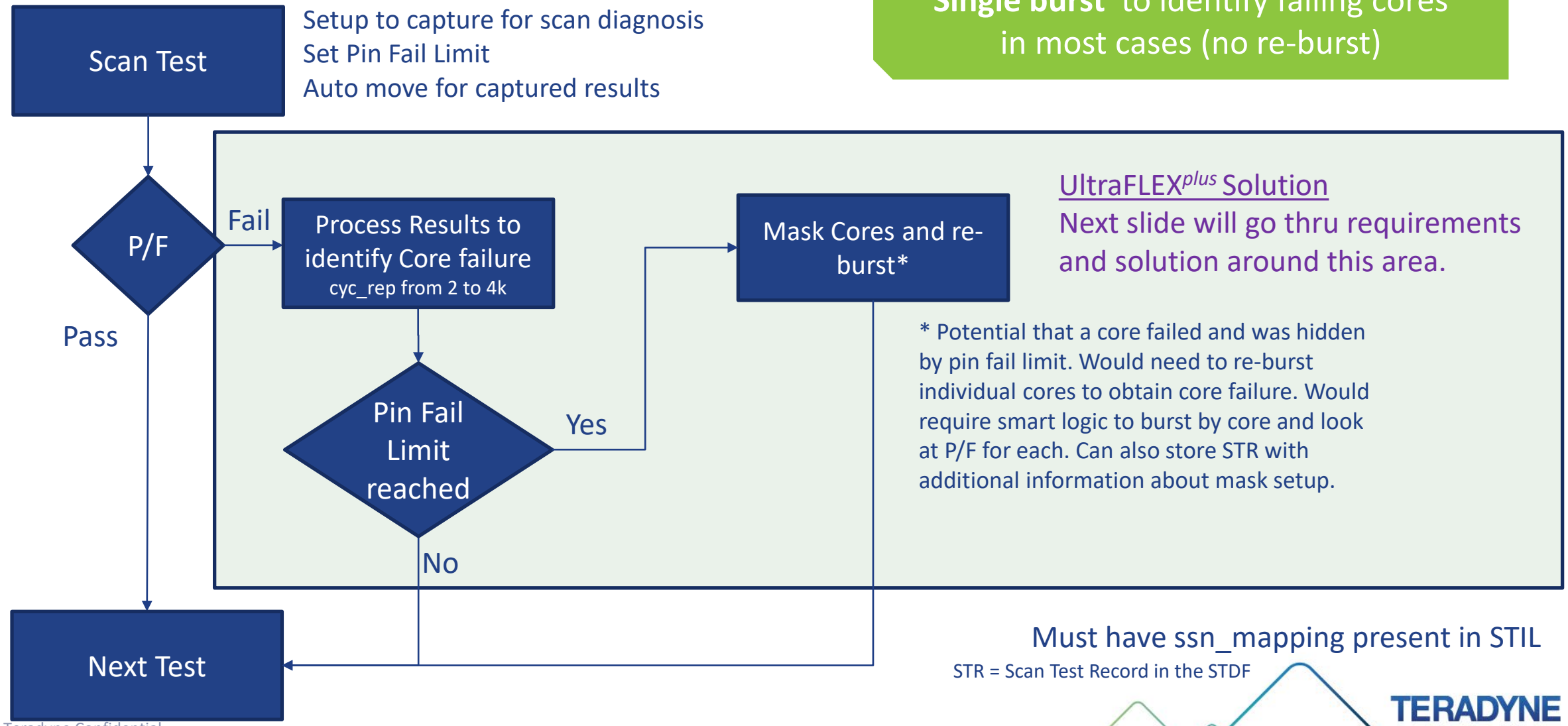
## - Tester Compare with multiple cores

**Single burst** to identify failing cores in most cases (no re-burst)




UltraFLEX*plus* Solution

Next slide will go thru requirements and solution around this area.

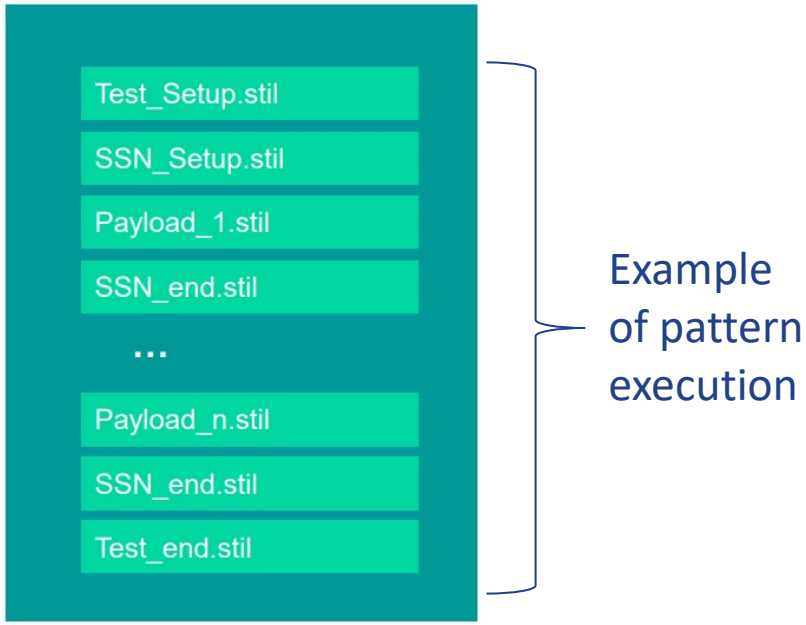
* Potential that a core failed and was hidden by pin fail limit. Would need to re-burst individual cores to obtain core failure. Would require smart logic to burst by core and look at P/F for each. Can also store STR with additional information about mask setup.

Must have ssn_mapping present in STIL

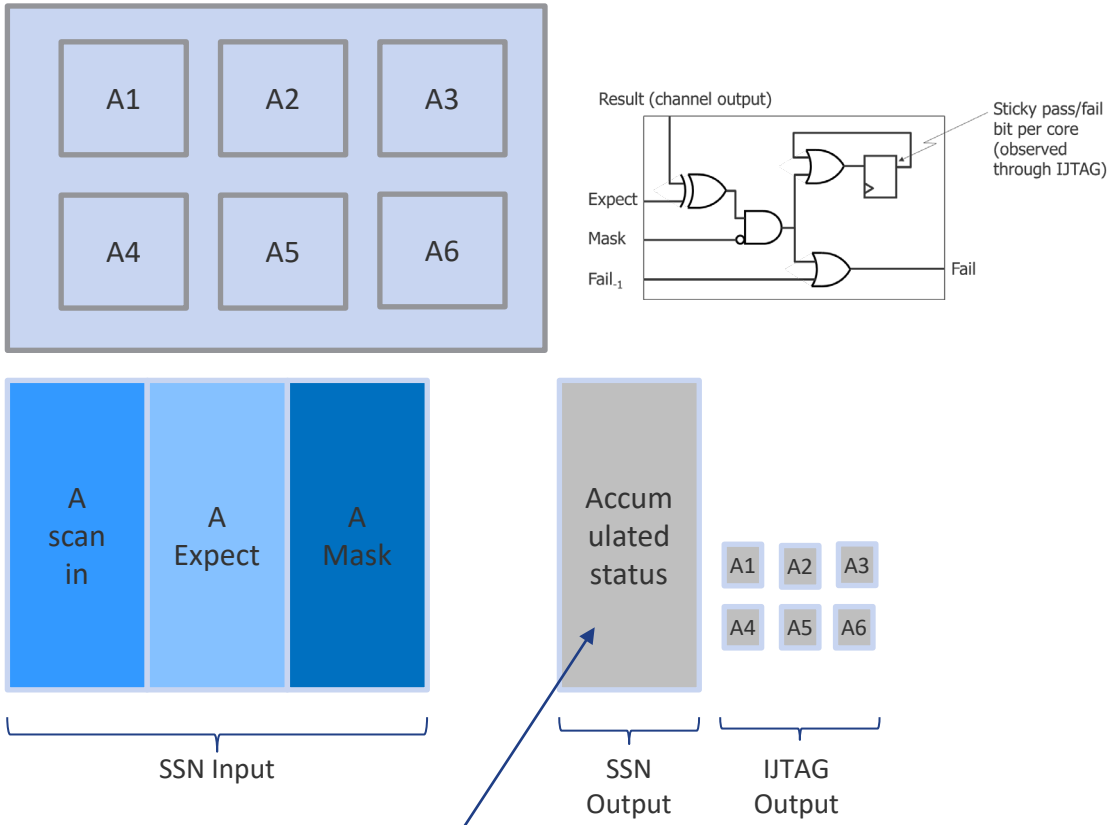
STR = Scan Test Record in the STDF

# Teradyne enabling Siemens SSN
## - OnChipCompare

- Test any number of identical cores at constant cost
- Scan in, expect data, and mask data for each set of identical cores delivered to all cores
- Compare circuitry for each core inside each host node
- Per-shift status bits accumulated across cores (SSN stream)
- Sticky status bit per core (IJTAG)

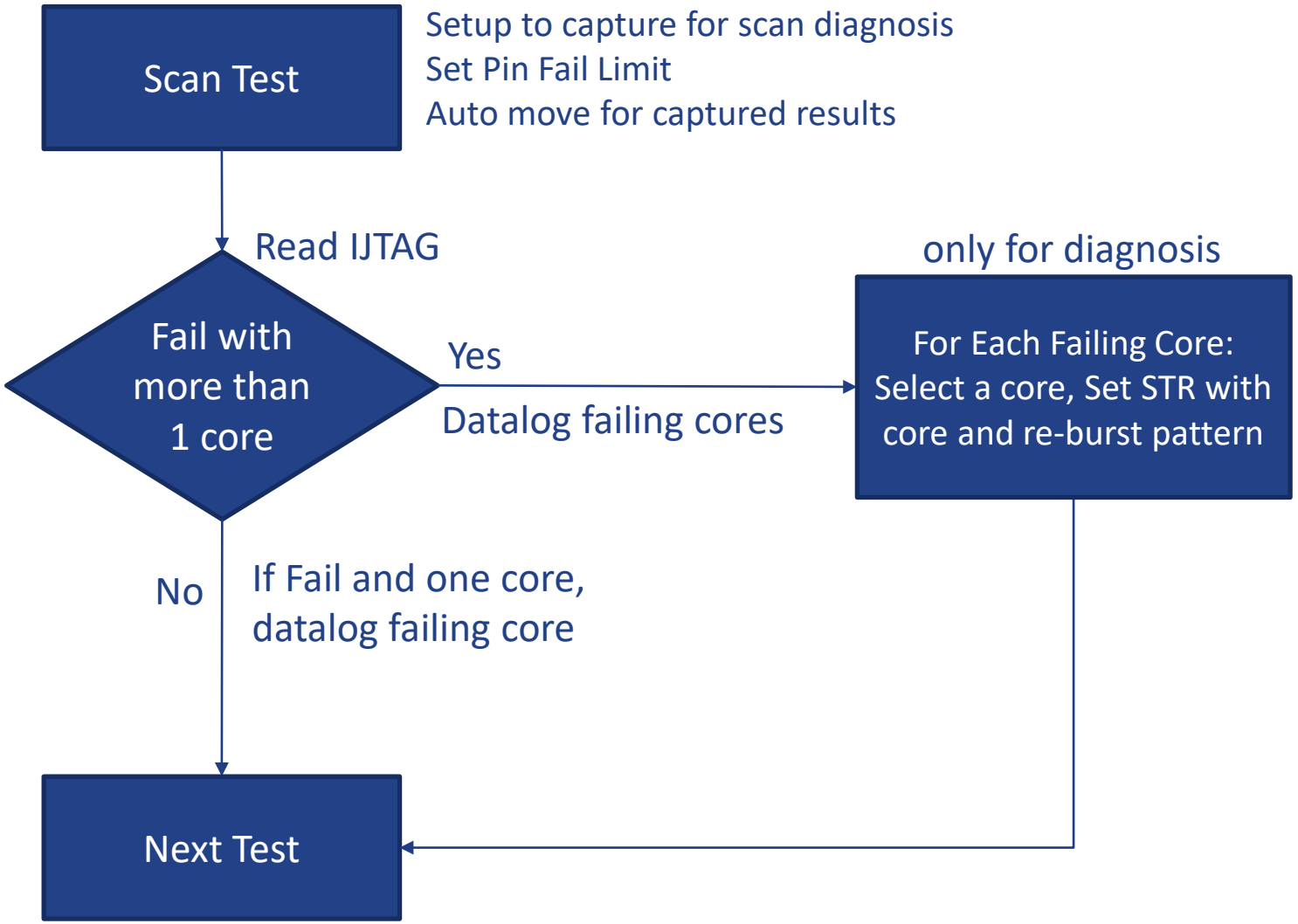



Example of pattern execution




One draw back is that logging will not know which core is failing. Requires unique test flow

# Teradyne enabling Siemens SSN
## - OnChipCompare Diagnosis flow




With internal compare you save test time but diagnosis has a case when re-burst is required. Multiple failing cores

UltraFLEX*plus* Solution

During re-burst phase will modify pattern to select a core. This ensures SSN output fail log from accumulated status register has a unique solution

STR = Scan Test Record in the STDF

New annotation in STIL file to locate core logging and core selection.

# Teradyne enabling Siemens SSN

| Use Case | Changes to Work flow | High level ATE implication |
|---|---|---|
| **SSN Tester Compare with a Single Core** | None | Some traditional debug methods cannot be used Note 1 |
| **SSN Tester Compare with Multiple Unique Cores -** Requires binning by core and core masking | Requires SSN core mapping information from STIL | Requires methodology to describe core and ability to mask core based on a cycle within the pattern |
| **SSN On-Chip Compare for Multiple Identical Cores -** Requires binning by core and core selecting | Requires information from STIL on setup and status registers | Requires methodology to retrieve failing information and map back to setup and status registers |
| **(+) IEEE 1149.10 -** Requires PEDDA initialization, KeepAlive, etc | New STIL formats | Bit alignment & Latency alignment<br>Split setup on low speed pins and scan on high speed pins |
| **(+) DDR high-speed IO for SSN** | TBD | In development with Siemens on implications |

Note 1: In the past chain = pin. Depending on SSN setup a chain is no longer associated with a pin and thus user can no longer mask a chain

# Teradyne enabling Siemens SSN

| Use Case | Test Insight Support | Teradyne Support |
|---|---|---|
| **SSN Tester Compare with a Single Core** | Yes | All IG-XL versions |
| **SSN Tester Compare with Multiple Unique Cores -** Requires binning by core and core masking | Plan on Q4 2022 | Planned for 10.40.00 |
| **SSN On-Chip Compare for Multiple Identical Cores -** Requires binning by core and core selecting | Plan on Q4 2022 | Planned for 10.40.00Px |
| **(+) IEEE 1149.10 -** Requires PEDDA initialization, KeepAlive, etc | Released in 2021 | 10.30.10 |
| **(+) DDR high-speed IO for SSN** | In development with Siemens on solution. | |

# Teradyne enabling Siemens SSN

**Siemens, Teradyne,** & **Test Insight** provides a **proven** design workflow for all use cases for SSN test patterns

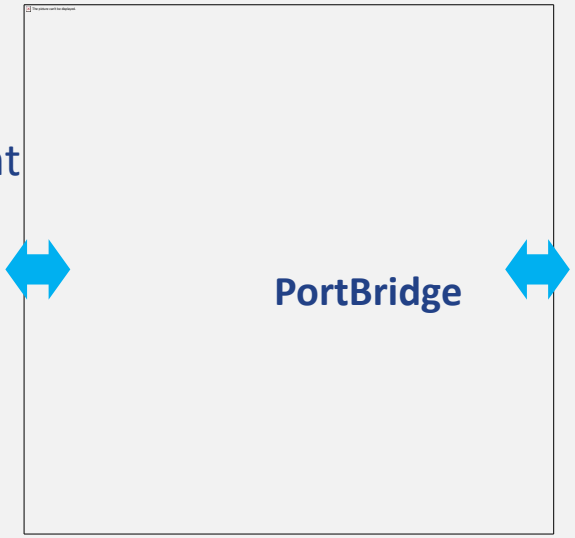
Design,
Core patterns,
Retargeting,
STIL

STIL → .atp

.atp → .pat,
Pattern Sets,
Test Methods,
Fail Processing


**Accelerate Debug**
with
Tessent **ATE-Connect** and Teradyne's **PortBridge**

Tessent
SiliconInsight




IGXL

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