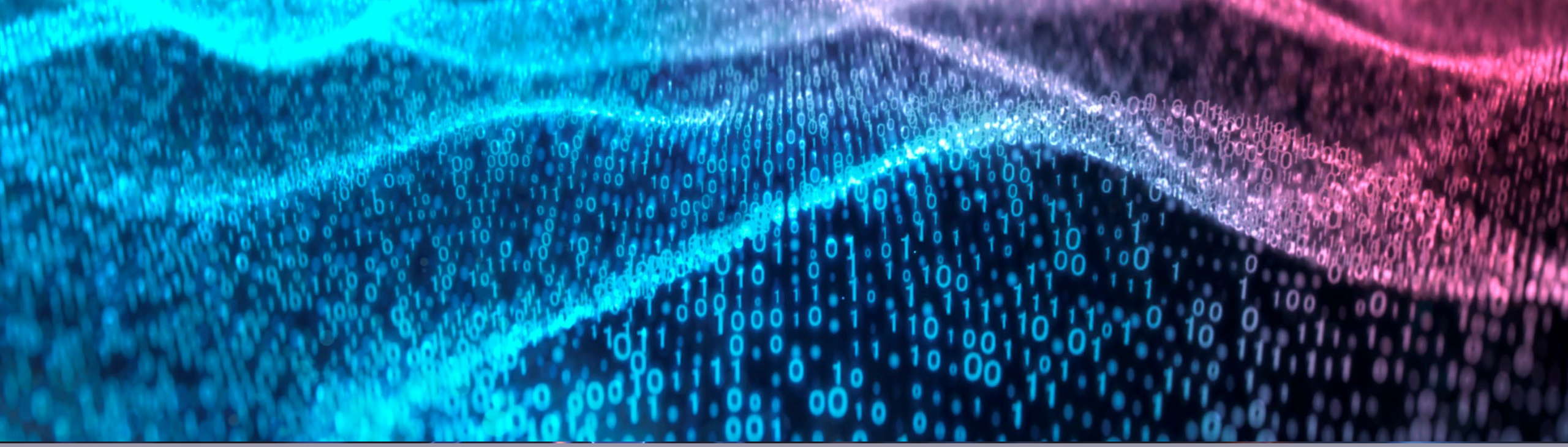

# ATPG Bench Validation with SSN and Salland's DTX

Gerwin Veltink – Salland Engineering
Kiyoshi Takeshita – Siemens DISW



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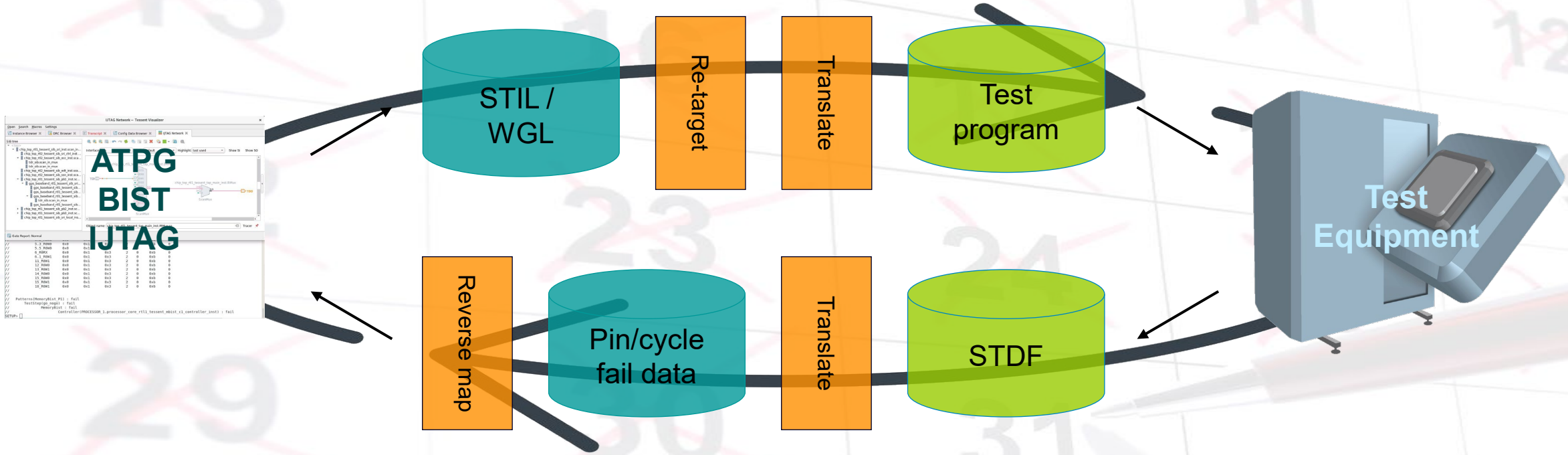
# Tessent SiliconInsight

## Introduction – Customers' challenges

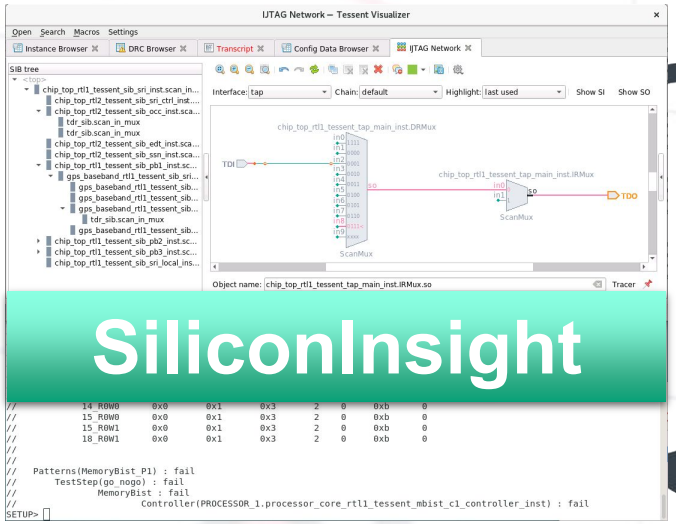
Silicon bring-up and diagnosis of embedded instruments require significant learning and is prone to errors causing increased cycle time



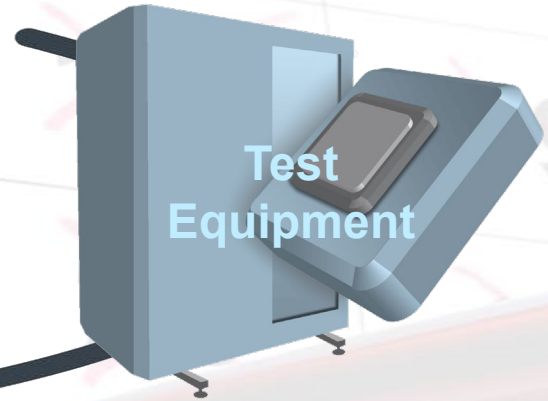

More difficult with non-intuitive results of SSN and with its on-chip compare.

# Tessent SiliconInsight
## Introduction – ATE-Connect

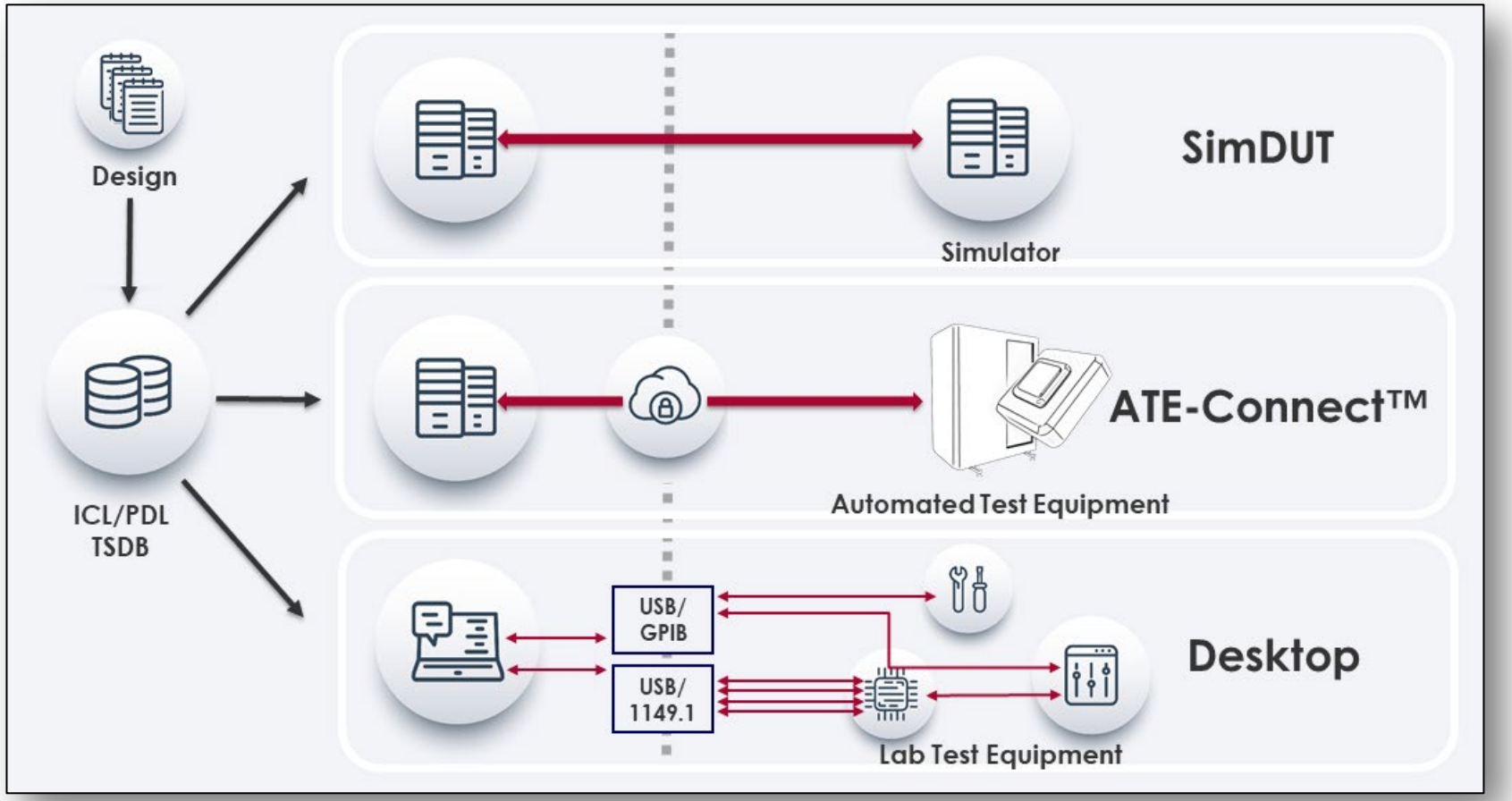
ATE-Connect technology in Tessent SiliconInsight introduces direct communication between Tessent DFT (Design for Test) software and testers, accelerating silicon bring-up from weeks to days







# ATE-Connect Solution
## Consistent among SimDUT, ATE-Connect and Desktop




Ensure bring-up is ready **before Si** comes back

First Si bring-up, debug and test for prototype ship

Rapid characterization for robust production test

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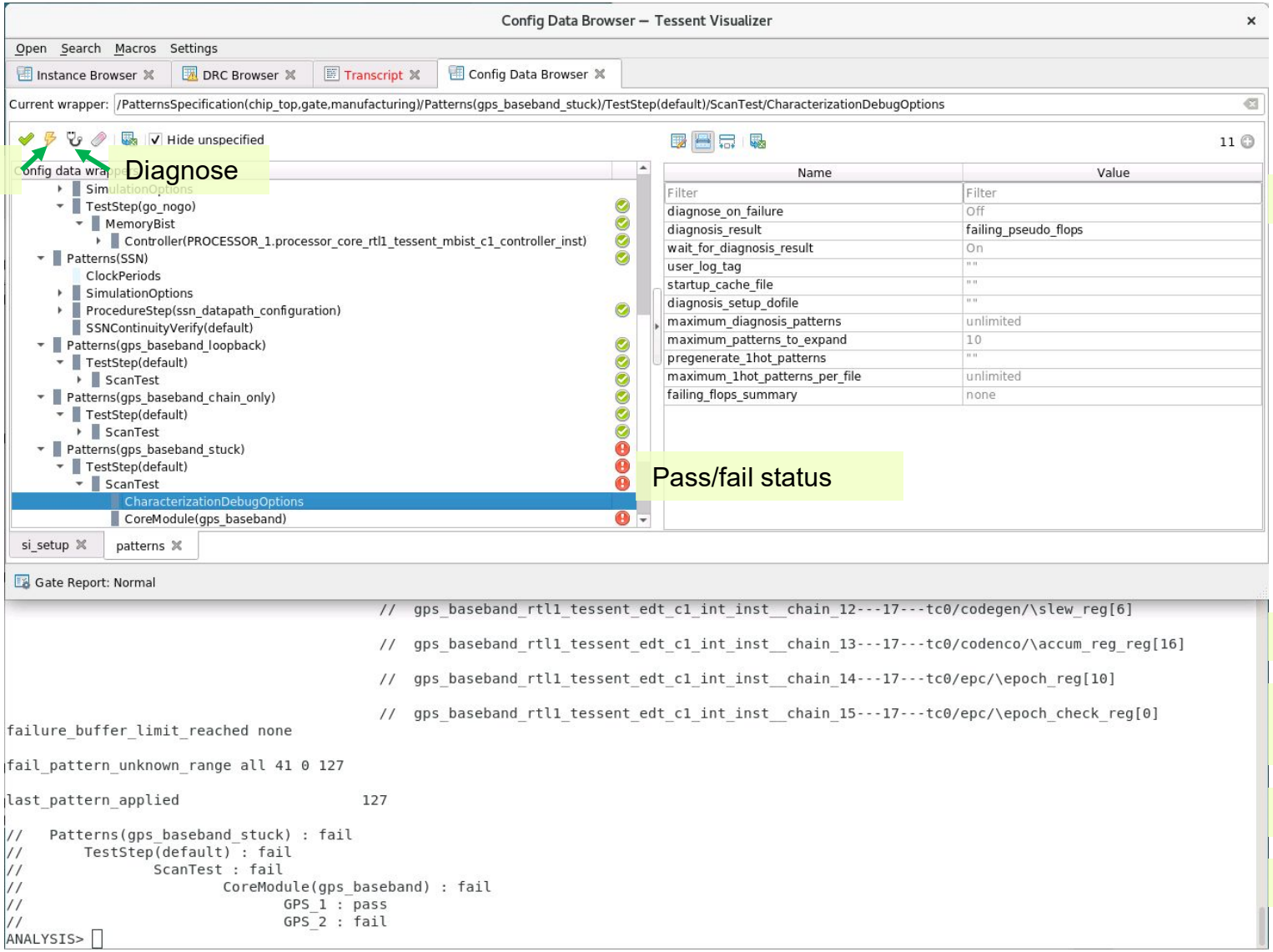
# Tessent SiliconInsight for SSN Diagnosis







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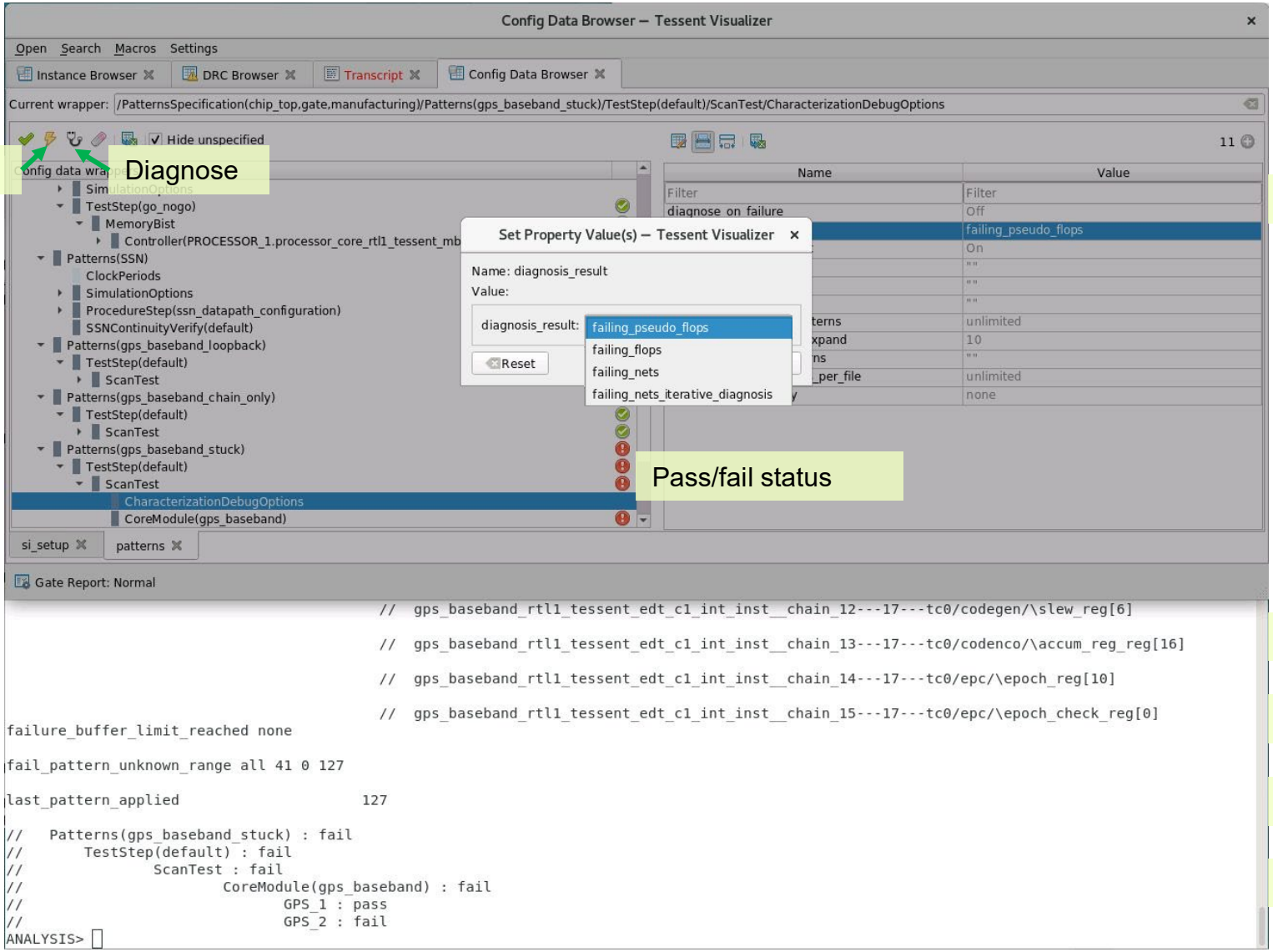
# Tessent SiliconInsight for SSN Diagnosis




Diagnosis settings

Detailed results

Customizable reports

Result introspection

Automation

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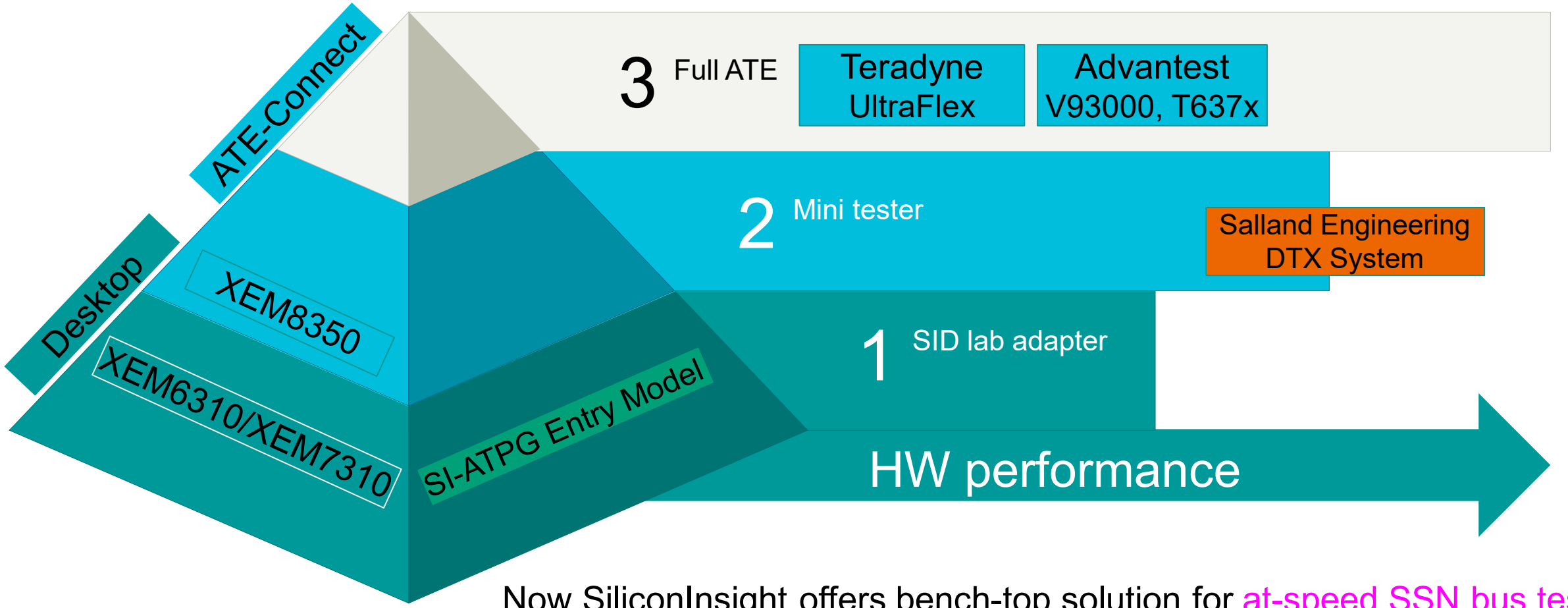
# SiliconInsight Landscape
## Product variation by hardware performance




Now SiliconInsight offers bench-top solution for at-speed SSN bus test.

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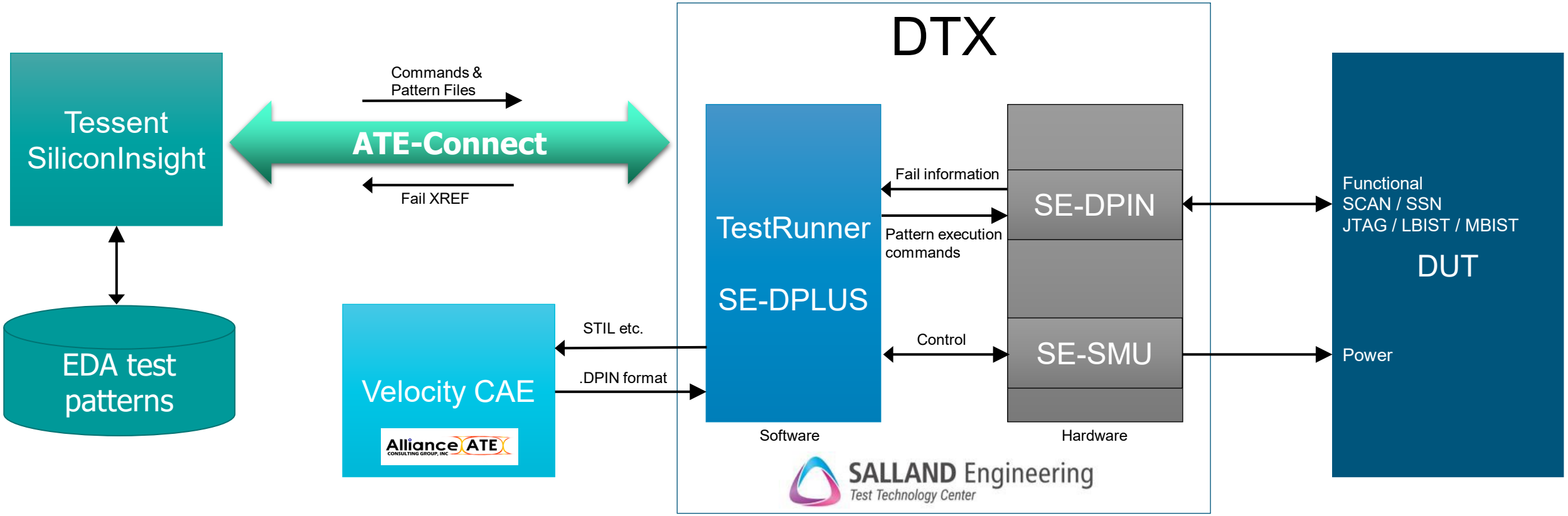
# Salland Engineering – DTX System

## Pattern flow for Post Silicon Validation, closed loop between EDA and DTX




1. Tessent SiliconInsight Generates STIL pattern
2. Velocity CAE tool converts to DPIN format
3. DPIN Executes Pattern and returns Fail Information to Silicon Insight via ATE-Connect
4. Silicon Insight finds Device faults or continues by generating next STIL pattern

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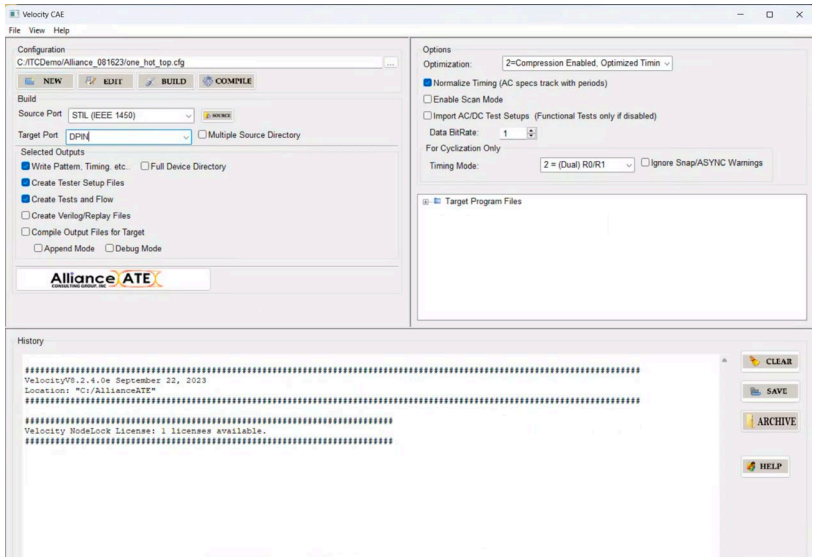
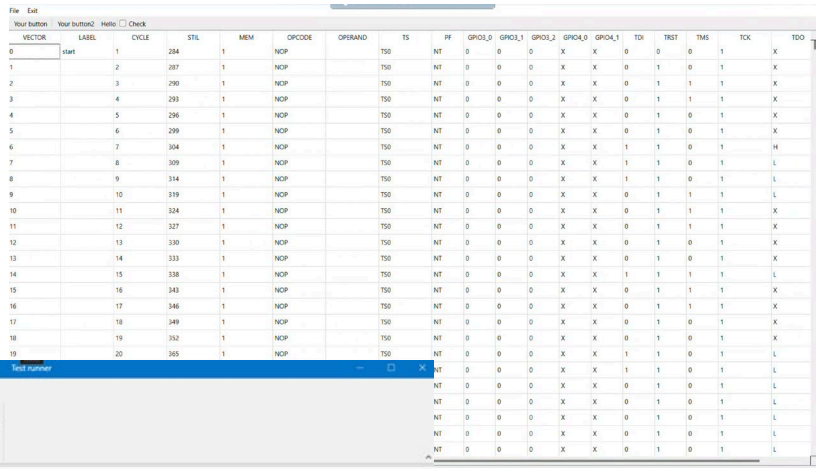
# Salland Engineering – DTX System
## Software

```
  }
//Pattern:233  Vector:947  TesterCycle:11899
Ann {* Pattern:233  Vector:947  TesterCycle:11899 *}
"pattern 233":
Macro "scan_edt_g1"  {
  "_ssn_datapath1_GPIO3_0_" = 1101001010000111111110000111101010101 \r10 1 01;
  "_ssn_datapath1_GPIO4_0_" = HHHHHHHLHLHLHLHLHLHLHLHLHLHLHHHHLLLLHHHHHLHLHLHLL;
  "_ssn_datapath2_GPIO3_1_" = 1 \r12 0 10100000000011110000010111101011011;
  "_ssn_datapath2_GPIO4_1_" = HHHHLHLLLHL \r10 H LHLLHLHLHL \r17 H L;
  }
//Pattern:234  Vector:948  TesterCycle:11947
Ann {* Pattern:234  Vector:948  TesterCycle:11947 *}
"pattern 234":
Macro "scan_edt_g1"  {
  "_ssn_datapath1_GPIO3_0_" = 00101101001010101111100001010 \r19 1;
  "_ssn_datapath1_GPIO4_0_" = \r12 L HLHLHLH \r29 X;
  "_ssn_datapath2_GPIO3_1_" = 01111000011111111010110100000 \r19 1;
  "_ssn_datapath2_GPIO4_1_" = HLHLHLHHHHHLLLLLLLXLXL \r25 X;
```

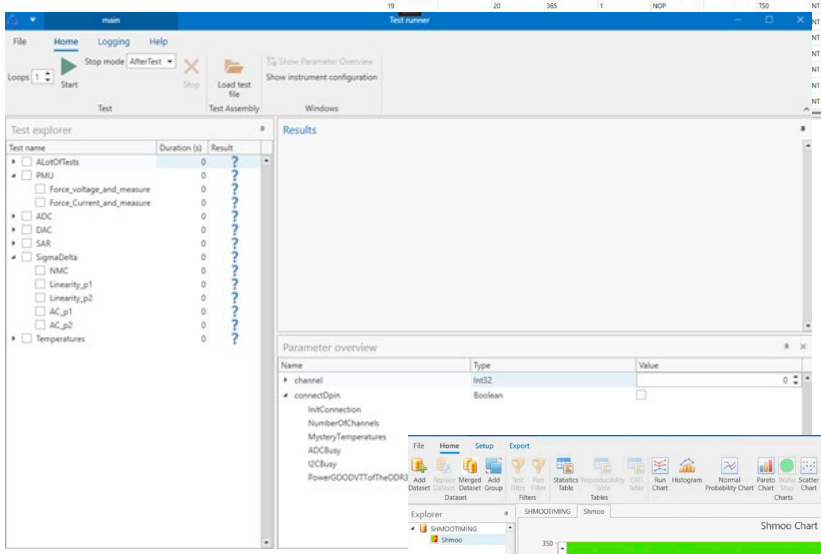
STIL pattern



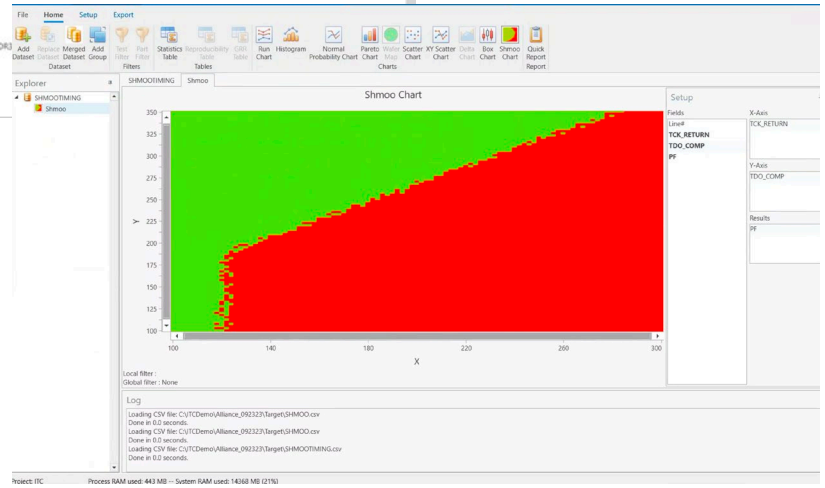

Velocity CAE



SE-DPIN pattern




Testrunner GUI




SE-DPLUS

SALLAND Engineering
Test Technology Center

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# Salland Engineering – DTX System
## Hardware specifications of Salland SE-DPIN core

SALLAND Engineering
Test Technology Center

| Parameter | SE-DPIN64-PXIe | SE-DPIN32-PXIe | SE-DPIN16 |
|---|---|---|---|
| **Form-factor** | PXIe single slot - 214mm x 131mm | | Module - 85mm x 72mm |
| **# of I/O channels** (note-1) | 64 single-ended / 32 differential | 32 single-ended / 16 differential | 16 single-ended / 8 differential |
| **Vector Memory** | Large 256M / Small 4k vectors per channel | | |
| **Source & Capture Memory** | 64Mbit per channel | | |
| **Error Memory** | 1k per channel | | |
| **Max vector rate** | High Voltage mode 50MHz (-2V to +6V) \|\| High Speed mode 200MHz (0V to +4V) | | |
| **Edge placement resolution** | 39.0625ps hardware; 1.22ps programming | | |
| **# timesets** | 127 | | |
| **Max offset (DGS – GND)** | ±300mV | | |
| **Per Pin PMU (FV/FI/MV/MI)** | -2V to +6V; ±50mA; Active load ±24mA | | |
| **Protocol R/W (I2C / SPI / UART)** | 200Mbps | | |
| **Maximum number of events** | 400Mbps (some formats) | | |
| **Scan Memory (max)** | 8Gbit scan depth (1x chain per 16ch) | | |
| **Scan Chain (max)** | 32 (32x SCANin + 32x SCANout) | 16 (16x SCANin + 16x SCANout) | 8 (8x SCANin + 8x SCANout) |
| **Power dissipation** | 83W (Max) | 45W (Max) | 24W |

- DPIN is offering full ATE IO technology with PPMU, ILoads, Level & Timing setting per pin up to 400Mbps.

Note 1: Multiple SE-DPIN PXIe cards can be installed to increase the channel count.




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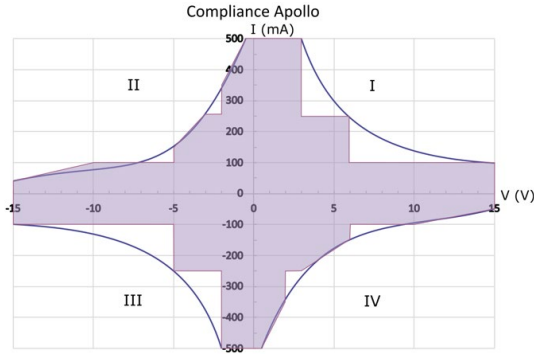
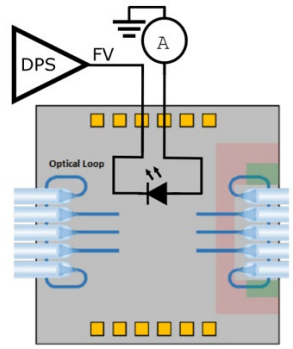
# Salland Engineering – DTX System
## Hardware specifications of Salland SE-SMU16

SALLAND Engineering
Test Technology Center

| Parameter | SE-SMU16-PXIe | | |
|---|---|---|---|
| **Form-factor** | PXIe single slot - 214mm x 131mm | | |
| **# of I/O DPS channels** | 16 | | |
| **Support modes** | FV, MV, FI, MI, HIz | | |
| **Force Voltage Ranges** | Compliance current | | DC Accuracy |
| **-2V to +3V** | ±5uA, ±25uA, ±250uA, ±2.5mA, ±25mA, ±100mA, ±250mA, ±500mA | | ±(0.2%FV + 10 mV) |
| **-5V to +6V** | ±5uA, ±25uA, ±250uA, ±2.5mA, ±25mA, ±100mA, ±250mA | | ±(0.2%FV + 15 mV) |
| **±15V** | ±5uA, ±25uA, ±250uA, ±2.5mA, ±25mA, ±100mA | | ±(0.2%FV + 20 mV) |
| **Measure Voltage Ranges** | Compliance current | | DC Accuracy |
| **-2V to +3V** | 126uV / LSB | | ±(0.2%FV + 10 mV) |
| **-5V to +6V** | 252uV / LSB | | ±(0.2%FV + 15 mV) |
| **±15V** | 504uV / LSB | | ±(0.2%FV + 20 mV) |
| **Force Current Ranges** | Ranges | | DC accuracy |
| | ±5uA, ±25uA, ±250uA, ±2.5mA, ±25mA, ±100mA, ±250mA, ±500mA | | TBD |
| **Measure Current Ranges** | Ranges | | DC accuracy |
| | ±5uA, ±25uA, ±250uA, ±2.5mA, ±25mA, ±100mA, ±250mA, ±500mA | | TBD |
| **Ganging** | Yes, 16 channels => 8 A | | |
| **# of Low Current channels** | 16 (low side sending measurement method) | | |
| **Current ranges** | DC accuracy | Resolution | Measurement time |
| **0 – 3nA** | ±(0.3%FSR + 500fA) | 46fA | 1ms |
| **0 – 6nA** | ±(0.3%FSR + 0.9pA) | 92fA | 1ms |
| **0 – 12nA** | ±(0.3%FSR + 1.7pA) | 0.18pA | 1ms |
| **0 – 300nA** | ±(0.2%FSR + 60pA) | 4.6pA | 0.02ms |
| **0 – 600nA** | ±(0.2%FSR + 110pA) | 9.2pA | 0.02ms |
| **0 – 1200nA** | ±(0.2%FSR + 200pA) | 18.5pA | 0,02ms |



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# Summary

- Tessent SiliconInsight offers quick turn-around time of silicon bring-up and diagnosis with direct communication between Tessent DFT software and test equipment.
- ATE-Connect technology enables Tessent SiliconInsight to control and observe DUT operated on 3rd-party test equipment such as ATE (Automated Test Equipment).
- Salland Engineering DTX System is now one of ATE-Connect partners, which allows our customers to run SSN bus test at speed in the bench test environment.




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