



ATPG Bench Validation with SSN and Salland's DTX

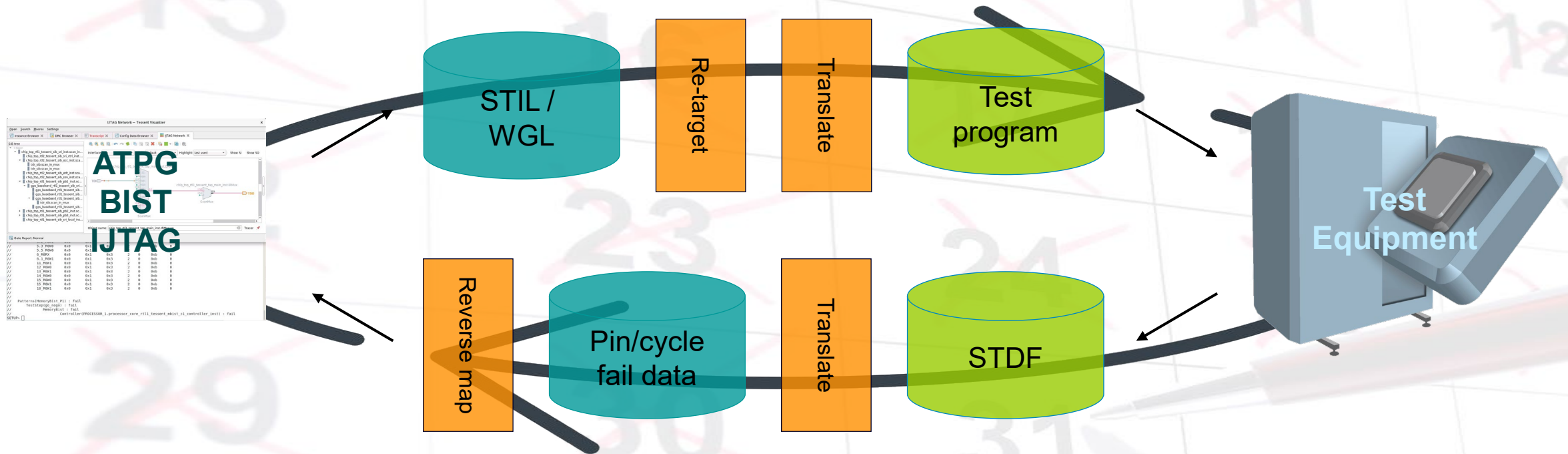
Gerwin Veltink – Salland Engineering

Kiyoshi Takeshita – Siemens DISW

Tessent SiliconInsight

Introduction – Customers' challenges

Silicon bring-up and diagnosis of embedded instruments require significant learning and is prone to errors causing increased cycle time

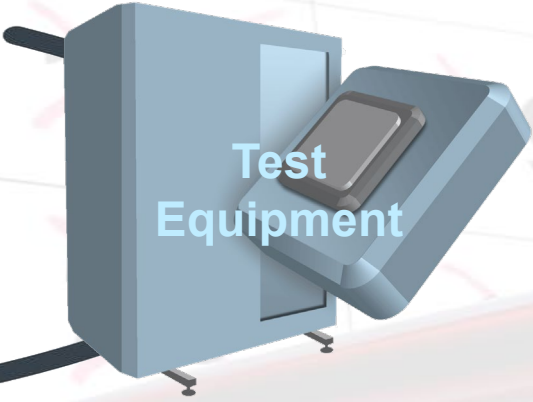
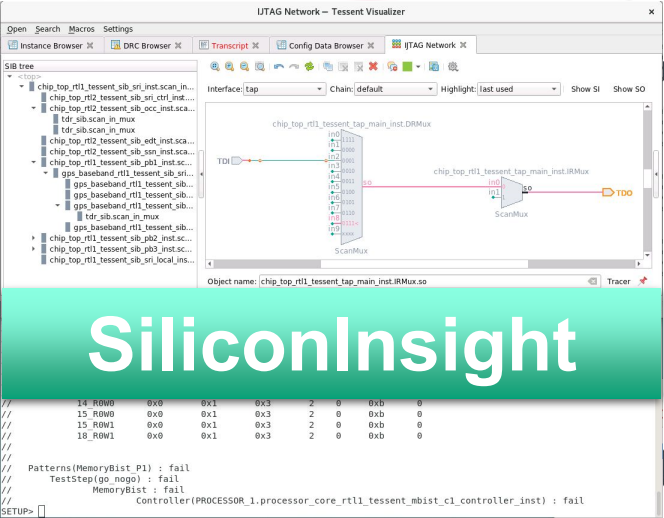


More difficult with non-intuitive results of SSN and with its on-chip compare.

Tessent SiliconInsight

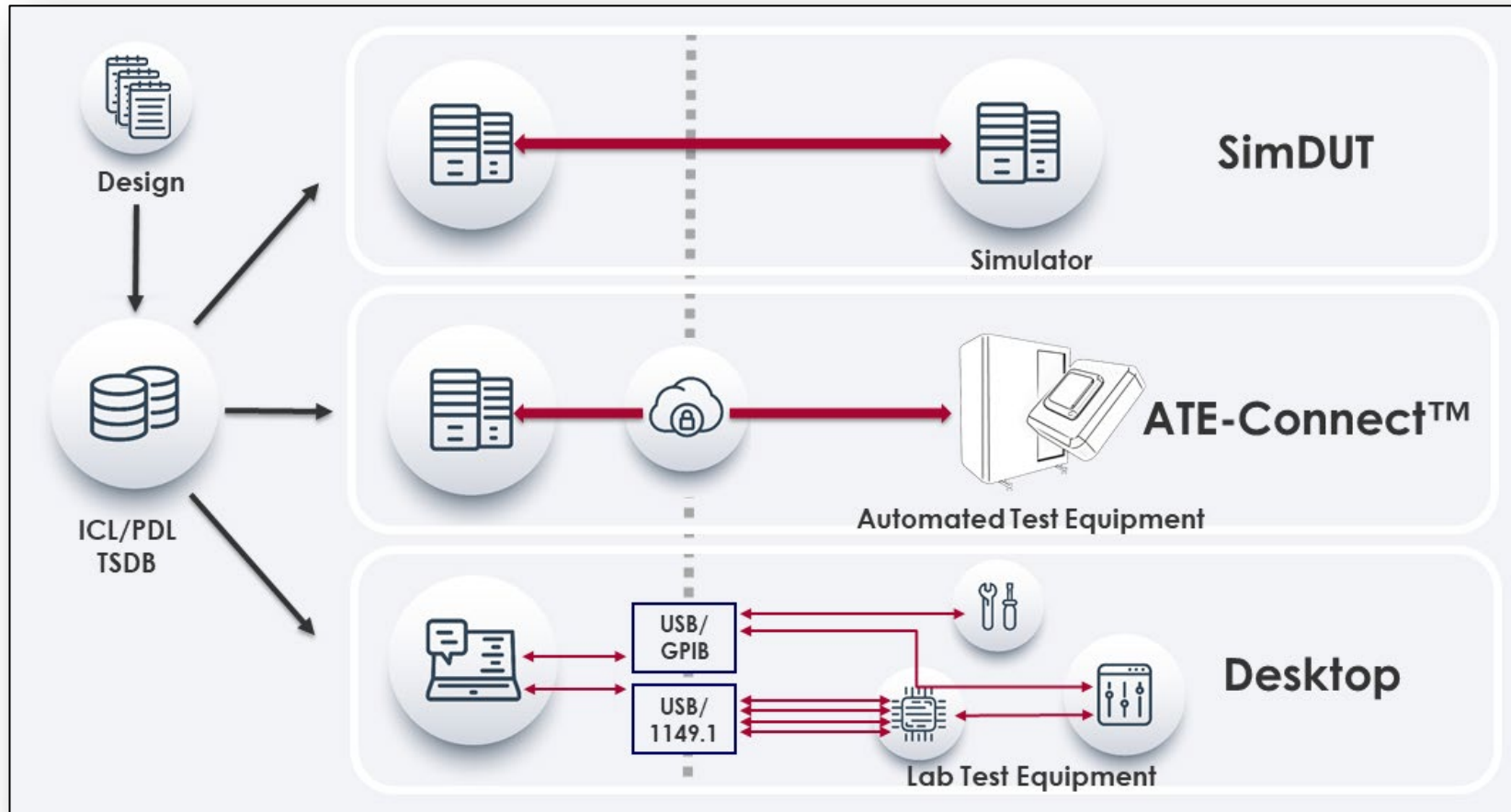
Introduction – ATE-Connect

ATE-Connect technology in Tessent SiliconInsight introduces direct communication between Tessent DFT (Design for Test) software and testers, accelerating silicon bring-up from weeks to days



ATE-Connect Solution

Consistent among SimDUT, ATE-Connect and Desktop



Ensure bring-up is ready **before Si** comes back

First Si bring-up, debug and test for prototype ship

Rapid characterization for robust production test

Tessent SiliconInsight for SSN Diagnosis

The screenshot shows the 'Config Data Browser - Tessent Visualizer' window. It features a menu bar (Open, Search, Macros, Settings) and several tabs (Instance Browser, DRC Browser, Transcript, Config Data Browser). The current wrapper path is displayed as: /PatternsSpecification(chip_top.gate.manufacturing)/Patterns(gps_baseband_stuck)/TestStep(default)/ScanTest/CharacterizationDebugOptions.

On the left, a tree view shows the configuration hierarchy. A green callout box labeled 'Execute' points to the 'Execute' icon, and another labeled 'Diagnose' points to the 'Diagnose' icon. The tree includes nodes like SimulationOptions, TestStep(go_nogo), MemoryBist, Controller, Patterns(SSN), ClockPeriods, SimulationOptions, ProcedureStep(ssn_datapath_configuration), SSNContinuityVerify(default), Patterns(gps_baseband_loopback), TestStep(default), ScanTest, Patterns(gps_baseband_chain_only), TestStep(default), ScanTest, Patterns(gps_baseband_stuck), TestStep(default), ScanTest, CharacterizationDebugOptions, and CoreModule(gps_baseband). A 'Pass/fail status' callout points to the status icons (green checkmarks and red exclamation marks) next to the nodes.

On the right, a table lists diagnosis settings:

Name	Value
Filter	Filter
diagnose_on_failure	Off
diagnosis_result	failing_pseudo_flops
wait_for_diagnosis_result	On
user_log_tag	""
startup_cache_file	""
diagnosis_setup_dofile	""
maximum_diagnosis_patterns	unlimited
maximum_patterns_to_expand	10
pregenerate_1hot_patterns	""
maximum_1hot_patterns_per_file	unlimited
failing_flops_summary	none

A 'Diagnosis settings' callout points to this table.

At the bottom, a 'Gate Report: Normal' section displays test results in a code-like format:

```
// gps_baseband_rtl1_tessent_edt_c1_int_inst_chain_12---17---tc0/codegen/\slew_reg[6]
// gps_baseband_rtl1_tessent_edt_c1_int_inst_chain_13---17---tc0/codenco/\accum_reg_reg[16]
// gps_baseband_rtl1_tessent_edt_c1_int_inst_chain_14---17---tc0/epc/\epoch_reg[10]
// gps_baseband_rtl1_tessent_edt_c1_int_inst_chain_15---17---tc0/epc/\epoch_check_reg[0]

failure_buffer_limit_reached none

fail_pattern_unknown_range all 41 0 127

last_pattern_applied          127

//   Patterns(gps_baseband_stuck) : fail
//     TestStep(default) : fail
//       ScanTest : fail
//         CoreModule(gps_baseband) : fail
//           GPS_1 : pass
//           GPS_2 : fail

ANALYSIS>
```

Callouts on the right side of the report area include 'Detailed results', 'Customizable reports', 'Result introspection', and 'Automation'.



Tessent SiliconInsight for SSN Diagnosis

The screenshot shows the Tessent Visualizer interface. The main window is titled "Config Data Browser - Tessent Visualizer". It features a tree view on the left, a central table of properties, and a bottom pane for reports. A "Set Property Value(s)" dialog box is open, showing a dropdown menu for "diagnosis_result" with options like "failing_pseudo_flops", "failing_flops", "failing_nets", and "failing_nets_iterative_diagnosis".

Annotations on the screenshot include:

- Execute**: A green arrow points to the "Execute" icon in the toolbar.
- Diagnose**: A green arrow points to the "Diagnose" icon in the toolbar.
- Diagnosis settings**: A yellow box highlights the "diagnose on failure" and "failing_pseudo_flops" rows in the table.
- Pass/fail status**: A yellow box highlights the status icons (green checkmarks and red exclamation marks) in the tree view.
- Detailed results**: A yellow box highlights the "Gate Report: Normal" section.
- Customizable reports**: A yellow box highlights the "failure_buffer_limit_reached none" and "fail_pattern_unknown_range all 41 0 127" lines.
- Result introspection**: A yellow box highlights the "last_pattern_applied 127" line.
- Automation**: A yellow box highlights the "Patterns(gps_baseband_stuck) : fail" and "TestStep(default) : fail" lines.

Name	Filter	Value
diagnose on failure	Filter	Off
failing_pseudo_flops	Filter	On
		..
		..
Patterns		unlimited
xpand		10
ns		..
per_file		unlimited
		none

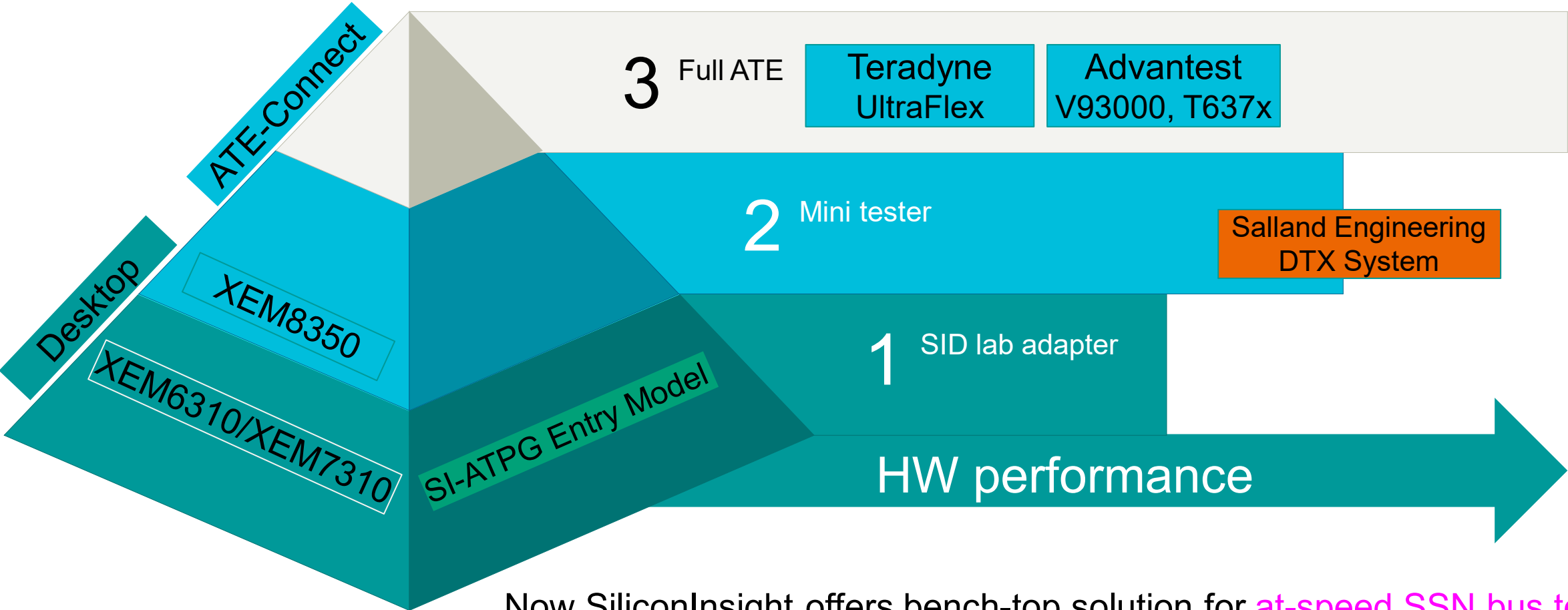
```
Gate Report: Normal
// gps_baseband_rtl1_tessent_edt_c1_int_inst_chain_12---17---tc/codegen/\slew_reg[6]
// gps_baseband_rtl1_tessent_edt_c1_int_inst_chain_13---17---tc/codenco/\accum_reg_reg[16]
// gps_baseband_rtl1_tessent_edt_c1_int_inst_chain_14---17---tc/epc/\epoch_reg[10]
// gps_baseband_rtl1_tessent_edt_c1_int_inst_chain_15---17---tc/epc/\epoch_check_reg[0]

failure_buffer_limit_reached none
fail_pattern_unknown_range all 41 0 127
last_pattern_applied 127
// Patterns(gps_baseband_stuck) : fail
// TestStep(default) : fail
// ScanTest : fail
// CoreModule(gps_baseband) : fail
// GPS_1 : pass
// GPS_2 : fail
ANALYSIS>
```



SiliconInsight Landscape

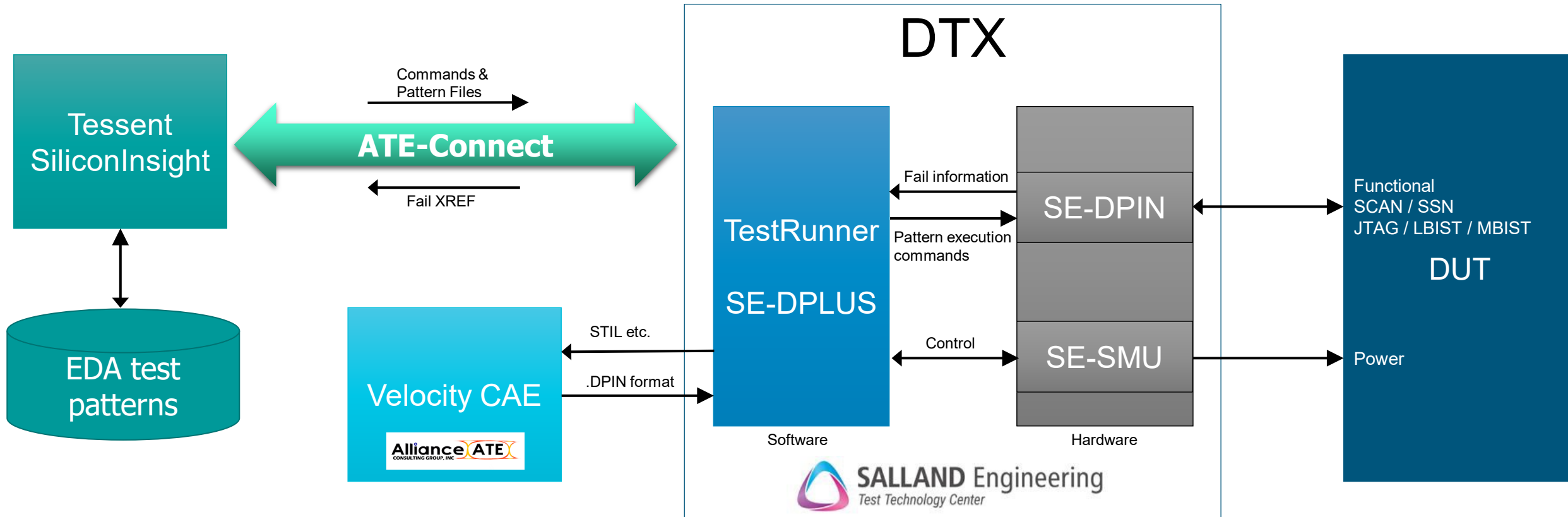
Product variation by hardware performance



Now SiliconInsight offers bench-top solution for **at-speed SSN bus test**.

Salland Engineering – DTX System

Pattern flow for Post Silicon Validation, closed loop between EDA and DTX



1. Tessent SiliconInsight Generates STIL pattern
2. Velocity CAE tool converts to DPIN format
3. DPIN Executes Pattern and returns Fail Information to Silicon Insight via ATE-Connect
4. Silicon Insight finds Device faults or continues by generating next STIL pattern

Salland Engineering – DTX System Software

VECTOR	start	CYCLE	STL	MEM	OPCODE	OPRND	TS	PF	GPIO_0	GPIO_1	GPIO_2	GPIO_3	GPIO_4	GPIO_5	TCK	TMS	TCK	TDO
0	1	234	1		NOP		T50	NT	0	0	0	X	X	0	1	1		X
1	2	287	1		NOP		T50	NT	0	0	0	X	X	0	1	1		X
2	3	290	1		NOP		T50	NT	0	0	0	X	X	0	1	1		X
3	4	293	1		NOP		T50	NT	0	0	0	X	X	0	1	1		X
4	5	296	1		NOP		T50	NT	0	0	0	X	X	0	1	1		X
5	6	299	1		NOP		T50	NT	0	0	0	X	X	0	1	1		X
6	7	304	1		NOP		T50	NT	0	0	0	X	X	1	1	0		H
7	8	309	1		NOP		T50	NT	0	0	0	X	X	1	1	0		L
8	9	314	1		NOP		T50	NT	0	0	0	X	X	1	1	0		L
9	10	319	1		NOP		T50	NT	0	0	0	X	X	0	1	1		L
10	11	324	1		NOP		T50	NT	0	0	0	X	X	0	1	1		X
11	12	327	1		NOP		T50	NT	0	0	0	X	X	0	1	1		X
12	13	330	1		NOP		T50	NT	0	0	0	X	X	0	1	0		X
13	14	333	1		NOP		T50	NT	0	0	0	X	X	0	1	0		X
14	15	338	1		NOP		T50	NT	0	0	0	X	X	1	1	1		L
15	16	343	1		NOP		T50	NT	0	0	0	X	X	0	1	1		X
16	17	346	1		NOP		T50	NT	0	0	0	X	X	0	1	1		X
17	18	349	1		NOP		T50	NT	0	0	0	X	X	0	1	0		X
18	19	352	1		NOP		T50	NT	0	0	0	X	X	0	1	0		X
19	20	365	1		NOP		T50	NT	0	0	0	X	X	1	1	0		L

```
//Pattern:233 Vector:947 TesterCycle:11899
Ann {* Pattern:233 Vector:947 TesterCycle:11899 *}
"pattern 233":
Macro "scan_edt_g1" {
  "ssn_datapath1_GPIO3_0" = 110100101000011111110000111101010 \r10 1 01;
  "ssn_datapath1_GPIO4_0" = HHHHHHLLHLHLHLHLHLHLHLHHHHLLLLHHHHHLLHLHLHL;
  "ssn_datapath2_GPIO3_1" = 1 \r12 0 10100000000011110000010111110101101;
  "ssn_datapath2_GPIO4_1" = HHHHLLHLHL \r10 H LHLHLHLHL \r17 H L;
}
//Pattern:234 Vector:948 TesterCycle:11947
Ann {* Pattern:234 Vector:948 TesterCycle:11947 *}
"pattern 234":
Macro "scan_edt_g1" {
  "ssn_datapath1_GPIO3_0" = 00101101001010101111100001010 \r19 1;
  "ssn_datapath1_GPIO4_0" = \r12 L HLHLHLH \r29 X;
  "ssn_datapath2_GPIO3_1" = 0111100001111111010110100000 \r19 1;
  "ssn_datapath2_GPIO4_1" = HLHLHLHHHHLLLLLLLLLXLX \r25 X;
}
```

STIL pattern

The screenshot shows the Testrunner GUI with the following components:

- Test explorer:** A tree view showing test categories like ALUOfTests, PMU, Force_voltage_and_measure, Force_Current_and_measure, ADC, DAC, SAR, SigmaDelta, NMC, Linearity_p1, Linearity_p2, AC_p1, AC_p2, and Temperatures.
- Results:** A window displaying test results, including a table with columns for Name, Type, and Value.
- Parameter overview:** A table showing parameters such as channel (In62), Boolean, and other test-specific settings.

SE-DPIN pattern

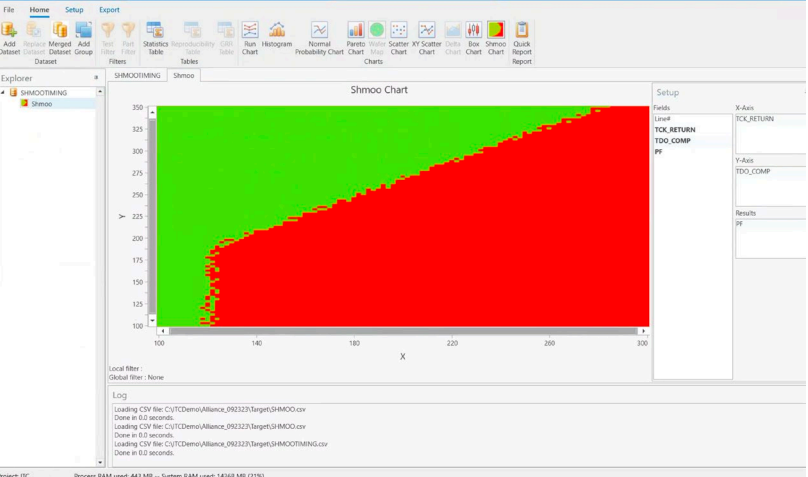


The screenshot shows the Velocity CAE software interface with the following components:

- Configuration:** Includes options for optimization (2-Compression Enabled), scan mode, and data bit rate.
- Build:** Shows source port (STL (IEEE 1450)) and target port (DPN).
- Selected Outputs:** Includes options for writing patterns, creating test setup files, and creating Verilog/Replay files.
- History:** A log window showing the software version (VelocityV8.2.4.0e) and the date (September 22, 2023).

Velocity CAE

Testrunner GUI



SE-DPLUS



Salland Engineering – DTX System

Hardware specifications of Salland SE-DPIN core



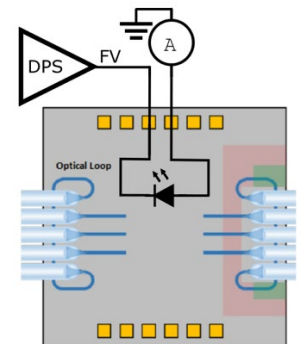
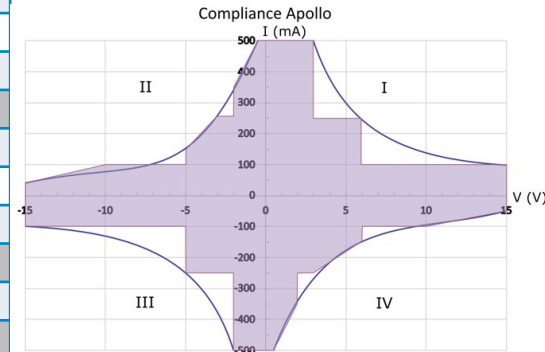
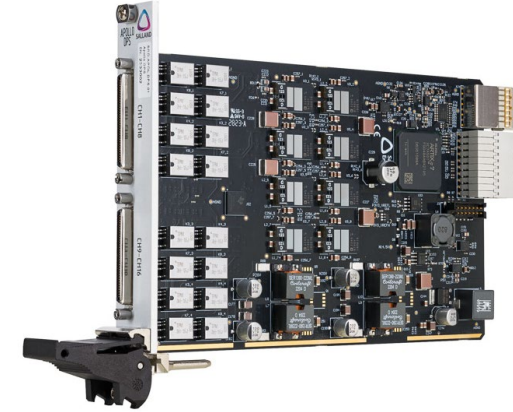
Parameter	SE-DPIN64-PXle	SE-DPIN32-PXle	SE-DPIN16
Form-factor	PXle single slot - 214mm x 131mm		Module - 85mm x 72mm
# of I/O channels <small>(note-1)</small>	64 single-ended / 32 differential	32 single-ended / 16 differential	16 single-ended / 8 differential
Vector Memory	Large 256M / Small 4k vectors per channel		
Source & Capture Memory	64Mbit per channel		
Error Memory	1k per channel		
Max vector rate	High Voltage mode 50MHz (-2V to +6V) High Speed mode 200MHz (0V to +4V)		
Edge placement resolution	39.0625ps hardware; 1.22ps programming		
# timesets	127		
Max offset (DGS – GND)	±300mV		
Per Pin PMU (FV/FI/MV/MI)	-2V to +6V; ±50mA; Active load ±24mA		
Protocol R/W (I2C / SPI / UART)	200Mbps		
Maximum number of events	400Mbps (some formats)		
Scan Memory (max)	8Gbit scan depth (1x chain per 16ch)		
Scan Chain (max)	32 (32x SCANin + 32x SCANout)	16 (16x SCANin + 16x SCANout)	8 (8x SCANin + 8x SCANout)
Power dissipation	83W (Max)	45W (Max)	24W

- DPIN is offering full ATE IO technology with PPMU, ILoads, Level & Timing setting per pin up to 400Mbps.

Note 1: Multiple SE-DPIN PXle cards can be installed to increase the channel count.

Salland Engineering – DTX System

Hardware specifications of Salland SE-SMU16



Parameter	SE-SMU16-PXIe		
Form-factor	PXIe single slot - 214mm x 131mm		
# of I/O DPS channels	16		
Support modes	FV, MV, FI, MI, HIz		
Force Voltage Ranges	Compliance current	DC Accuracy	
-2V to +3V	$\pm 5\mu\text{A}, \pm 25\mu\text{A}, \pm 250\mu\text{A}, \pm 2.5\text{mA}, \pm 25\text{mA}, \pm 100\text{mA}, \pm 250\text{mA}, \pm 500\text{mA}$	$\pm(0.2\%FV + 10\text{ mV})$	
-5V to +6V	$\pm 5\mu\text{A}, \pm 25\mu\text{A}, \pm 250\mu\text{A}, \pm 2.5\text{mA}, \pm 25\text{mA}, \pm 100\text{mA}, \pm 250\text{mA}$	$\pm(0.2\%FV + 15\text{ mV})$	
$\pm 15\text{V}$	$\pm 5\mu\text{A}, \pm 25\mu\text{A}, \pm 250\mu\text{A}, \pm 2.5\text{mA}, \pm 25\text{mA}, \pm 100\text{mA}$	$\pm(0.2\%FV + 20\text{ mV})$	
Measure Voltage Ranges	Compliance current	DC Accuracy	
-2V to +3V	126 μV / LSB	$\pm(0.2\%FV + 10\text{ mV})$	
-5V to +6V	252 μV / LSB	$\pm(0.2\%FV + 15\text{ mV})$	
$\pm 15\text{V}$	504 μV / LSB	$\pm(0.2\%FV + 20\text{ mV})$	
Force Current Ranges	Ranges	DC accuracy	
	$\pm 5\mu\text{A}, \pm 25\mu\text{A}, \pm 250\mu\text{A}, \pm 2.5\text{mA}, \pm 25\text{mA}, \pm 100\text{mA}, \pm 250\text{mA}, \pm 500\text{mA}$	TBD	
Measure Current Ranges	Ranges	DC accuracy	
	$\pm 5\mu\text{A}, \pm 25\mu\text{A}, \pm 250\mu\text{A}, \pm 2.5\text{mA}, \pm 25\text{mA}, \pm 100\text{mA}, \pm 250\text{mA}, \pm 500\text{mA}$	TBD	
Ganging	Yes, 16 channels => 8 A		
# of Low Current channels	16 (low side sending measurement method)		
Current ranges	DC accuracy	Resolution	Measurement time
0 – 3nA	$\pm(0.3\%FSR + 500\text{fA})$	46fA	1ms
0 – 6nA	$\pm(0.3\%FSR + 0.9\text{pA})$	92fA	1ms
0 – 12nA	$\pm(0.3\%FSR + 1.7\text{pA})$	0.18pA	1ms
0 – 300nA	$\pm(0.2\%FSR + 60\text{pA})$	4.6pA	0.02ms
0 – 600nA	$\pm(0.2\%FSR + 110\text{pA})$	9.2pA	0.02ms
0 – 1200nA	$\pm(0.2\%FSR + 200\text{pA})$	18.5pA	0,02ms

Summary

- Tessent SiliconInsight offers quick turn-around time of silicon bring-up and diagnosis with direct communication between Tessent DFT software and test equipment.
- ATE-Connect technology enables Tessent SiliconInsight to control and observe DUT operated on 3rd-party test equipment such as ATE (Automated Test Equipment).
- Salland Engineering DTX System is now one of ATE-Connect partners, which allows our customers to run SSN bus test at speed in the bench test environment.