ITC 2024 PO 39: Improved area overhead with advanced memory dump and memory test automation for AI chips

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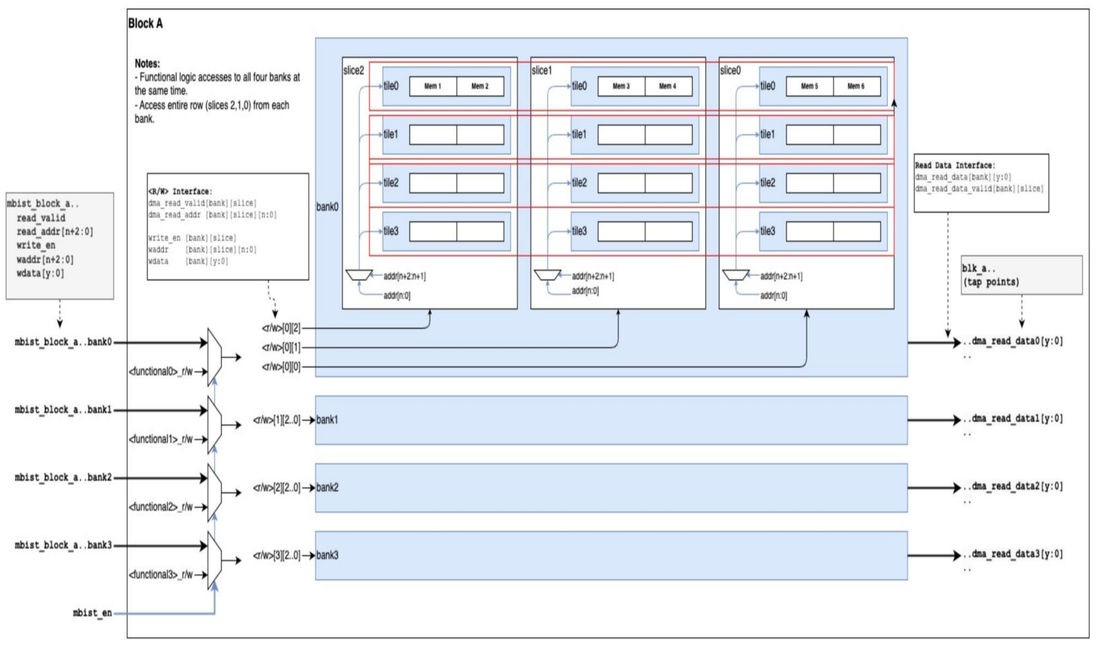
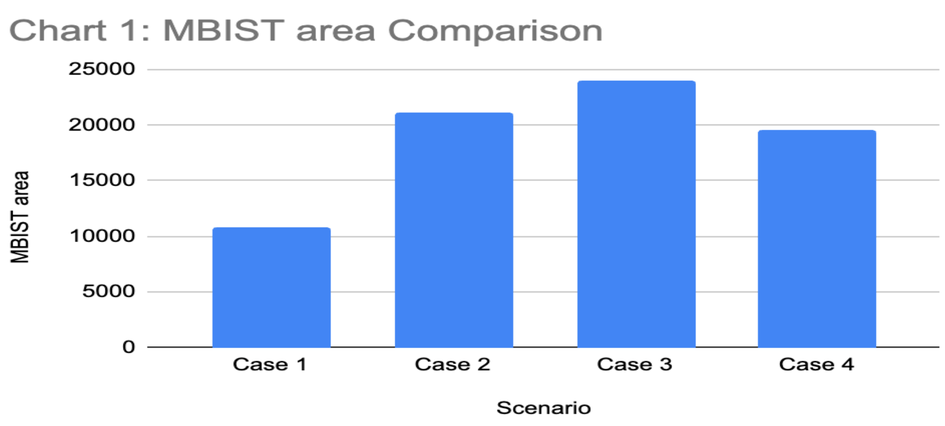
Introduction

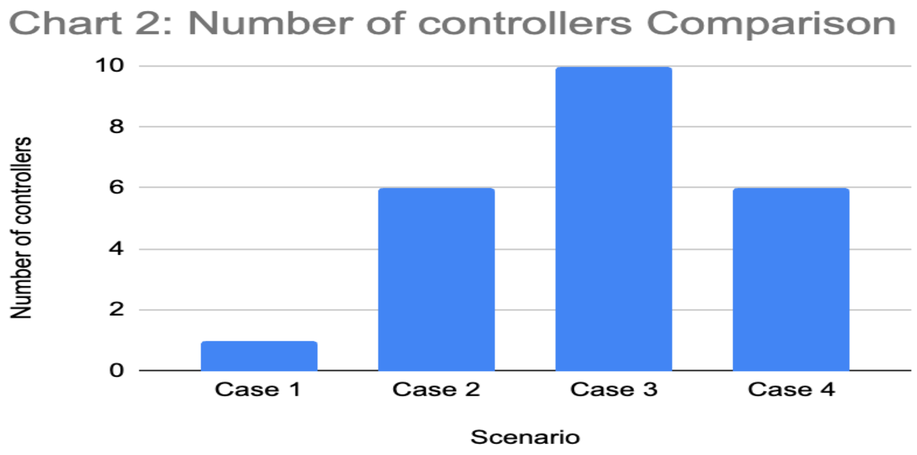
AI chips usually have many identical cores that can facilitate parallel computing requirements. The advanced memory dump feature integrated with memory test automation enables debugging of memory in functional mode and supports scalability when adding memories to a module.

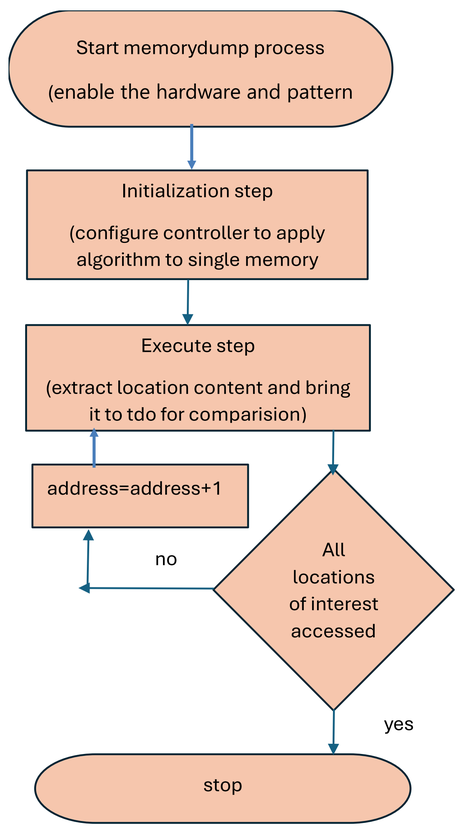


PROS	CONS
1) For Standalone MBIST Flow	
• Multiple physical memories had MBIST controllers which wrapped with BIST logic, enable early MBIST generation.	• Area overhead. • Created congestion for controller sharing. • Timing challenges for controller sharing.
2) Post Shared bus TMB Solution	
• timing friendly as its similar to func mode • No Routing congestion • Interface reuse	• Effort to understand the design • Integration effort as it is custom shared bus is high • Simulation debug effort is high for complex designs • whenever design changes(under the sharedbus interface),we have to regenerate the MBIST

Scenario	Mbist Area (reg count)	Number of controllers	Memories per controller step	no of steps	Routing congestion	Test time	Comparator type	Flow type
Case 1	10766	1	1	16(LM)	baseline	baseline	shared	SharedBus Flow
Case 2	21149	6	16	1	more than Case 1	1x Case1	local	Memwrap
Case 3	23997	10	10	1	more than Case 1	0.7x Case1	local	Memwrap
Case 4	19597	6	1	16	more than Case 1	1x Case1	shared	Memwrap







- Enables debugging of memory in functional mode
- Supports scalability when adding memories to a module
- Vital routing resources are saved
- Timing closure is eased
- Significant area reductions in the overall MBIST footprint
- Easier dump out of the contents of the arrays.

Conclusion

Automating the memory dump process through a shared bus architecture demonstrates significant benefits in terms of area efficiency, reliability enhancement, and test time reduction. The automated memory testing infrastructure on top of AI designs leads to optimal area savings. These improvements make this approach particularly attractive for various applications, especially in the realm of AI chip design where cost-effectiveness, streamlined processes, and ease of implementation are important critical factors.