ITC 2023 PO 40: Efficiency of packetized data delivery in 2.5D/3D designs

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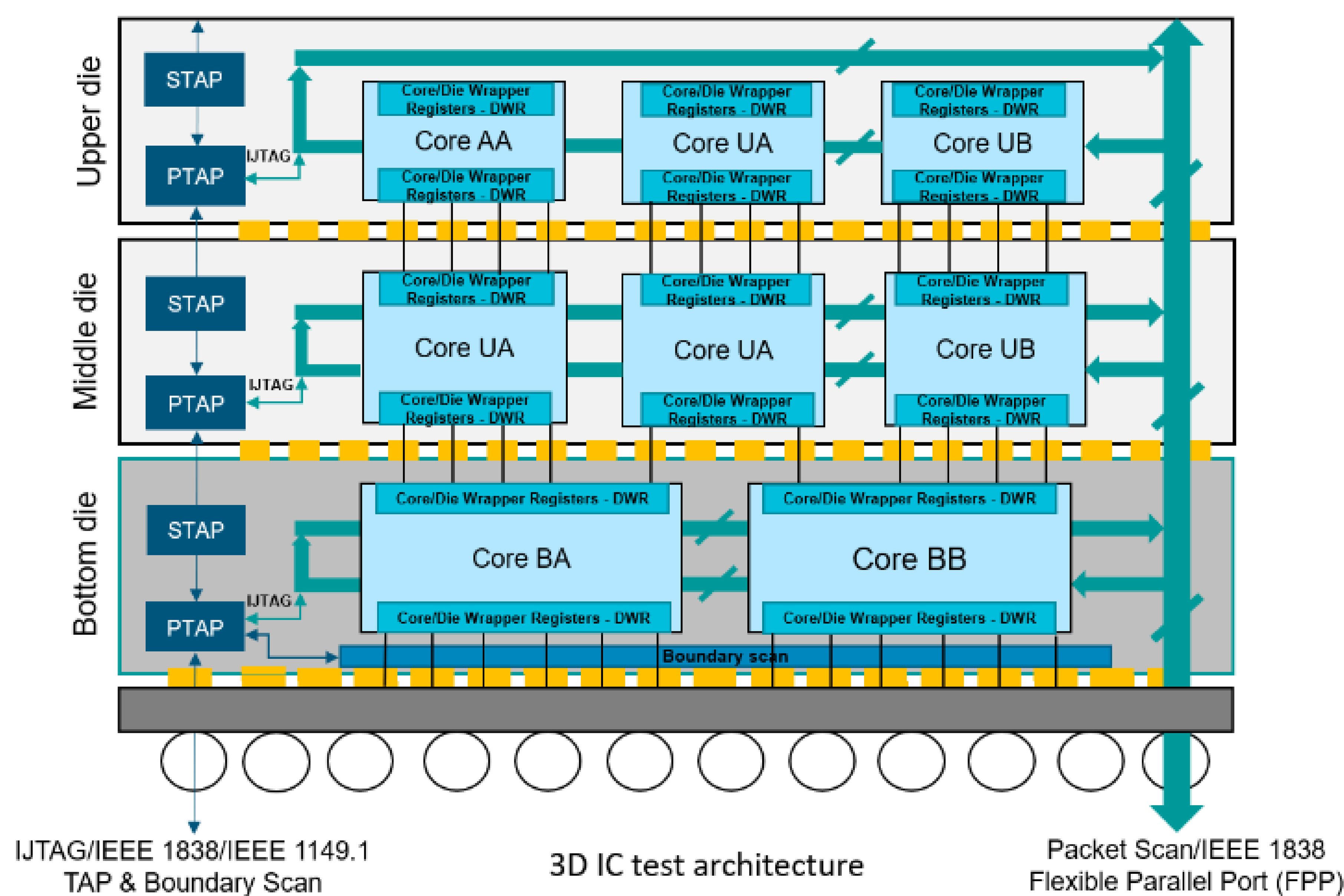
Abstract

With the growing complexity of Integrated Circuits (ICs), packetized scan data has shown to be a major component in test time reduction. With a packetized scan interface scan data is distributed to all cores concurrently. The optimization can include independent compression for all cores, resulting in an improvement in test time and pattern count reduction. Designs with 2.5D/3D architecture also benefit from parallel bus techniques as it simplifies the deployment of Design For Test (DFT) significantly.

Limitations without Flexible Parallel Port (FPP)

1. TAP access limits the scan bus to one bit
2. Low test clock (1149.1 TCK) frequency
3. High-effort routing and timing closure of test signals
4. No safety backup mechanism



3D IC test architecture

Benefits of the parallel bus

- Implementation of FPP that allows data packetizing for scan data delivery provides independent test signal sources for each die. This way cores within a die can be run concurrently while having a predictable, local timing to each core.
- Parallel access enables multiple-bit bus width. Combined with higher bus clock frequency the bus provides high throughput.
- Additional data delivery method makes the IJTAG access a backup mechanism in case the bus is inoperative

Possible test time reduction

Bus width	TAP/IJTAG access	FPP access
One bit	1x*	Nx**
M bits	1x (wider bus is forbidden)	(NxM)x

* Test clock without FPP acts as a reference clock

** N is calculated as the frequency ratio of the FPP bus clock to the 1149.1 test clock

Comparison between non-FPP and FPP design

Description	Without FPP	With FPP
Scan Delivery	Scan data shifted through TAP controllers and IJTAG network	Scan data shifted through the bus (IJTAG access as a backup mechanism)
Bus clocking	1149.1 test clock	Independent bus clock
Access to adjacent dies (2.5D)	In-series Test Access Ports (TAPs)	Mux-based parallel bus configuration for bypassing unused dies (TAPs as a backup)
Access to upper-level dies (3D)	In-series Primary TAPs (PTAPs) and Secondary TAPs (STAPs)	Direct access through the dies - mux-based configuration to access the internal die logic
Test signal management	Sourced from stack boundary and routed to all dies	Locally generated for each core inside each die
Compression logic	Pin-mux based configuration, dependent on the number of pins	Number of input/output channels independent from the number of pins, connected to FPP logic
Core dependency during tests	All cores dependent on shared global test signal sources	Cores run concurrently thanks to locally generated test signals

Die-level considerations

- With packetized data delivery the cores are encapsulated – changes in these cores are not visible from a die-level perspective
- Test signals don't span hierarchy boundaries. This simplifies routing at all levels

Summary

Packetized data delivery improves testability through parallel access. Utilizing locally generated signals allows easier timing analysis. Compliance with tile-based and multi-dimensional design makes it a dependable solution for these architectures.

References

[1] „IEEE Standard for Test Access Architecture for Three-Dimensional Stacked Integrated Circuits," in IEEE Std 1838-2019, vol., no., pp.1-73, 13 March 2020, doi: 10.1109/IEEESTD.2020.9036129.