Scalable bus in 2.5D / 3D Packaged Chips

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Introduction

2.5D and 3D integration of monolithic chiplets using different process nodes

- Challenges with concurrent core testing in a traditional pin-muxed scan-access design

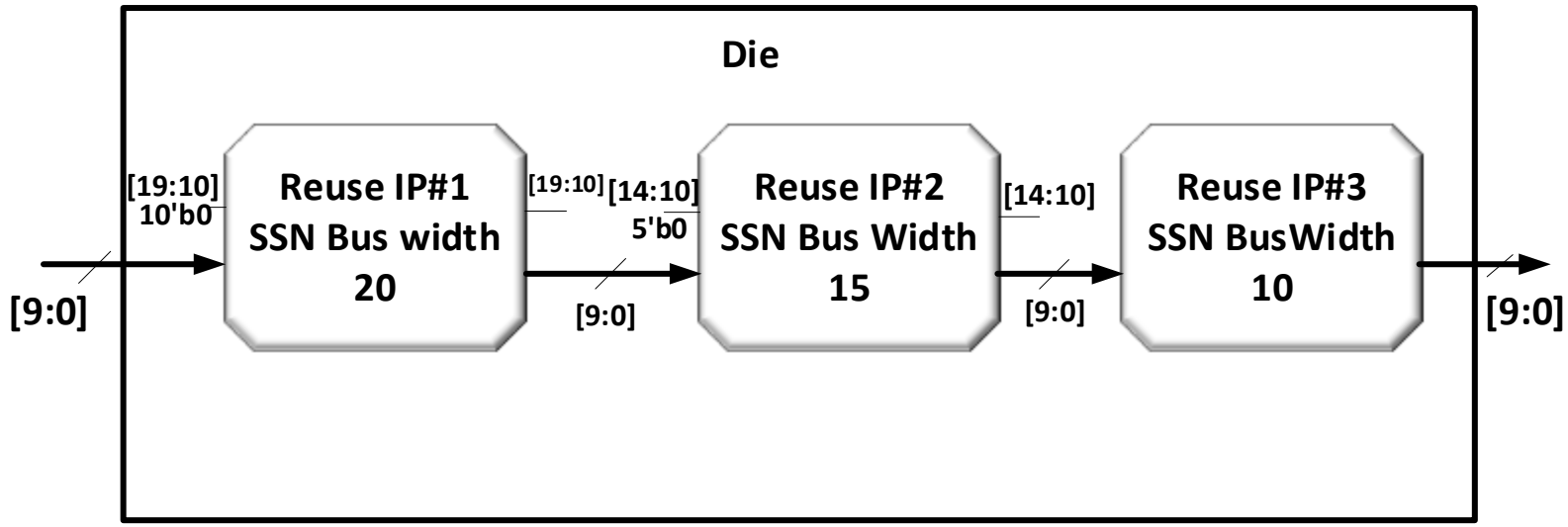
Suitability of Tessent Streaming Scan Network (SSN)

- Reuse of IPs and chiplets of multi-die devices
- SSN allows scalable bus width down to 1-bit

IP Core DFT Reuse

Tessent Streaming Scan Network (SSN) allows scalable bus width down to 1-bit

Same IP core can be re-used in different SOCs with varying SSN bus width implementation



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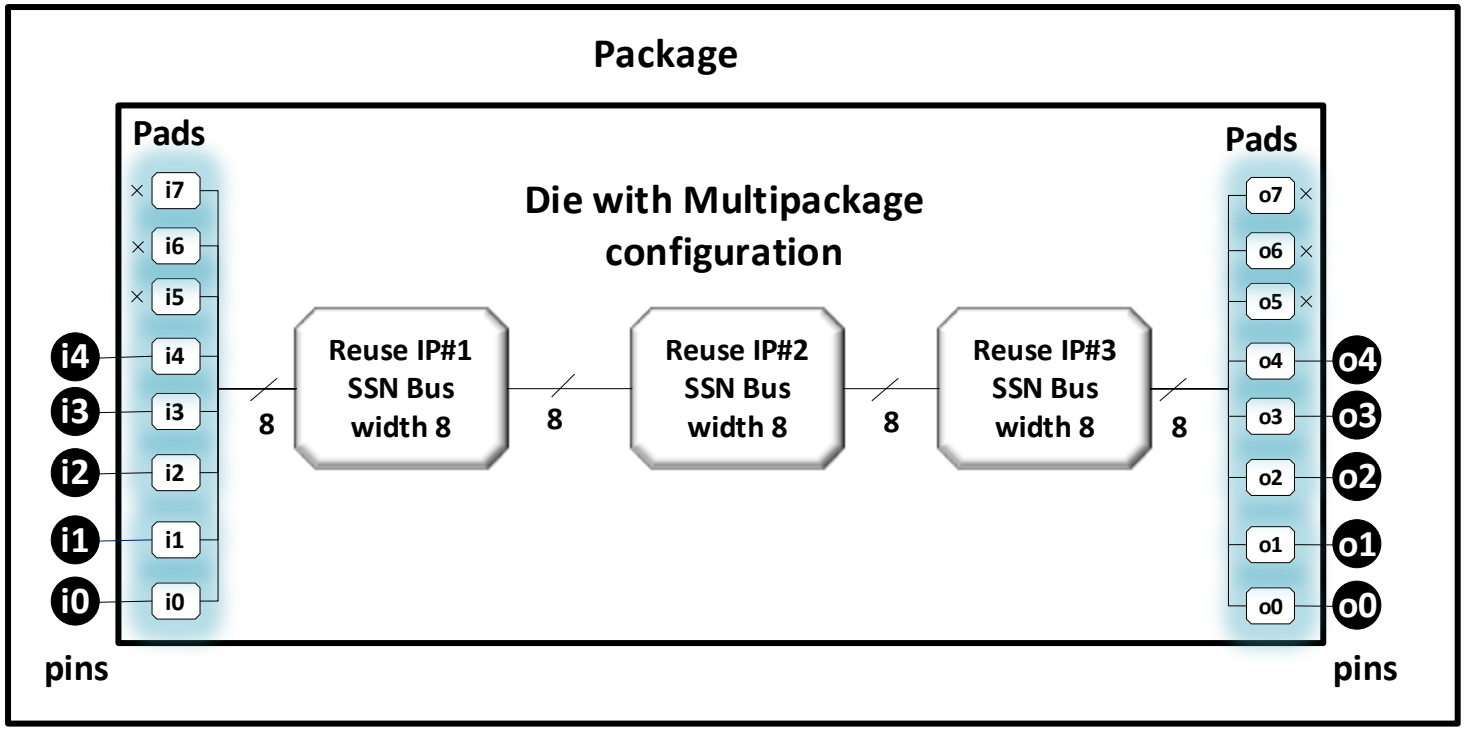
Die with Multi-Package Bonding Configuration

SOC / chiplet die with multi-package option bond different set of IOs depending on market needs

IOs fixed at die-level, package level IOs can be less or equal to die IOs



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Chiplet in Homogenous Package Integration

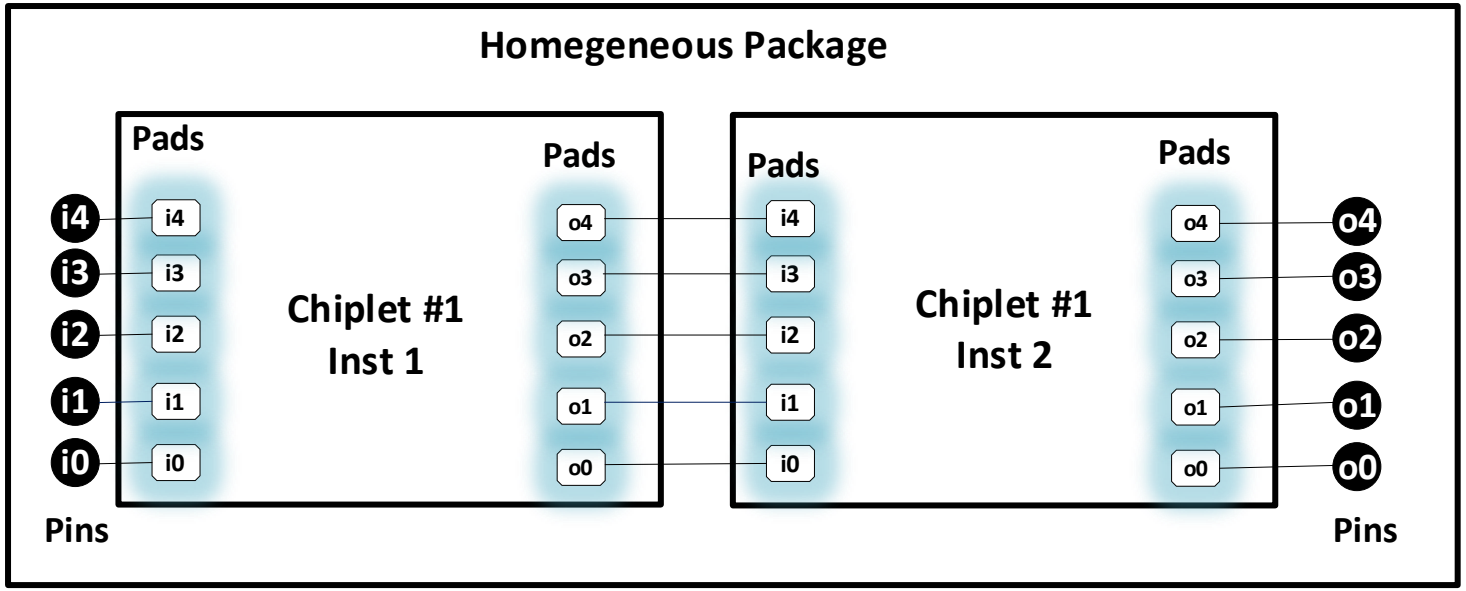
Chiplets with same or different modes or functionality designed and integrated by a single chip supplier

Chiplets may not be designed from start, reused from existing monolithic dies

IO availability and routing resources at package-level can be integrated with full or reduced bus-width

Pattern retargeting is only needed if package-level bus-width is smaller than the chiplet bus-width

Full test coverage is ensured without having to rearchitect the DFT for chiplets



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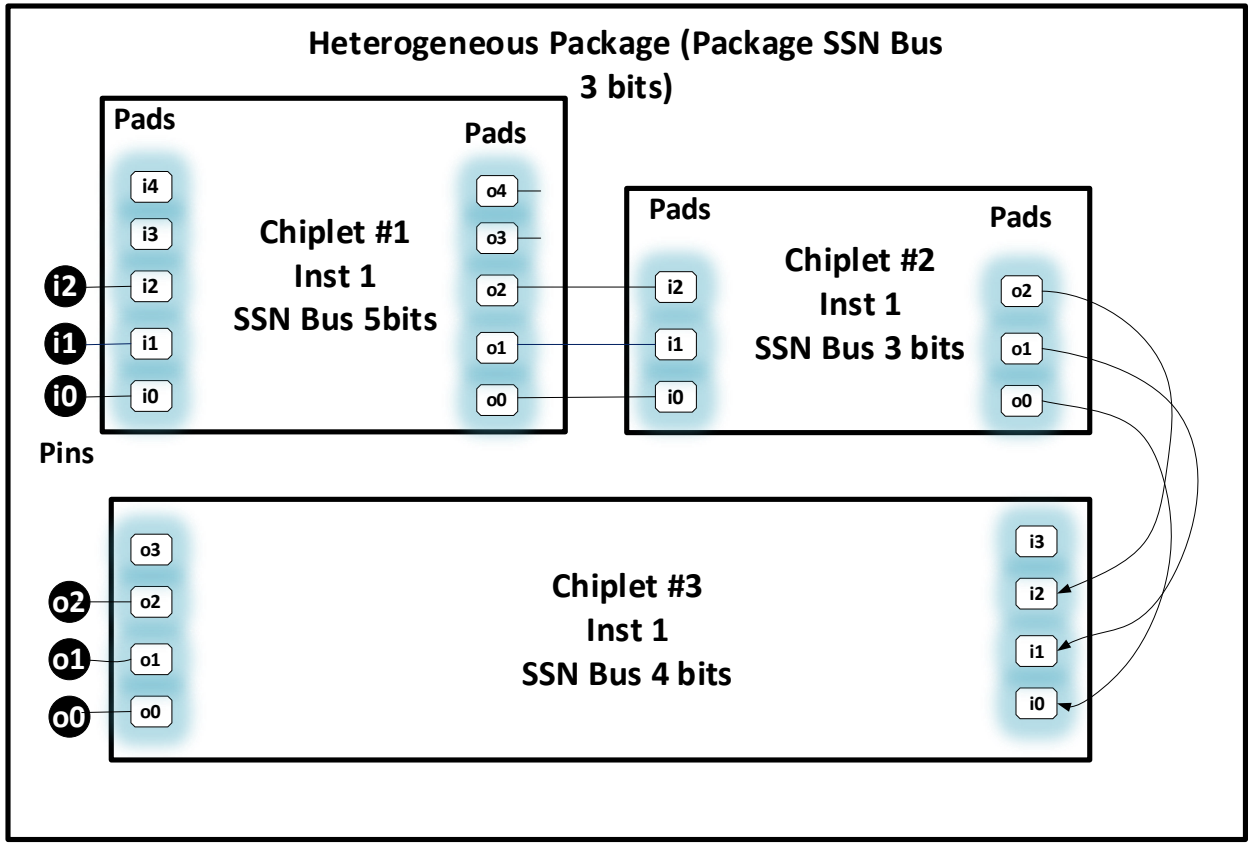
Chiplet Reuse in Heterogeneous Package Integration

Common to use chiplets from different vendors and different process nodes

Pin-limited packages, all IOs for test from chiplets may not be accessible

Chiplets with varying SSN bus-widths can be tested together

Combined test coverage at package-level not compromised



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Conclusion

With all flexibilities of a scalable bus at IP core level, chiplet, and package, SSN is ideal choice

Late design changes with reduced availability of package IO pins

Avoided DFT implementation changes which would have impacted chip schedule by up to few months