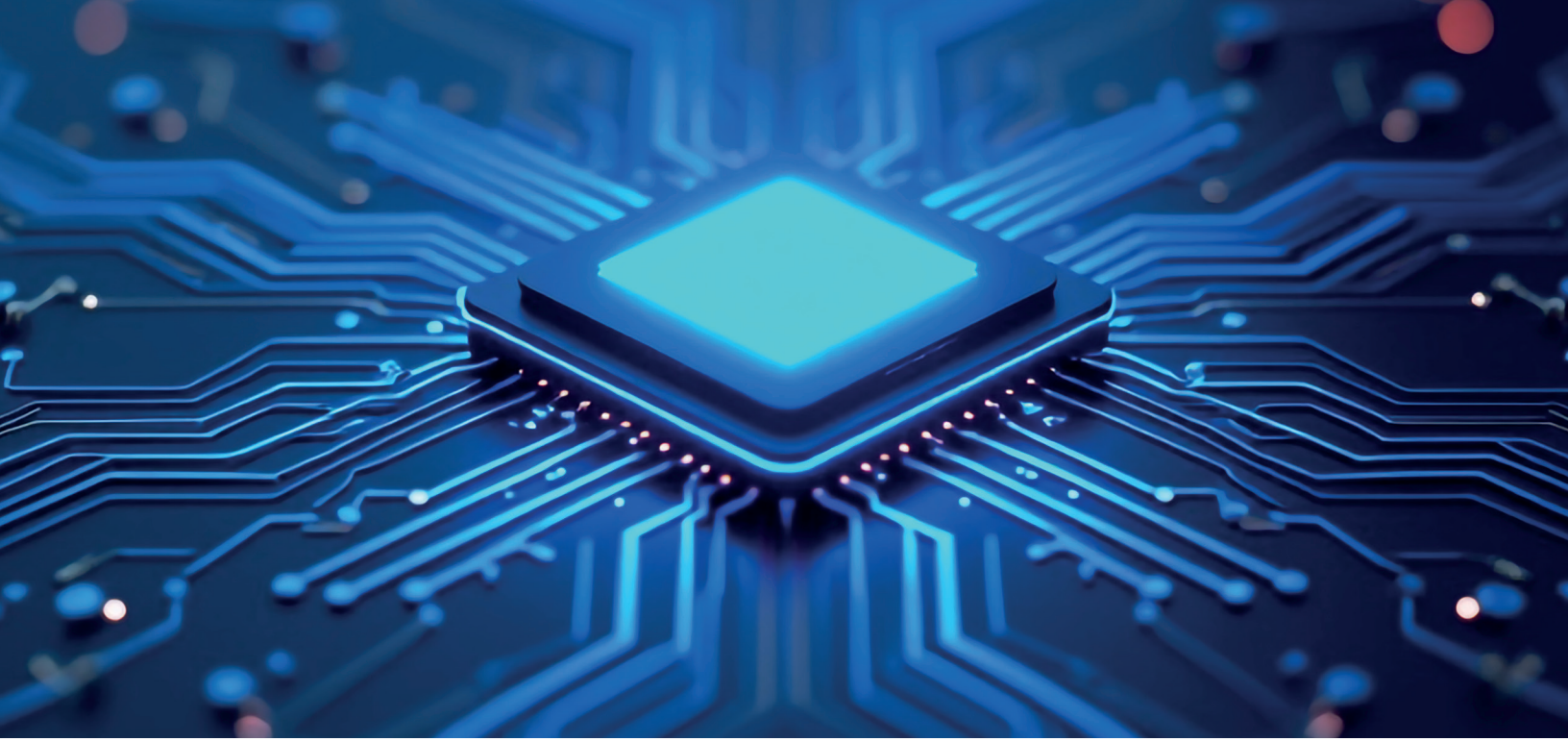


DIGITAL INDUSTRIES SOFTWARE

Tessent AnalogTest

Industry-first innovation for analog component testing

Benefits

- Cuts test pattern development time from months to days
- Provides higher test-coverage structural tests compared to conventional specification-based tests
- Shrinks test times to <1 ms for any AMS function, resulting in test time reductions of up to 100x and defect simulation time reductions of up to 100x
- Fully automates the test generation process, eliminating manual coding tasks
- Automatically verifies specification-based tests manually written in intuitive, P1687.2-based high-level PDL

Revolutionary Approach

Tessent™ AnalogTest software is a breakthrough IC test solution that fully automates pattern generation for analog components, similar to traditional ATPG methods for digital circuits. It represents a significant advance in analog circuit testing, offering automation and efficiency that were previously unavailable in the industry. This first-of-its-kind solution can reduce testing time by up to 100 times compared to traditional methods while providing superior test coverage.

This solution addresses one of the industry's most persistent challenges: the time-intensive nature of analog circuit testing. By automating the process and leveraging industry standards, it not only saves valuable development time but also improves the quality and reliability of test results. Tessent AnalogTest completes silicon tests 10-100x sooner than is possible with manual efforts, with a corresponding test cost saving. Its automated tests are generated sooner and simulate much faster than traditional methods, resulting in a significantly shorter time to market. Designers can achieve a high (>90%) P2427-based defect coverage for a block that can be verified in hours, fast enough to be verified before tape-out.

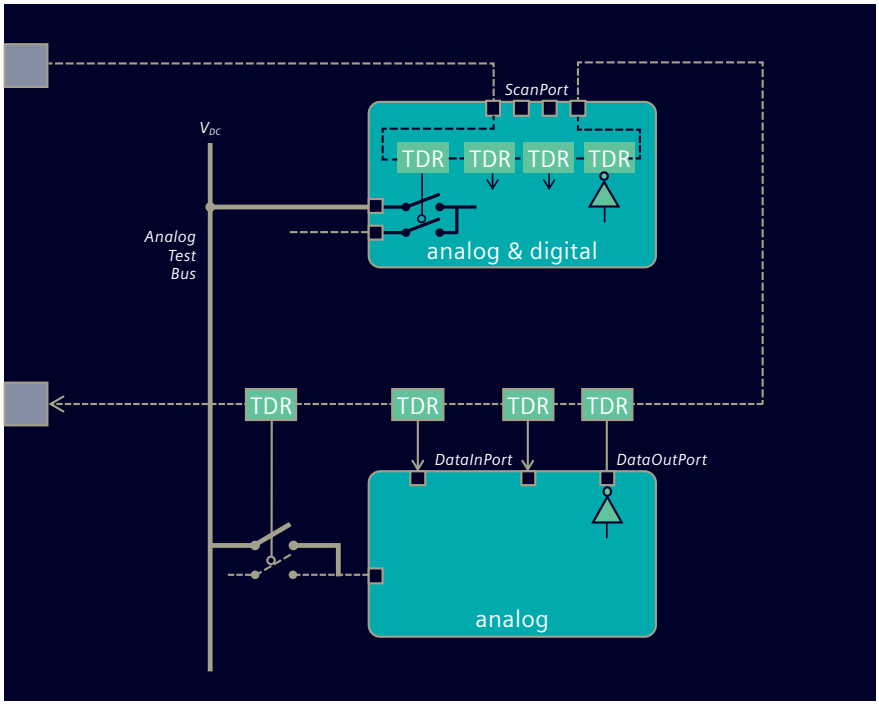
Benefits *continued*

- Enables simpler, quicker writing of error-free tests for manufacturing or functional safety
- Requires less expertise to write tests
- Proves testability before silicon tape-out
- Automatically generates test patterns for delivery by digital-only or mixed-signal DFT and ATE

Features

- Easy-to-use IJTAG-based workflow for DFT to simulation to testing, via graphical user interfaces, command line or user-written scripts
- Quickly simulated, block-level structural tests that achieve higher defect coverage than specification tests alone
- Standards-based methodologies for test pattern generation (IEEE P1687.2 and P2427)
- Leverages analog IJTAG (IEEE P1687.2) to simplify DFT, test creation and simulation

It generates high-coverage structural tests, quickly measures their effectiveness, and verifies specification tests, including tests with conditional branches such as trimming, that can augment (top-up) the coverage to achieve maximum test quality. It provides a direct and reusable IJTAG-based simulation-to-ATE flow.



Digital IJTAG infrastructure in which analog blocks appear as digital.

Tessent AnalogTest is the only commercial offering that uses established industry standards (IEEE P1687.2 and IEEE P2427), ensuring compatibility and reliability across the testing process. IEEE P1687.2 is an analog extension to the popular IJTAG standard that simplifies digital test creation.

An option to Tessent DefectSim Multi software, Tessent AnalogTest achieves provably higher test coverage than traditional specification tests while significantly reducing test development and application times. It enables post-silicon optimization of defect coverage or yield and facilitates extending automated defect diagnosis, widely used with scan-based tests of digital circuits, into analog domains.

Enables functional safety standards

Tests generated with AnalogTest can be verified using ISO 26262 functional safety metrics. Embedded scan tests for AMS effectively move test stimulus and response analysis closer to the hardware-under-test and can be encrypted for increased IP security. High-level, intuitive IEEE P1687.2 (“Analog IJTAG”) ICL & PDL languages are used for both verification and measurement of ISO 26262

functional safety metrics, providing a consistent, simulatable and effective automated test description. These IJTAG-based test descriptions directly lead to simulatable testbenches; the high-level PDL language describes the intended test sequences.

Easy interaction with digital DFT

The embedded scan test generated by Tessent AnalogTest presents AMS circuits as black-boxed IJTAG-ready scan-inserted digital blocks, which are more familiar to DFT Engineers. Tests are applied via the same IJTAG-based infrastructure used in many digital test implementations, allowing them to integrate easily with other digital-only DFT hardware.

Reduces test cost

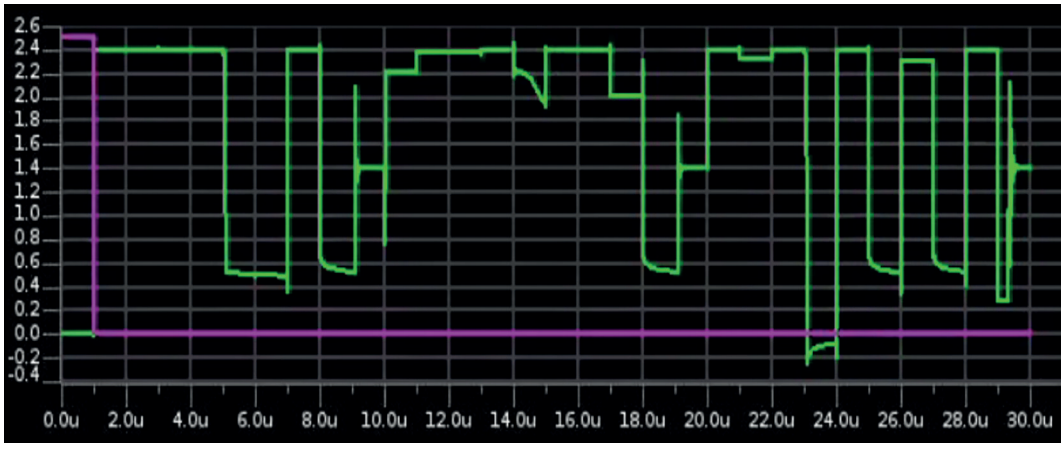
Traditional analog testing requires lengthy test times on expensive mixed-signal testers, with defect coverage that can be impractical to measure in simulation. Tessent AnalogTest automatically generates minimal-impact DFT circuitry and digital test patterns to test almost any analog circuit block in <1 ms on digital-only testers. The software provides comparable defect coverage in test times 10x-100x shorter than specification tests. Digital test patterns enable the use of digital-only ATE, allowing for the testing of more blocks and ICs in parallel, thereby further reducing test costs.

Increases engineering efficiency

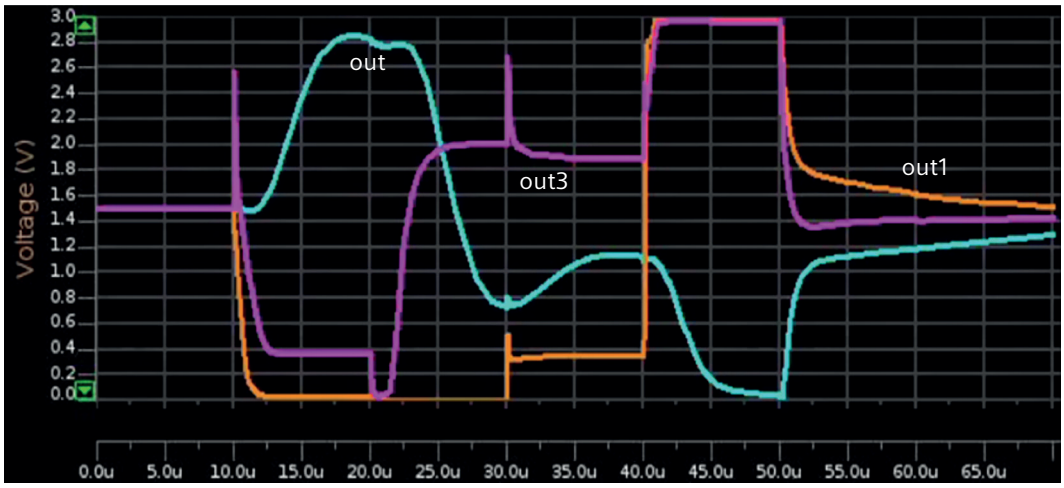
Tessent AnalogTest transforms analog DFT and test development from a tedious, months-long manual effort to a quick, automated process. Structural and specification tests can be verified in simulation before they are run on ATE or in-system, significantly reducing debug time and dependency on defect-free first silicon. It also verifies interactive tests such as those used for trimming.

Maximizes analog test coverage

Traditional specification testing of analog circuits can have inherently lower test coverage to minimize yield loss. And many analog (and digital) circuit modules in ICs have function-mode simulation times that are too long for defect (or fault) simulation to be practical. Digital scan-based DFT and ATPG can quickly simulate test patterns that achieve higher defect coverage without increasing yield loss.



A single analog output during an example scan test.



Structural test waveforms

60 µs

Multiple outputs being tested concurrently.

Product Family

Tessent offers comprehensive solutions for integrated circuit (IC) testing and functional monitoring. These include top-tier tools designed for testing optimization, data analytics, security, debugging and in-life monitoring. Our products ensure maximum test coverage, accelerate yield ramp-up and enhance quality and reliability throughout the silicon lifecycle.

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