ITC 2023 PO 41: Adaptive DFT technology in use with Automated Test Equipment (ATE)

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Abstract

Implementing Design for Test (DFT) techniques is a necessity to achieve high-quality chips. With the ever-growing complexity of designs, the effort to efficiently test these designs is also growing. Automated Test Equipment (ATE) performance is directly affected by Design Under Test (DUT) resources required for the test. There is a need for adaptive DFT technology that allows configuring the DUT setup to reflect the current condition of ATE.

Problems to consider

- Static programming
- No flexibility – test time improvement, decreased power dissipation, etc.
- Changes require pattern regeneration
- Inefficient use of resources for identical cores

Adapting to conditions on ATE

- ✓ Cores to retarget at time of retargeting
- ✓ Change core shift timing at time of retargeting
- ✓ Scale parallel bus down to single bit
- ✓ Reuse IJTAG interface as streaming interface

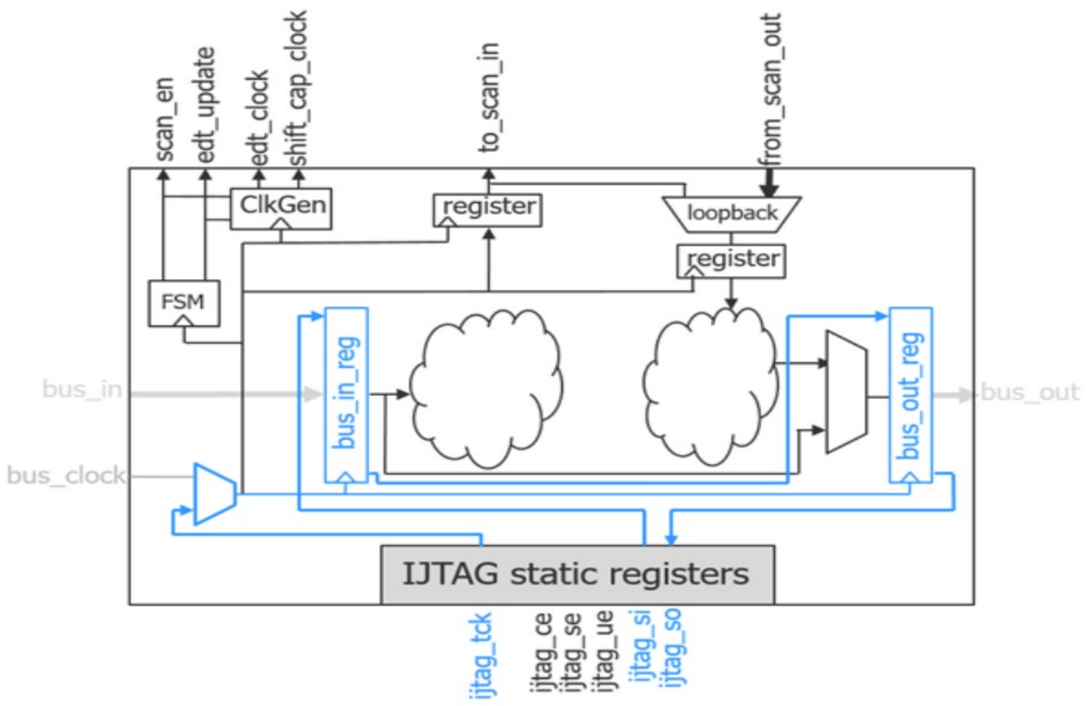

Fig.1 – Streaming through IJTAG

Not only for scan tests

- Support for Laser Voltage Imaging/Probing (LVI/LVP) and burn-in patterns
- Broadcast data to all scan chains or to a specific one
- Operation mode set with IJTAG protocol

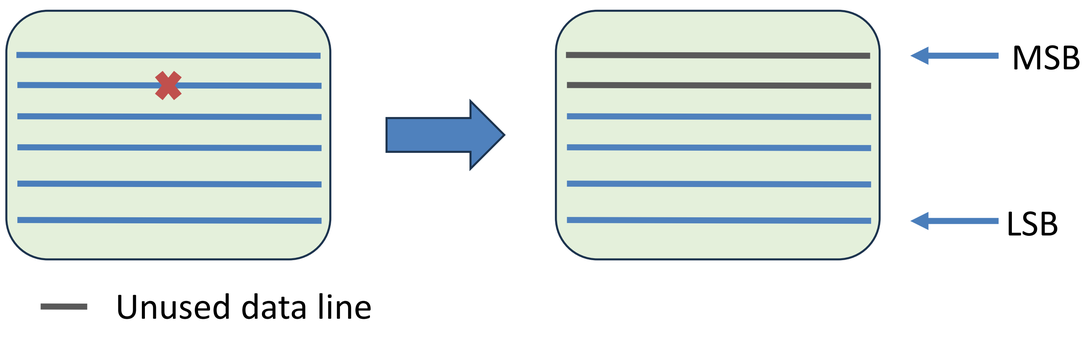

Fig.2 – Bus scaling

Using On-Chip Comparison

- ❖ Output scan data collected immediately through transmission protocol or stored internally with on-chip comparison logic
- ❖ On-chip compare re-test method enables efficient testing of identical cores
- ❖ Improved quality of failing cores diagnosis

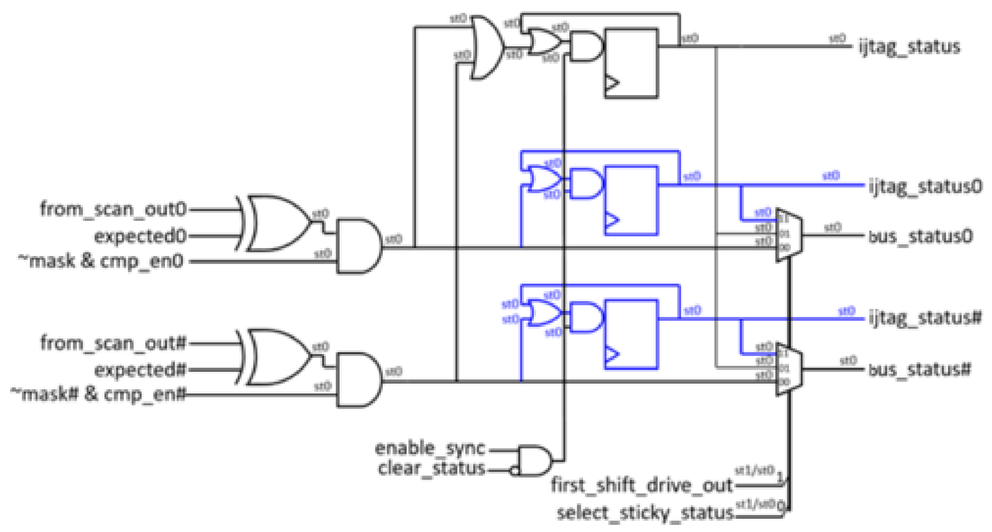

Fig.3 – On-chip comparison logic

Adaptive to design changes

- Plug-and-play design changes without affecting DFT architecture
- Full encapsulation of cores makes higher-level changes independent from lower-level cores
- Reusable patterns generated after design changes

Summary

Adaptive solutions improve the quality of testing by reusing the patterns by a parallel bus. On-the-fly changes in test configuration without changes in payload provide flexibility during test and diagnosis.

References

[1] JF Cote et al., Streaming Scan Network (SSN): An Efficient Packetized Data Network for Testing of Complex SoCs, 2020 IEEE International Test Conference (ITC)