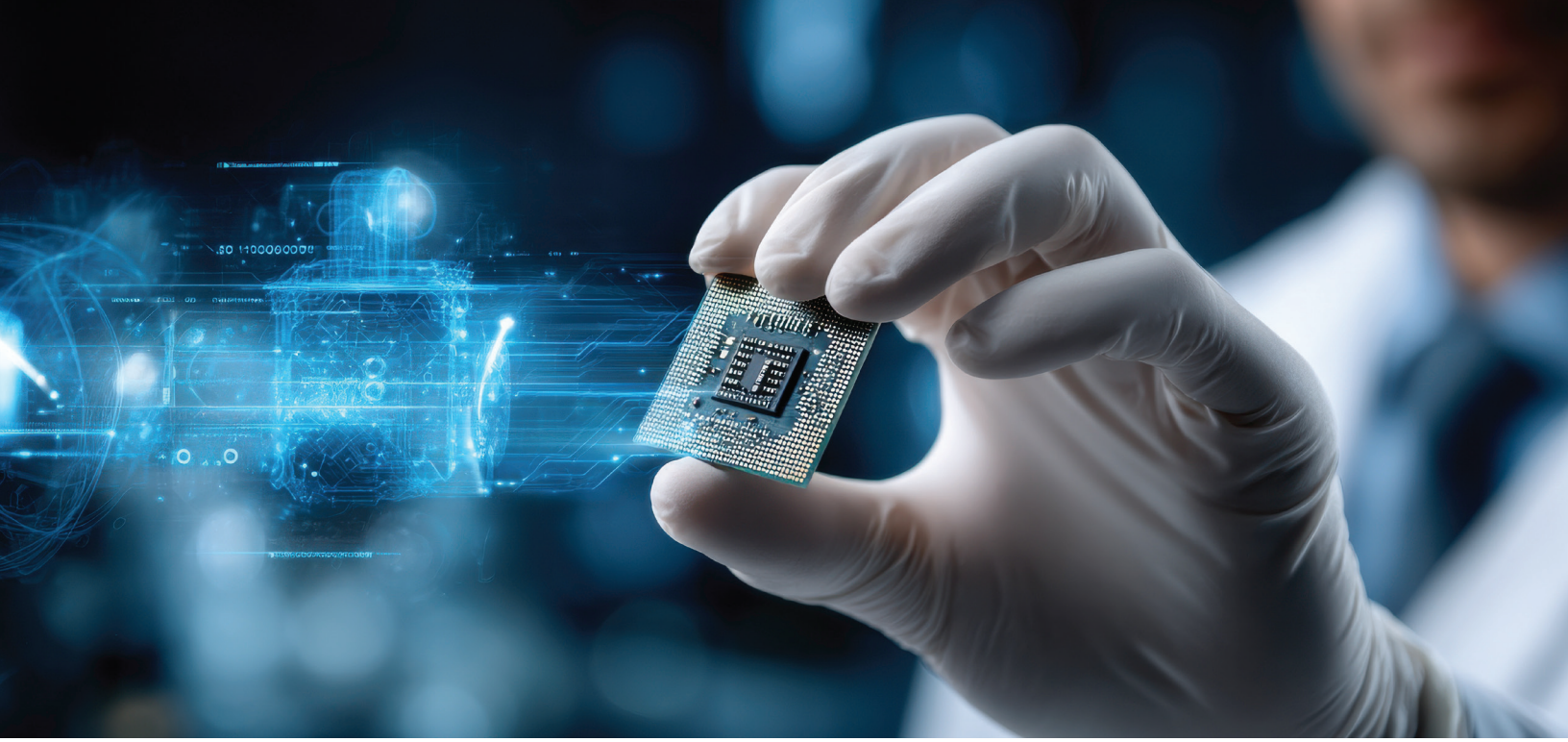


DIGITAL INDUSTRIES SOFTWARE

Tessent IJTAG Pro

Accelerating test and validation for next-generation designs

Benefits

- Reduces manufacturing, test and diagnosis costs by accelerating the time-consuming loading and unloading of IJTAG pattern data
- Expedites test setup time using a high-speed parallel bus
- Maximizes return on investment through optimized, production-proven Tessent infrastructure
- Future-proofs testing strategy by addressing the escalating test pattern counts and complexity of advanced 2.5D and 3D designs
- Enables uniform access and use of embedded IP independent of the IP source
- Expands available embedded IP choices

Enhanced productivity with Tessent IJTAG Pro

Tessent IJTAG Pro elevates the standard set by Tessent IJTAG, offering all its features while introducing groundbreaking enhancements for higher bandwidth applications. This state-of-the-art solution is designed to revolutionize the use of IJTAG patterns and generic data streaming. By transforming traditional serial IJTAG operations into high-speed parallel processes, it significantly boosts efficiency. Additionally, Tessent IJTAG Pro expands the functionality of IJTAG by allowing read and write access to custom hardware. The seamless integration of these new capabilities within the production-proven Tessent platform makes it a comprehensive and user-friendly solution.

Reducing test time and cost

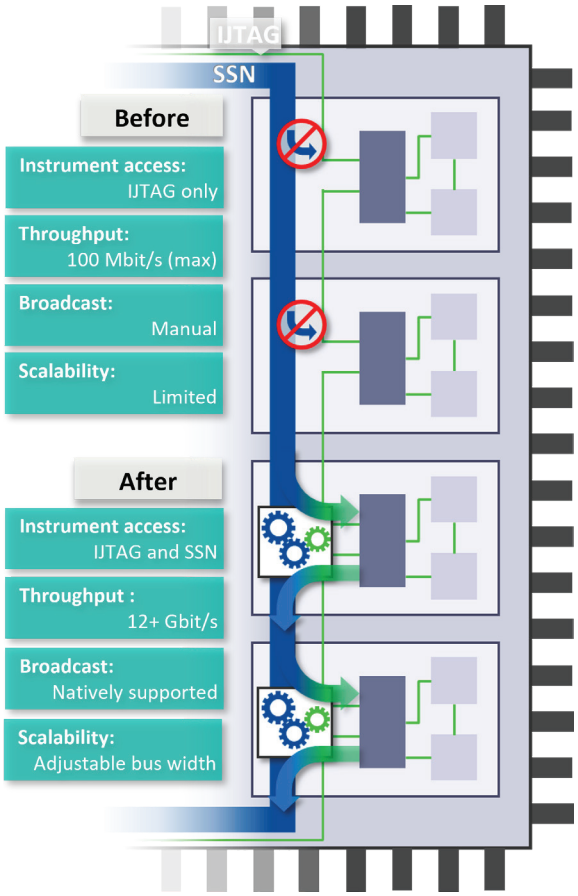
Revolutionizing test efficiency, Tessent IJTAG Pro utilizes the Tessent™ Streaming Scan Network (SSN) architecture to convert traditional serial IJTAG operations into high-bandwidth parallel processes, an industry first. Tessent SSN uses a symmetric bus architecture for scan automatic test pattern generation (ATPG) pattern delivery. Parallel processing helps reduce test setup application time while providing high-bandwidth IJTAG and generic data streaming (GDS). The GDS functionality extends the Tessent SSN bus by enabling the transmission of custom data to various generic instruments throughout the design hierarchy.

Features

- High-bandwidth IJTAG
  - Complements the traditional serial TDI/TDO path using the IEEE 1687 / 1149.1 TAP (Test Access Port) with a significantly faster data transfer method
  - Enables simultaneous loading and unloading of IJTAG (IEEE 1687) network sections via the Tessent SSN bus at the SSN bus clock frequency
- Generic data streaming
  - Extends the Tessent SSN bus to provide read and write access to custom generic nodes and instruments
  - Allows users to supply custom data via the parallel bus for applications, including loading firmware and RAM resident test
- Integration with existing test flows
  - High-bandwidth IJTAG patterns can be applied efficiently before running other test applications such as Scan ATPG, Memory BIST, Logic BIST and In-System Test patterns
- Validated performance
  - Effectiveness proven through successful silicon implementation

Benefits *continued*

- Reduces design schedules by accelerating integration of IEEE 1687-compliant IP
- Achieves minimum cycle count for accessing IP within a reconfigurable network
- Provides a common integration flow and access network for Tessent IP and any third-party IEEE 1687-compliant IP
- Comprehensive IJTAG debug and visualization capabilities leveraging Tessent Visualizer



High bandwidth IJTAG over Tessent SSN.

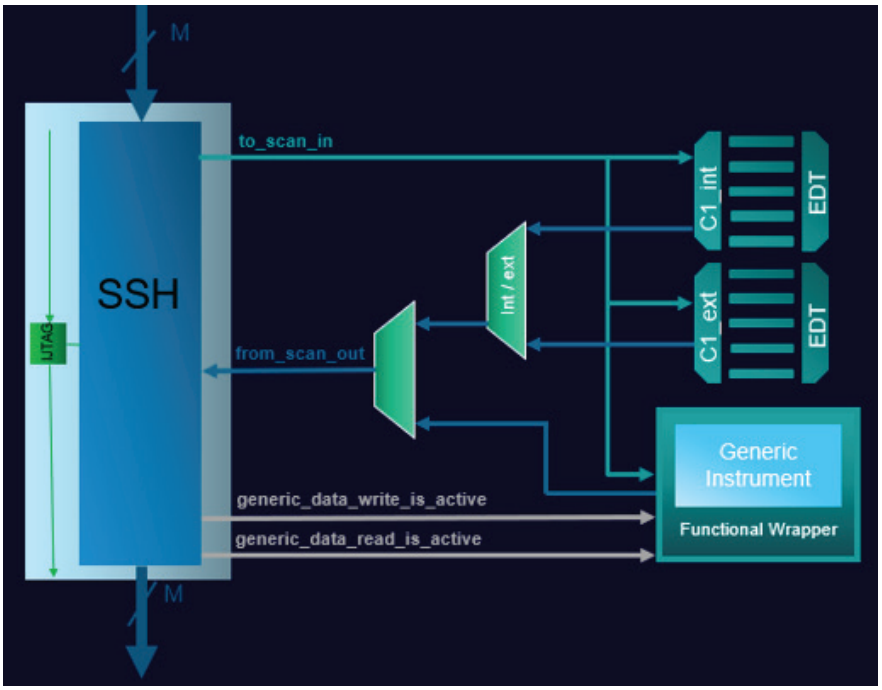
Addressing transistor density

As the semiconductor industry witnesses an explosion in transistor density, designs are rapidly evolving from 2D to advanced 2.5D and 3D architectures. This progress, however, has exponentially multiplied design testing challenges: we face soaring test pattern counts, extended pattern application times, escalating Automatic Test Equipment (ATE) costs and a shrinking number of accessible test pins. In this demanding landscape, optimizing existing infrastructure for efficient, scalable test solutions is not just crucial—it's essential for sustained competitiveness.

Tessent IJTAG Pro significantly reduces both test time and cost for complex 2D, 2.5D and 3D IC designs. A key factor in these savings is the accelerated loading and unloading of IJTAG pattern data, a notoriously time-consuming task. This has traditionally been accomplished using a serial TDI/TDO path with an IEEE 1149.1 Test Access Port (TAP) controller. The Tessent SSN bus broadens the utility of IJTAG patterns, enabling their use in other essential test applications such as Memory BIST, Logic BIST and In-System Test. As designs evolve into 3D ICs, these substantial test cost reductions apply across each chiplet and the entire package.

Features *continued*

- Includes all Tessent IJTAG capabilities:
- Finds and extracts IJTAG ICL network data from gate-level or RTL netlist
- Flexible IEEE 1687 network creation and insertion
- Provides access to IEEE 1687 data structures, attributes and parameters
- Retargets PDL commands from the IP boundary to any point within an ICL-described IEEE 1687 network
- Generates Verilog testbenches for PDL verification
- Translates chip-level PDL patterns to ATE pattern formats (STIL, WGL)
- Includes advanced introspection and design editing capabilities through Tessent Platform
- Visualization of the extracted ICL model



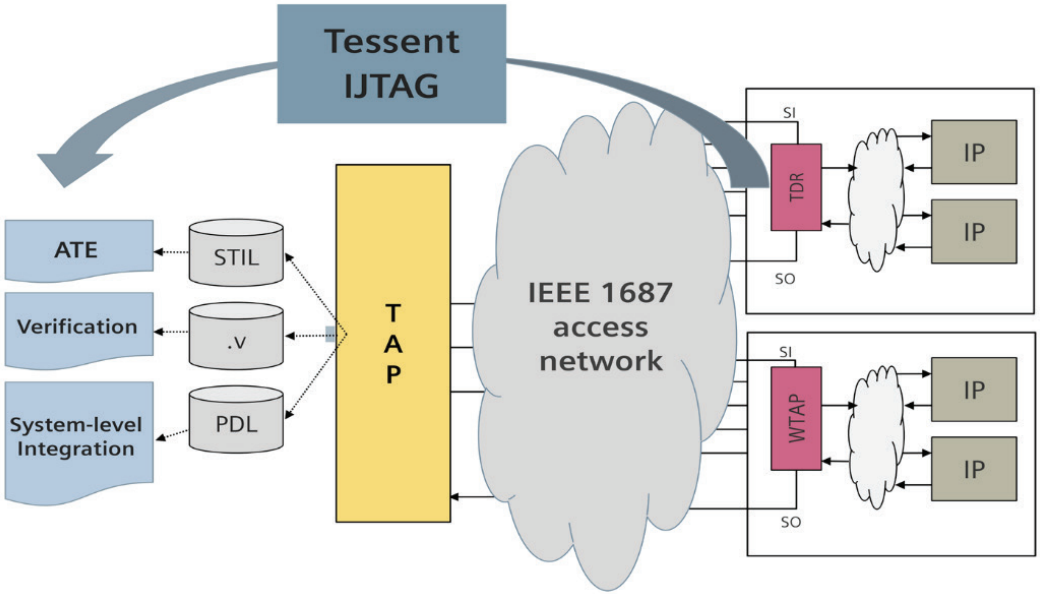
Generic instrument and EDT connected to a Tessent SSN ScanHost

Building on a solid foundation

Tessent has long provided automation of the IEEE 1687 standard through its IJTAG software. Tessent IJTAG delivers comprehensive automation support for implementing and debugging the standard, providing plug-and-play intellectual property (IP) test and instrumentation integration. IP providers use it to ensure compliance, and chip designers use it to efficiently integrate IEEE 1687-compliant IP from various sources into their designs.

Tessent IJTAG can be used to create simulation testbenches that verify the Instrument Connectivity Language (ICL) against the IP's Verilog description. It can convert PDL routines into Verilog for verification against the IP's ICL description using automatically generated simulation testbenches.

Tessent IJTAG Pro



Product Family

Tessent offers comprehensive solutions for integrated circuit (IC) testing and functional monitoring. These include top-tier tools designed for testing optimization, data analytics, security, debugging and in-life monitoring. Our products ensure maximum test coverage, accelerate yield ramp-up and enhance quality and reliability throughout the silicon lifecycle.

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