Renesas' Strategy to apply Tessent MemoryBIST Soft Programmable

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SOLUTION OFFERINGS

Our mission is to develop a safer, healthier, greener, and smarter world by providing intelligence to our four focus growth segments: Automotive, Industrial, Infrastructure, and IoT that are all vital to our daily lives, meaning our products and solutions are embedded everywhere.

Automotive

Highly reliable vehicle control, safe and secure autonomous driving, Eco-friendly electric vehicles

Industrial

Lean, flexible and smart industry

Infrastructure

Robust infrastructure, enabling safety and efficiency

IoT

Comfortable, safe and healthy lifestyles through IoT

BACKGROUND

- There are cases which new algorithm is required for quality unstable memory under new process and miniaturization.
- When new algorithm is required for a detected memory fail, it is not possible to add it as hard logic since the MBIST implementation has already been completed.
- Tessent MemoryBIST has soft programmable algorithm function.

  But it didn't have a soft operation set function to control memory enable signals.
- In this time, Tessent MemoryBIST provides complete soft programmable function.

  So, we evaluated this to determine product applicability.

Tessent MemoryBIST Hard Programmable

- **Tessent MemoryBIST has two methods as the implementation for MBIST algorithms.**
  - **Hard programmable**
  - **Soft programable (Next page.)**

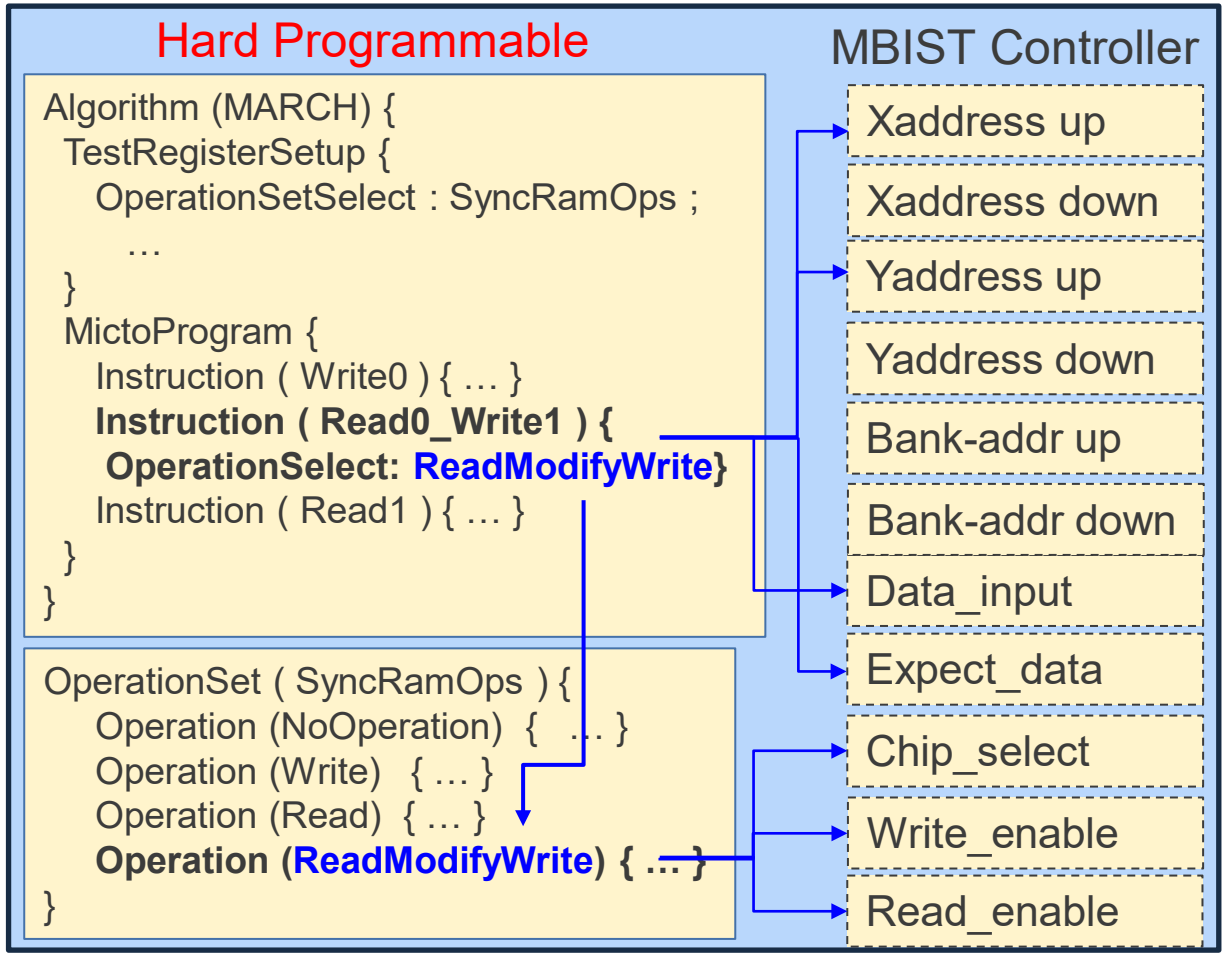
- **Hard programmable**

✓ **Main use : mass production test**

✓ **Implement the algorithms as hard logic.**

✓ **For Mass production pattern**

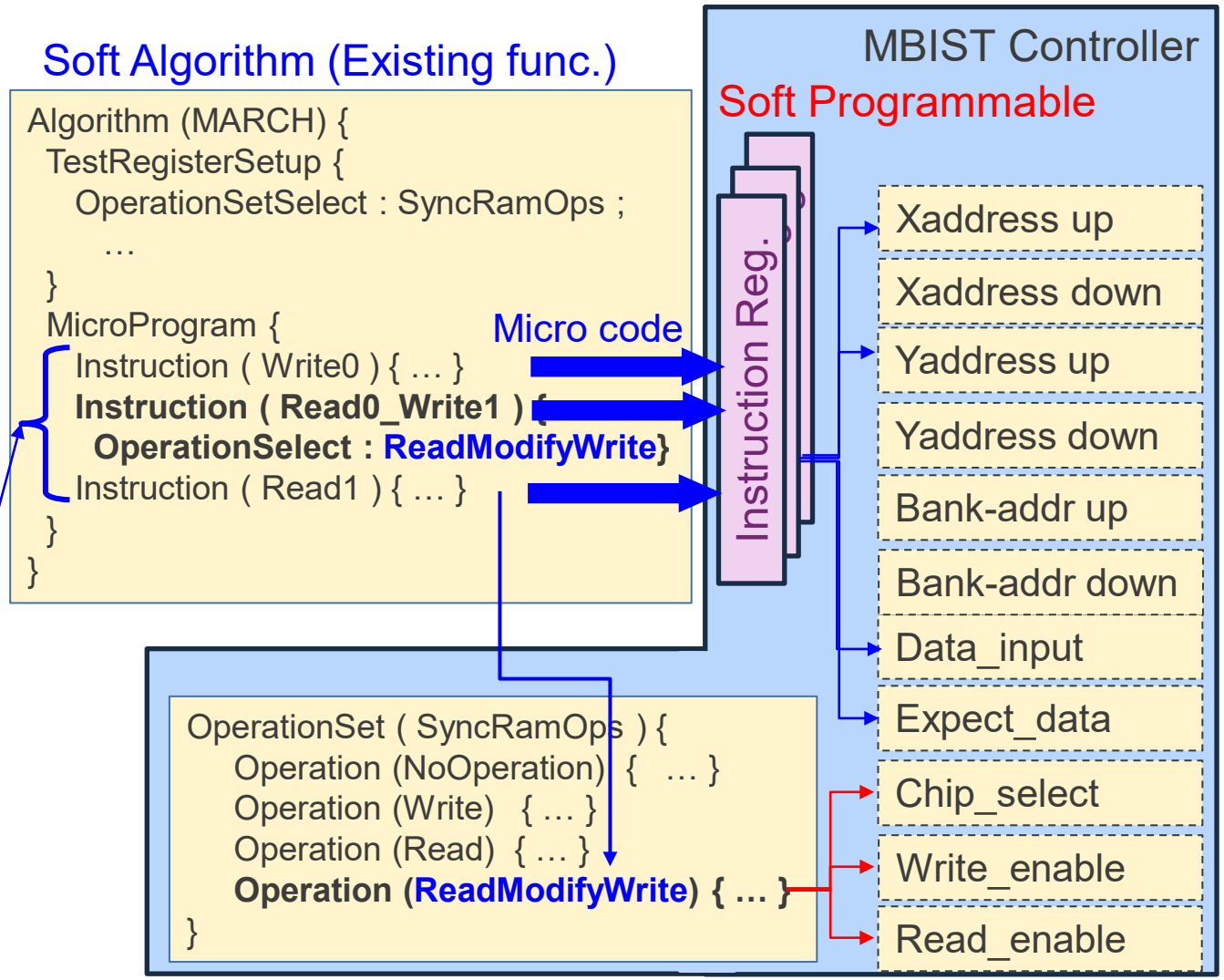
✓ **For using memory fail analysis in past**



Tessent MemoryBIST Soft Programmable Algorithms

- **Soft Programable Algorithm (Existing func.)**
  - ✓ **Main use : Memory Fail analysis**
  - ✓ **Can add new algorithm after implementation**
  - ✓ **However, the algorithms with OperationSet implemented as Hard logic.**

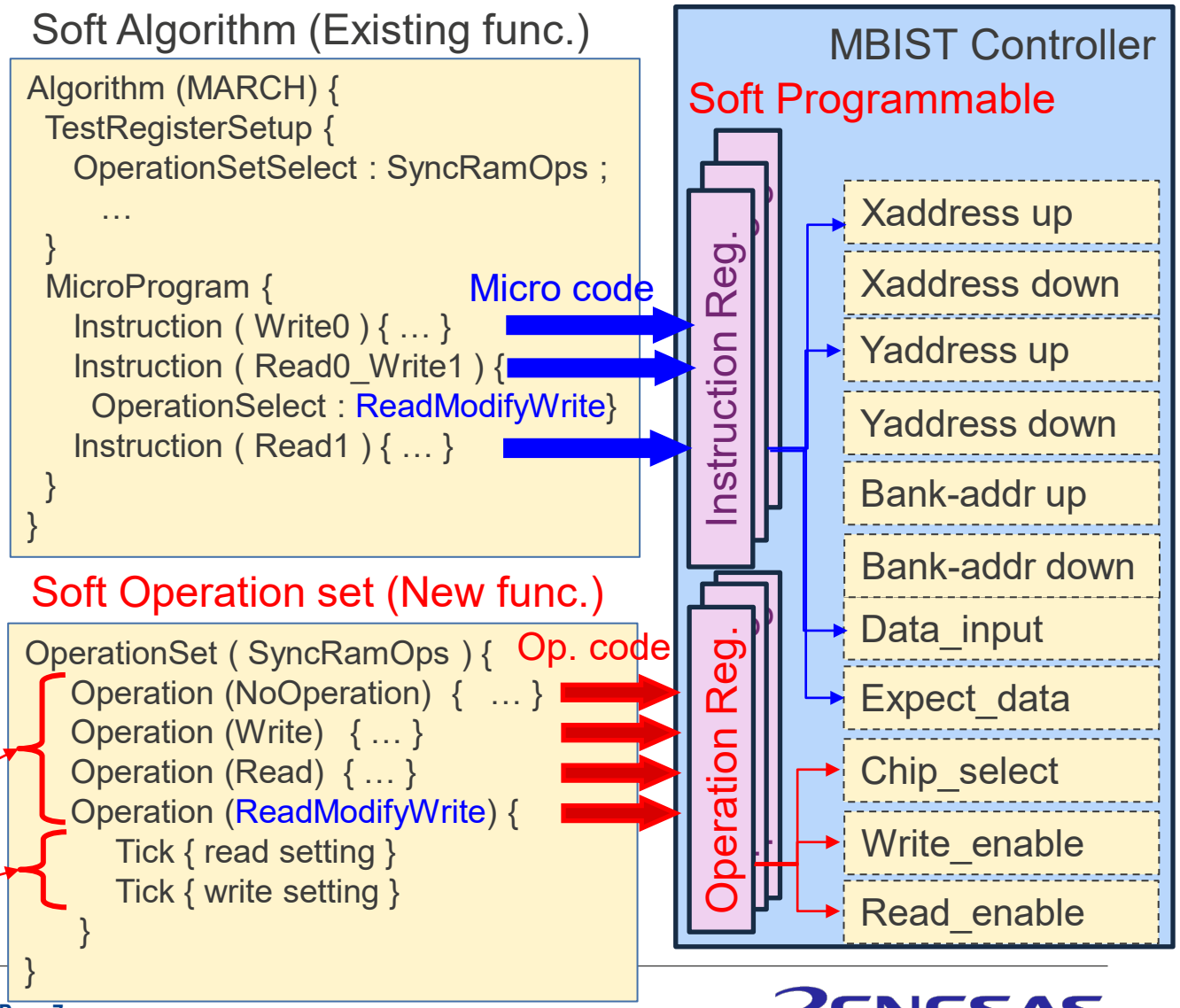
    ➔ Cannot add new enable control pattern which isn't defined in OperationSet.
  - ✓ **Must prepare instruction reg. for using soft algorithm**
    - **Specify with "soft_instruction_count" parameter**
    - **Renesas strategy : prepare it for three instructions**



SOLUTION : New function Soft Programmable Operation set

Want to test memory / fail analysis greater flexibility in post-silicon.

- **Soft Programmable Operation set (New func.)**
  - ✓ **Main use : Memory Fail analysis**
  - ✓ **Can add new algorithm including operation set after implementation**
  - ✓ **Must prepare operation reg. for using soft algorithm**
    - ✓ **Specify the following parameters**
      - – **“soft_operation_count” parameter**
      - – **“soft_operation_length” parameter**



EVALUATION for Soft Programable operation set function

For greater flexible memory test / fail analysis in post-silicon.

New Soft Programmable Operation set function need to add the registers for storing micro codes.

Therefore, it becomes a trade-off between quality (algorithm flexibility) and MBIST area.

◆ Evaluate the MBIST area impact for applying Soft Programmable Operation set.

- Assume that the allowable area increase range is 10%

  (Although the actual conditions depend on the product specifications.)

EVALUATION & RESULT (1)

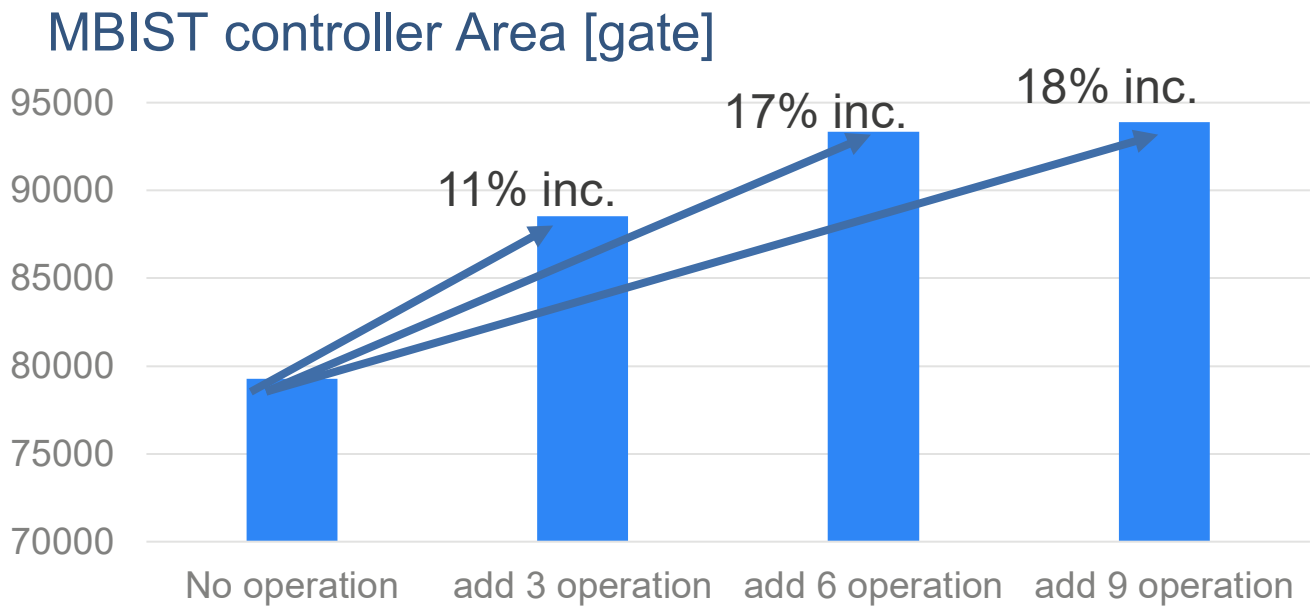
- ✓ **Check an area increase rate when changing the number of "soft_operation_count"**
  - **"soft_operation_count" parameter : 3 ➔ 6 ➔ 9**

➔ **By preparing more operations, the setting of enable signals can be made flexibly.**

- **Target 1 controller of ASIC product : with 16 Mem-IF (including {Max 1024word x 16bit})**

soft_operation_count	Area [0.63/gate]
No use	79,292 [gate]
3 operation	88,540 [gate]
6 operation	93,356 [gate]
9 operation	93,895 [gate]

(soft_instruction_count = 13)
(soft_operation_length = 2)



➔**The impact on MBIST area becomes heavy, over 10%, when setting 3 operations or more.**

EVALUATION & RESULT (2)

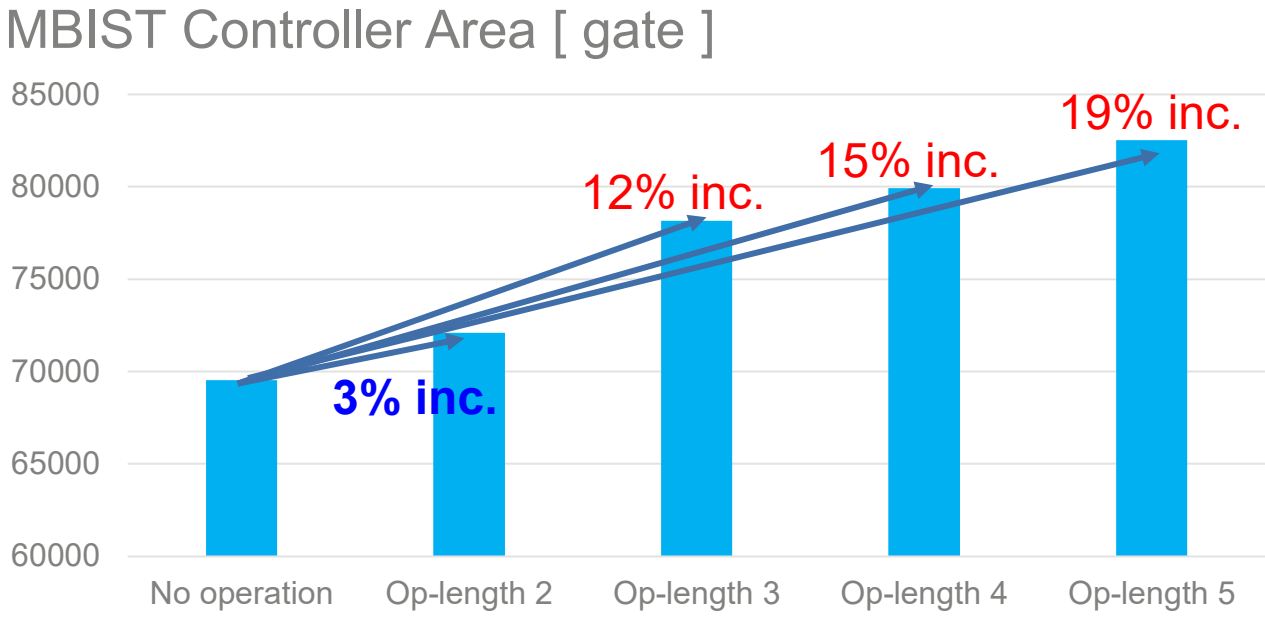
- ✓ **Check an area increase rate when changing the number of "soft_operation_length"**
  - **"soft_operation_length" parameter : 2 ➔ 3 ➔ 4 ➔ 5**

➔ By preparing more length, Allows more operations for one address.

- **Target 1 controller of ASIC product : with 16 Mem-IF (including {Max 1024word x 16bit})**

soft_operation_length	Area [0.63/gate]
No use	69,532 [gate]
Operation length 2	72,103 [gate]
Operation length 3	78,171 [gate]
Operation length 4	79,917 [gate]
Operation length 5	82,511 [gate]

(soft_instruction_count = 3)
(soft_operation_count = 3)



➔ The impact on MBIST area becomes heavy, when setting 3 length or more per 1 operation.

CONCLUSION

◆ Evaluation result :

- Based on 10% area increase, can apply the soft operation set with the following setting.
  - ✓ The number of **operation is 3** and the number of **operation length is 2**.

➔ We can use this function as follows under the above setting.

- **Can test with more flexible enable control.**
- **Complex algorithms that use many operations** become **trade-off with area increase**.

➔ If the product specifications allow for a MBIST area increase, we consider to implement soft programmable under the following purpose.

- ✓ Aiming for 100% cause identification in failure analysis.

◆ Expectation for Siemens EDA

- Reduce an area for soft programmable, especially for operation length.

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