

# Renesas' Shift Left with Design-for-Test Using Tessent® RTL TPI

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Hiroyuki Iwata  
Digital Design Technology Department  
Renesas Electronics Corporation

# About Renesas Electronics Corporation

Our mission is to develop a safer, healthier, greener, and smarter world by providing intelligence to our four focus growth segments: Automotive, Industrial, Infrastructure, and IoT that are all vital to our daily lives, meaning our products and solutions are embedded everywhere.



Automotive

Highly reliable vehicle control,  
safe and secure  
autonomous driving,  
Eco-friendly electric vehicles



Industrial

Lean, flexible and  
smart industry



Infrastructure

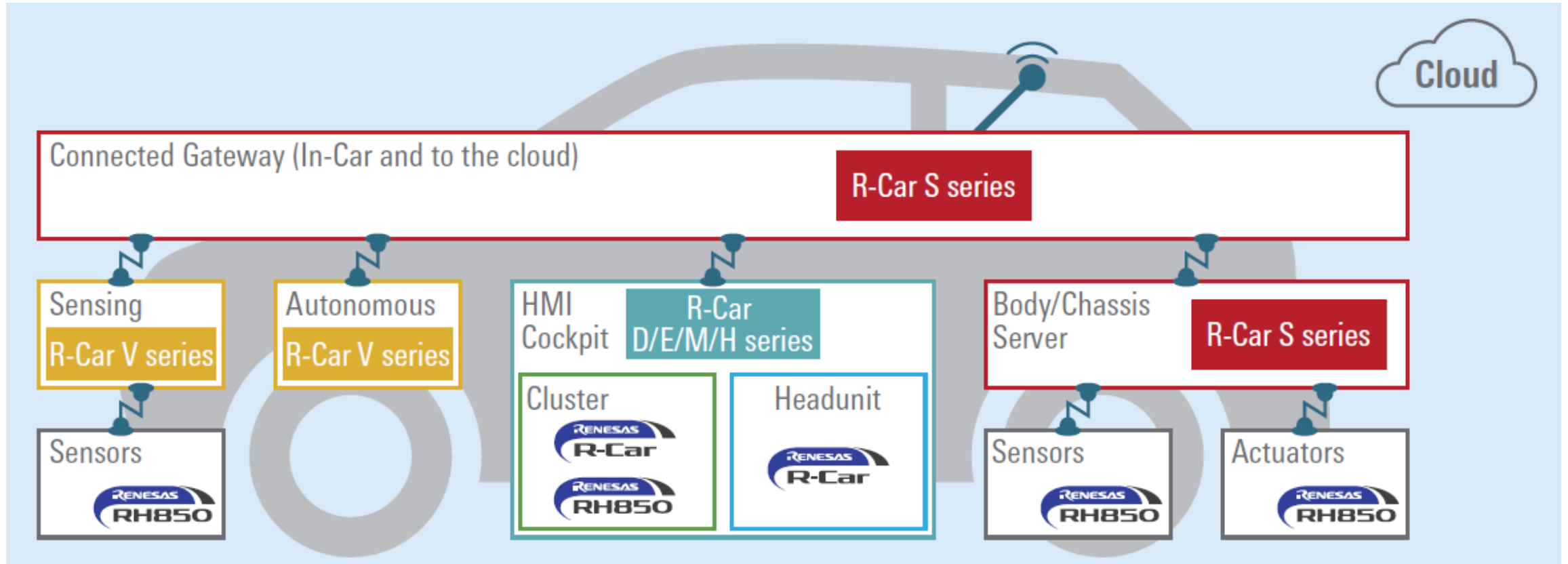
Robust infrastructure,  
enabling  
safety and efficiency



IoT

Comfortable, safe and  
healthy lifestyles  
through IoT

# Renesas Automotive Products Comply with ISO 26262



- Functional Safety support (ISO26262)
- Contribution to ASIL B~D support of customer systems

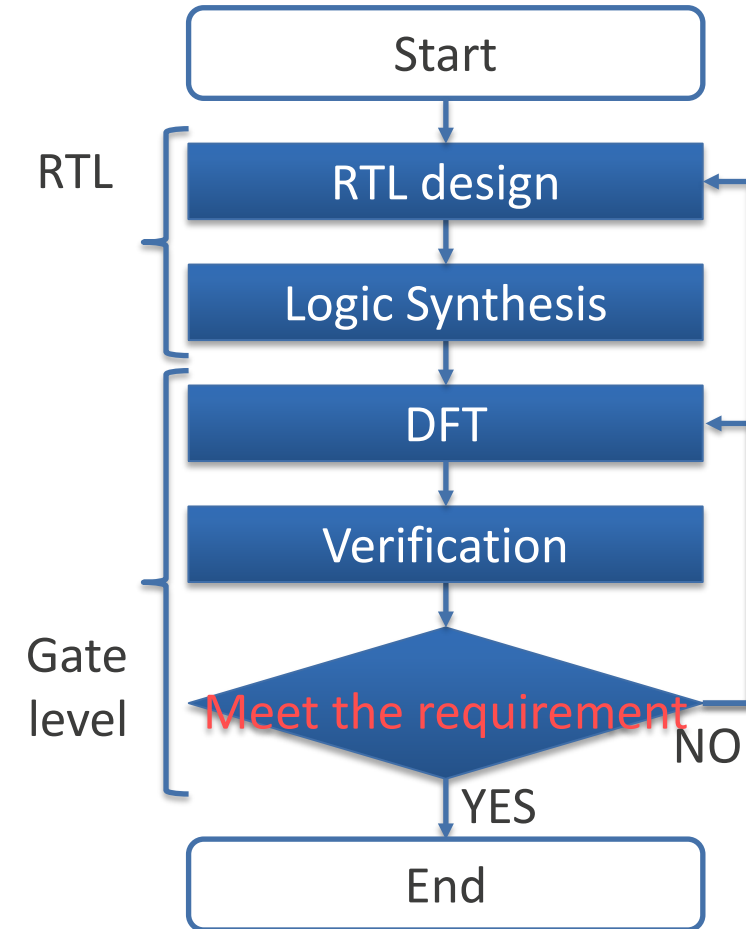
# Outline

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- 1. Background**
  - Design Shift Left
  - Tessent new feature: RTL TPI
- 2. Evaluation Result of RTL TPI**
- 3. Conclusion**

# Necessity of Design Shift Left

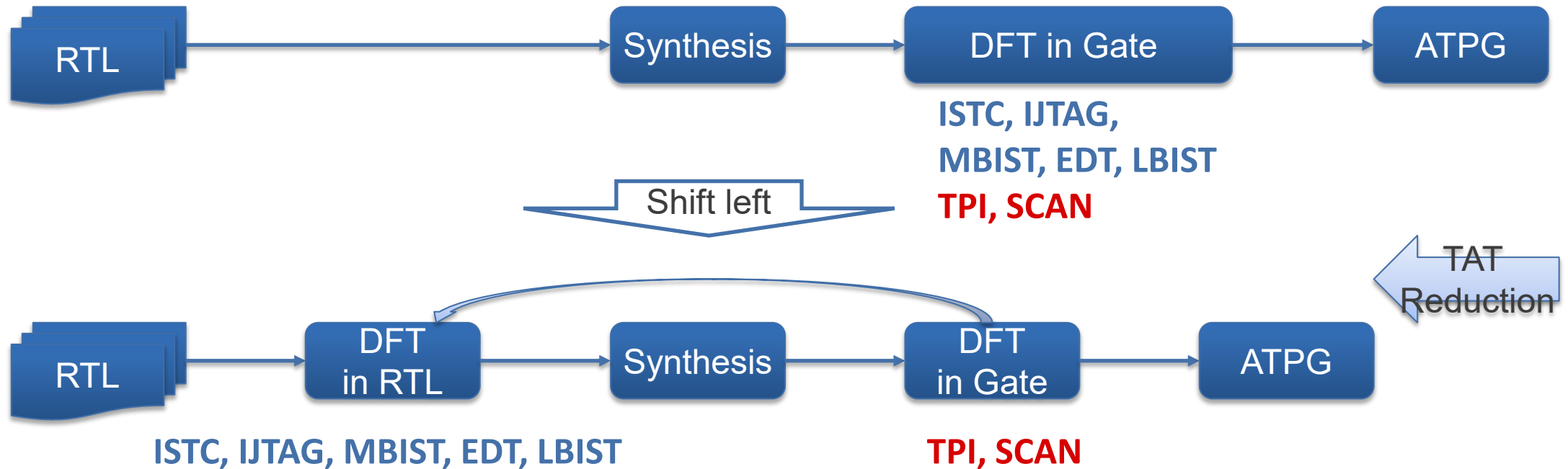
- Safety is a mandatory request for semiconductors
- Implementation of functional safety function is complicated
  - Its verification tends to be long term because some items need to be done at gate-level
    - Large overhead on account of rework from Gate to RTL
- An approach to reduce design period is design shift left
  - Part of verification is done in RTL
    - Fast verification
    - Small iteration overhead



Traditional front-end design flow

# Shift Left of DFT

- We have developed DFT-in-RTL flow in which DFT IP insertion moves toward RTL
  - TPI and Scan insertion are remaining at gate-level





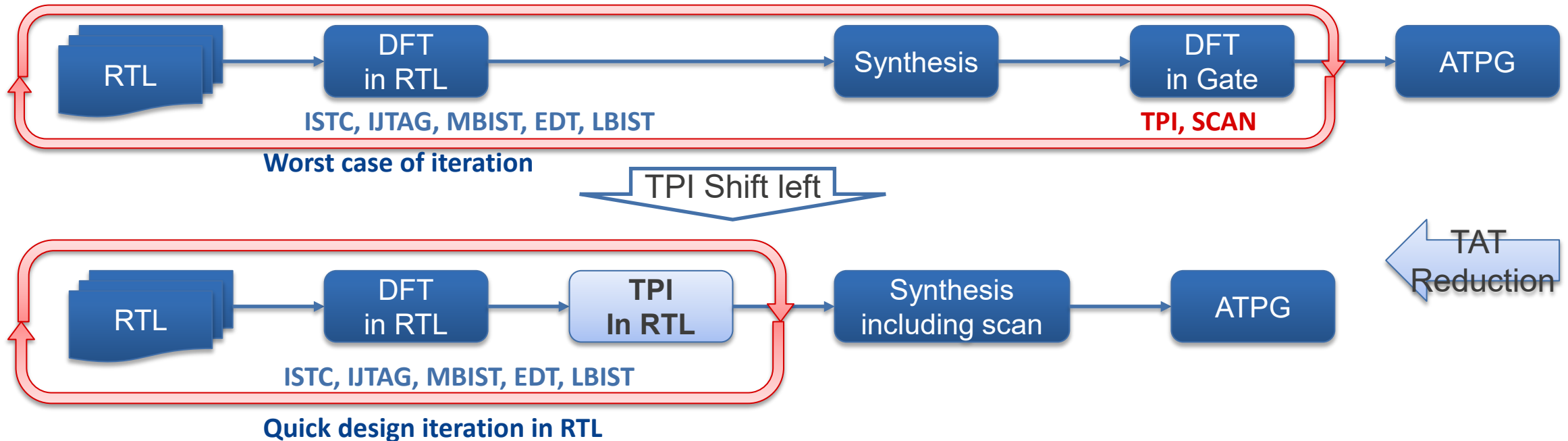
# Challenge of Functional Safety Function Implementation

- Increasing demand for higher ASIL certification
- Part of safety mechanism is implemented with Logic BIST (LBIST)
  - The target test coverage must be achieved for each functional safety module within a limited test time
  - Considerable test points are required
    - **TPI process has a significant impact on design period**
- **Expectation for RTL TPI**
  - If RTL TPI achieves the same LBIST test coverage as Gate TPI, it is usable for design shift-left to reduce design period

	ASIL B	ASIL C	ASIL D
Single point fault metric (SPFM)	≥ 90%	≥ 97%	≥ 99%
Latent fault metric (LFM)	≥ 60%	≥ 80%	≥ 90%

# Tessent New Feature: RTL TPI

- Tessent new feature enables TPI in RTL
  - A test point is directly incorporated into RTL code
  - DFT and Verification will be completed at RTL
    - Quick verification iteration will achieve short design period





# Tessent RTL TPI Evaluation

- RTL TPI Evaluation for 3 RTL safety modules
  - Common features
    - Many TPs are required to improve test coverage and many TPI iterations occur
- RTL TPI vs Gate TPI evaluation items
  - Estimated test coverage
  - Cell area after scan chain insertion (Gate level)
  - Actual LBIST test coverage @ same pattern count
  - # EDT patterns @ same test coverage

## Module Specification

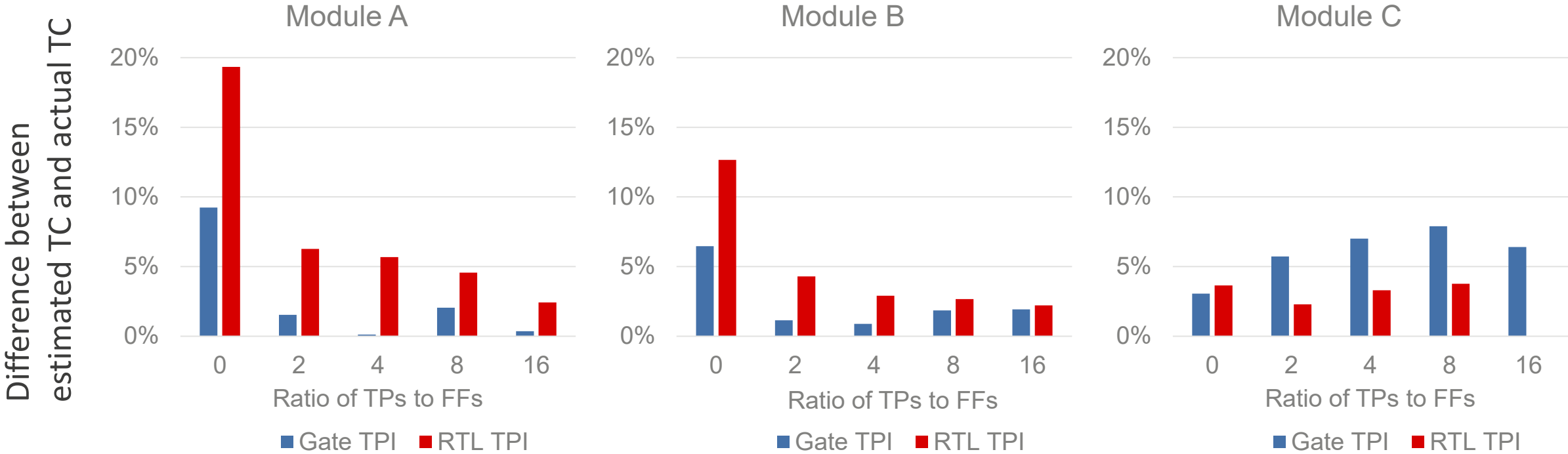
	A	B	C
# RTL lines	320k	164k	367k
# FFs (after synthesis)	11k	33k	256k
# gates (after synthesis)	124k	571k	3,913k

- Evaluation condition
  - # inserted TPs is the following ratio to #FFs
    - 0%, 2%, 4%, 8%, 16%

# Evaluation Results:

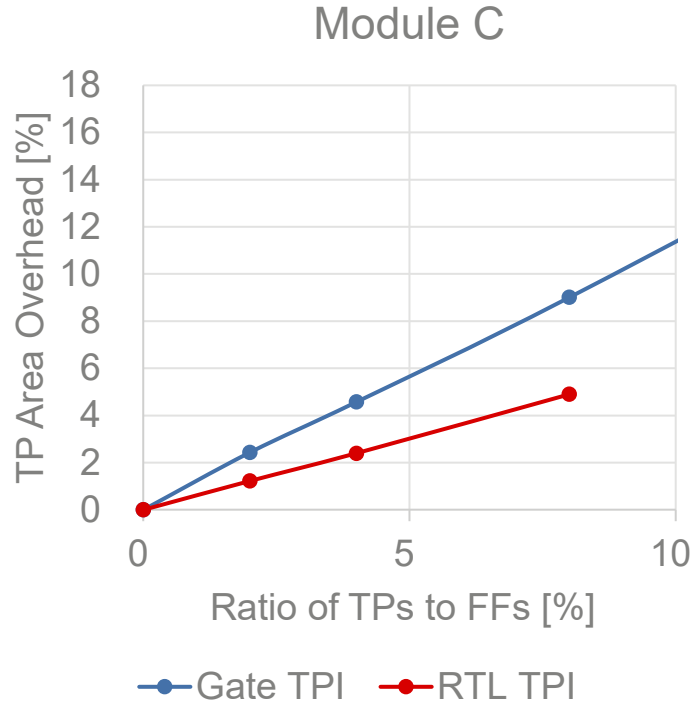
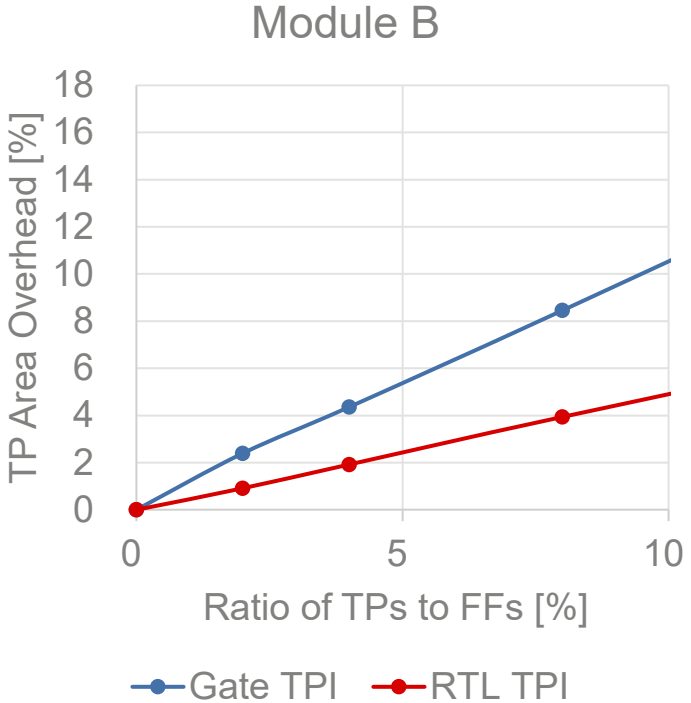
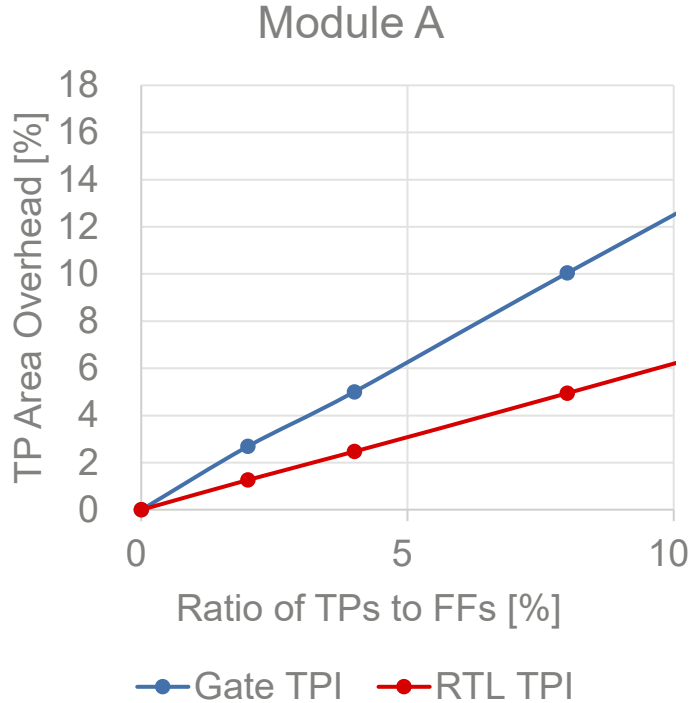
## LBIST TC Difference between Estimation and Actual Result

- Although there are variations in the tendency of the results depending on the module, the difference is within about 5%



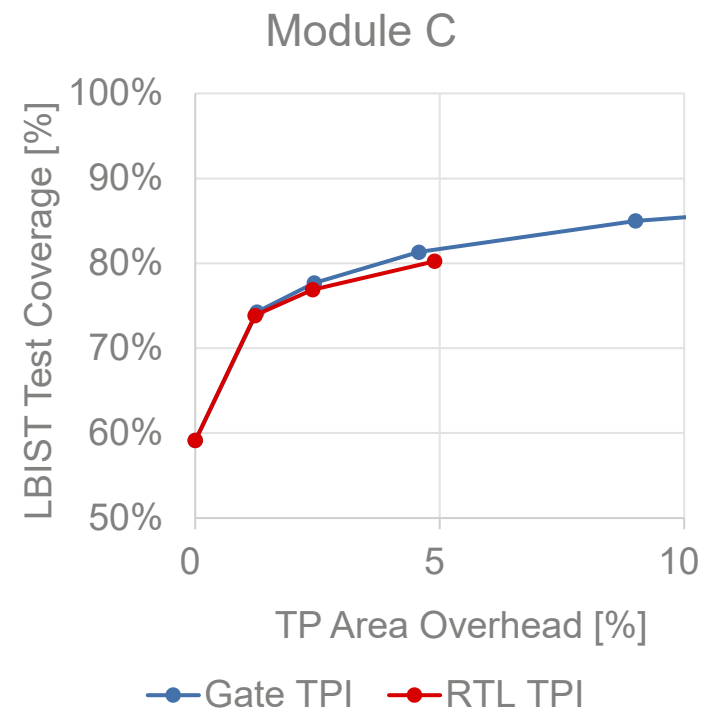
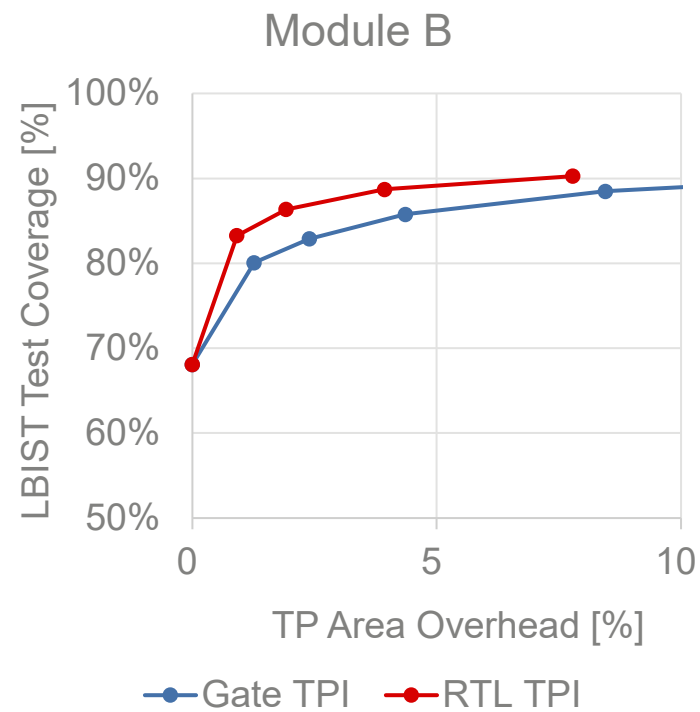
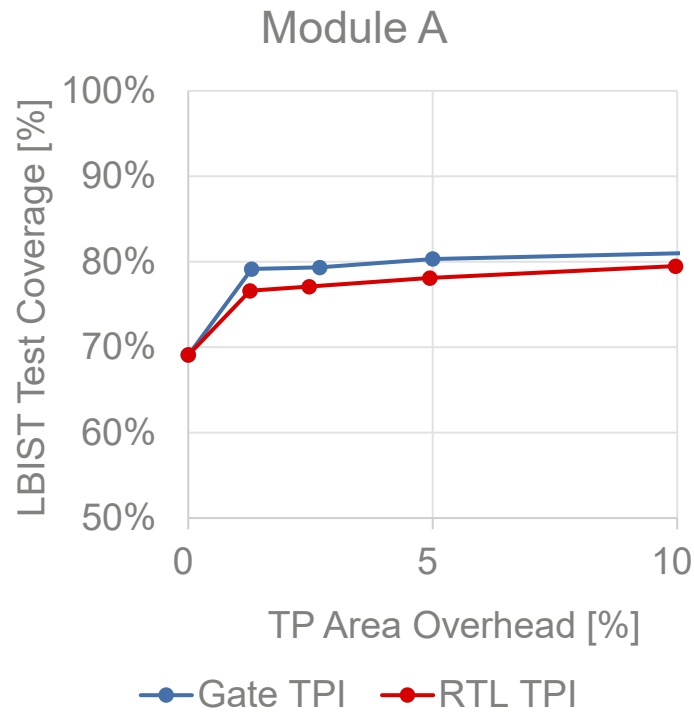
# Evaluation Results: Cell Area

- The area overhead of RTL TPI tends to be smaller than that of Gate TPI



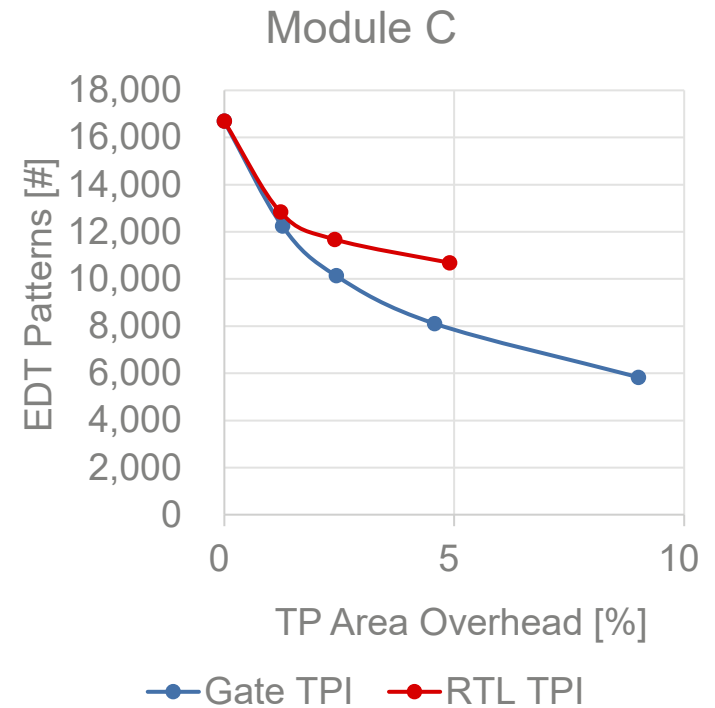
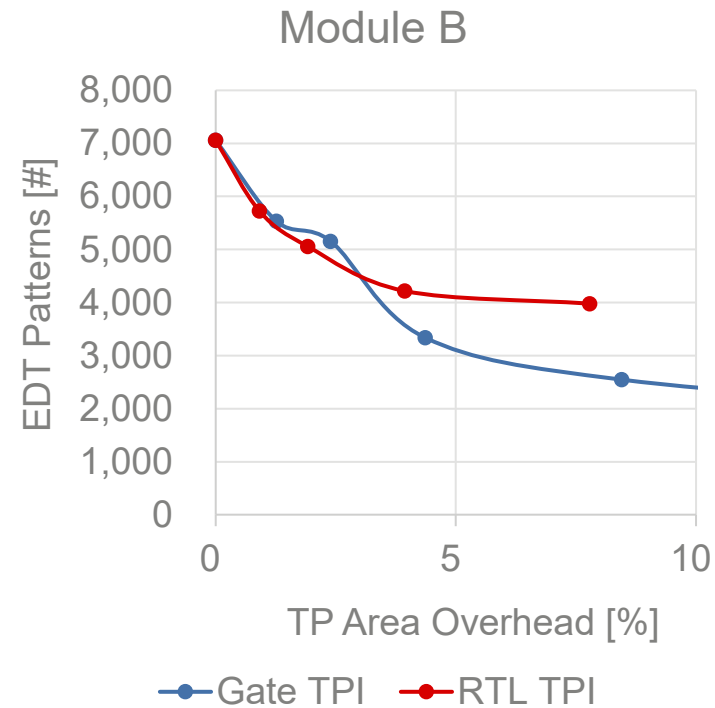
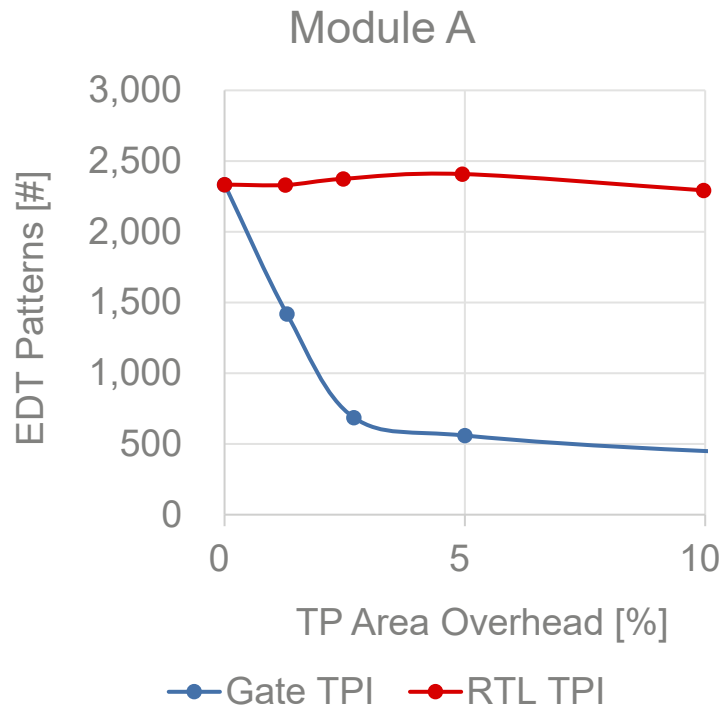
# Evaluation Results: LBIST Test Coverage

- Improvement in LBIST test coverage relative to area OH is comparable  
⇒ **RTL TPI is usable for safety mechanism implementation**



# Evaluation Results: # EDT patterns

- Not effective in terms of mass-production testing as compared with Gate TPI



# Conclusion

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- Renesas advances the design shift-left utilizing Tessent
  - Tessent RTL TPI can be a practical solution for implementation of safety mechanism
    - TPI process can also move toward RTL in a real product design
  - Most of the DFT implementation can be completed in RTL, allowing for shorter design period
  
- Expectations for Tessent
  - Improvement of # EDT patterns in terms of mass production testing
  - Continued improvement of solution for design shift-left

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