Renesas’ Shift Left with Design-for-Test Using Tessent® RTL TPI

Sep 27, 2022
Hiroyuki Iwata
Digital Design Technology Department
Renesas Electronics Corporation
About Renesas Electronics Corporation

Our mission is to develop a safer, healthier, greener, and smarter world by providing intelligence to our four focus growth segments: Automotive, Industrial, Infrastructure, and IoT that are all vital to our daily lives, meaning our products and solutions are embedded everywhere.

Highly reliable vehicle control, safe and secure autonomous driving, Eco-friendly electric vehicles

Lean, flexible and smart industry

Robust infrastructure, enabling safety and efficiency

Comfortable, safe and healthy lifestyles through IoT
Renesas Automotive Products Comply with ISO 26262

- Functional Safety support (ISO26262)
- Contribution to ASIL B~D support of customer systems
Outline

1. Background
   - Design Shift Left
   - Tessent new feature: RTL TPI

2. Evaluation Result of RTL TPI

3. Conclusion
Necessity of Design Shift Left

- Safety is a mandatory request for semiconductors
- Implementation of functional safety function is complicated
  - Its verification tends to be long term because some items need to be done at gate-level
    - Large overhead on account of rework from Gate to RTL
- An approach to reduce design period is design shift left
  - Part of verification is done in RTL
    - Fast verification
    - Small iteration overhead
Shift Left of DFT

- We have developed DFT-in-RTL flow in which DFT IP insertion moves toward RTL
  - TPI and Scan insertion are remaining at gate-level
Challenge of Functional Safety Function Implementation

- Increasing demand for higher ASIL certification
- Part of safety mechanism is implemented with Logic BIST (LBIST)
  - The target test coverage must be achieved for each functional safety module within a limited test time
- Considerable test points are required
  - TPI process has a significant impact on design period

<table>
<thead>
<tr>
<th></th>
<th>ASIL B</th>
<th>ASIL C</th>
<th>ASIL D</th>
</tr>
</thead>
<tbody>
<tr>
<td>Single point fault metric (SPFM)</td>
<td>≥ 90%</td>
<td>≥ 97%</td>
<td>≥ 99%</td>
</tr>
<tr>
<td>Latent fault metric (LFM)</td>
<td>≥ 60%</td>
<td>≥ 80%</td>
<td>≥ 90%</td>
</tr>
</tbody>
</table>

Expectation for RTL TPI

- If RTL TPI achieves the same LBIST test coverage as Gate TPI, it is usable for design shift-left to reduce design period
Tessent New Feature: RTL TPI

- Tessent new feature enables TPI in RTL
- A test point is directly incorporated into RTL code
- DFT and Verification will be completed at RTL
  - Quick verification iteration will achieve short design period

![Diagram showing the flow of design and verification steps including RTL, DFT, Synthesis, ATPG, and TAT Reduction.](image-url)
Tessent RTL TPI Evaluation

- RTL TPI Evaluation for 3 RTL safety modules
  - Common features
    - Many TPs are required to improve test coverage and many TPI iterations occur

- RTL TPI vs Gate TPI evaluation items
  - Estimated test coverage
  - Cell area after scan chain insertion (Gate level)
  - Actual LBIST test coverage @ same pattern count
  - # EDT patterns @ same test coverage

<table>
<thead>
<tr>
<th>Module Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
</tr>
<tr>
<td># RTL lines</td>
</tr>
<tr>
<td># FFs (after synthesis)</td>
</tr>
<tr>
<td># gates (after synthesis)</td>
</tr>
</tbody>
</table>

- Evaluation condition
  - # inserted TPs is the following ratio to #FFs
    - 0%, 2%, 4%, 8%, 16%
Evaluation Results:
LBIST TC Difference between Estimation and Actual Result

- Although there are variations in the tendency of the results depending on the module, the difference is within about 5%
Evaluation Results: Cell Area

- The area overhead of RTL TPI tends to be smaller than that of Gate TPI
Evaluation Results: LBIST Test Coverage

- Improvement in LBIST test coverage relative to area OH is comparable
  \[\Rightarrow\text{RTL TPI is usable for safety mechanism implementation}\]
Evaluation Results: # EDT patterns

- Not effective in terms of mass-production testing as compared with Gate TPI
Conclusion

- Renesas advances the design shift-left utilizing Tessent
  - Tessent RTL TPI can be a practical solution for implementation of safety mechanism
    - TPI process can also move toward RTL in a real product design
  - Most of the DFT implementation can be completed in RTL, allowing for shorter design period

- Expectations for Tessent
  - Improvement of # EDT patterns in terms of mass production testing
  - Continued improvement of solution for design shift-left