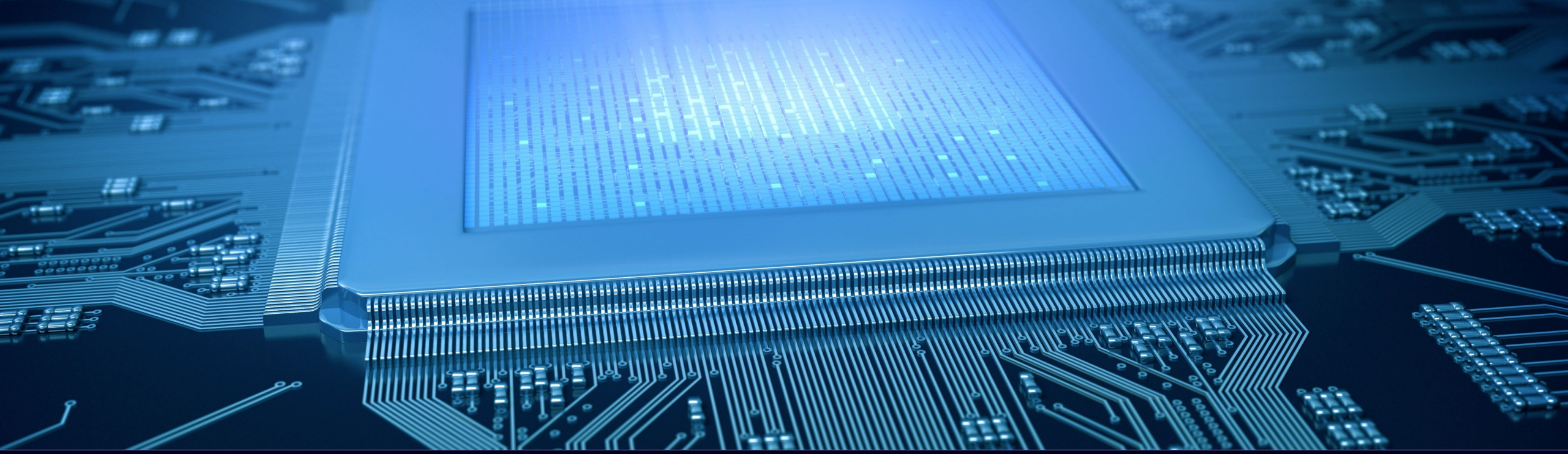

Efficiency of Packetized data delivery in 2.5D/3D designs

Peter Orlando, Kacper Grubich, Mateusz Czartoryski

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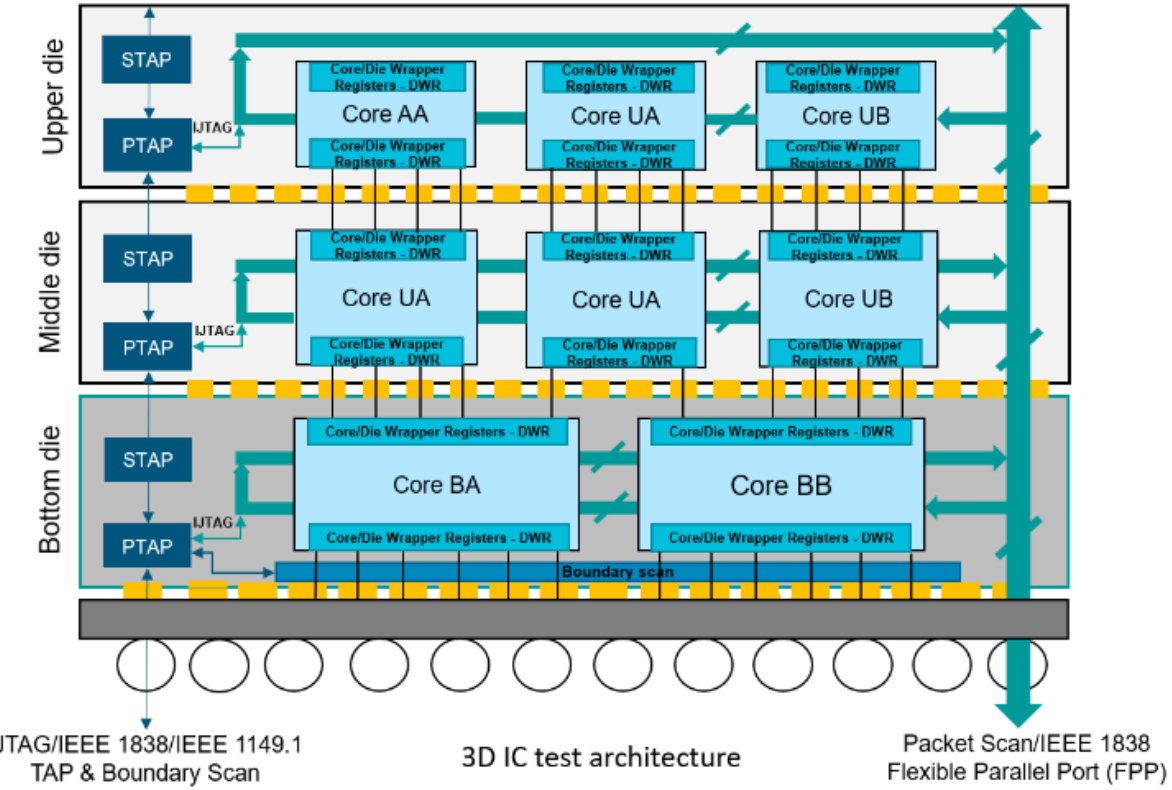
Packetized scan network for 2.5D/3D designs

- IEEE 1838
- Test access architecture for 3D stacked ICs



- Same benefits seen with 1D designs
- Scalable solution when using FPP
- Parallel n-bit wide bus to all cores in designs
- Payload synchronously distributed concurrently to active cores
- Proven to be major component in test time reduction and optimal scan data volume
  - Bandwidth turning
  - Decouple core level channel requirements from chip IO resources
  - Fewer patterns through optimal scan compression

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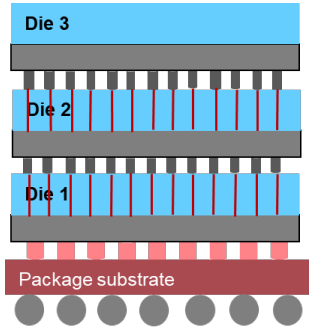
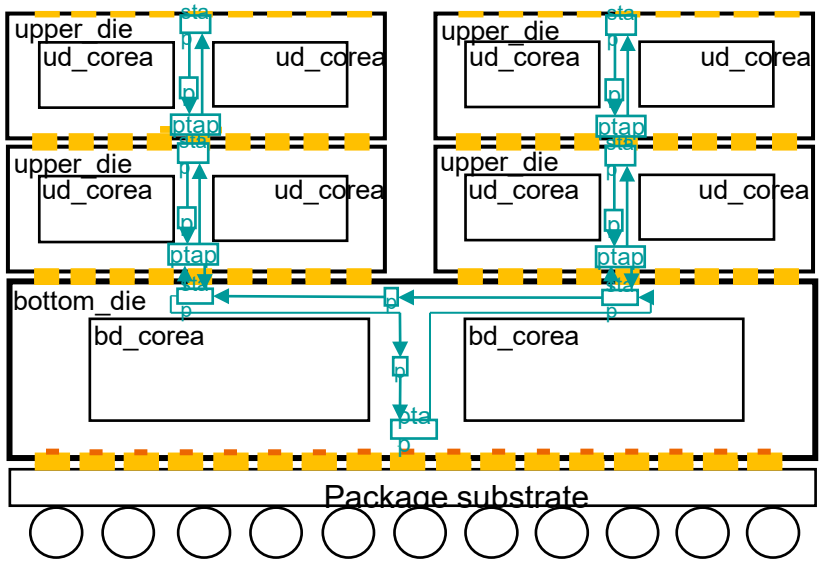
Limitations without Flexible Parallel Port (FPP)



3D device



- TAP access limits the scan bus to single bit
- Low test clock (1149.1 TCK) frequency
- High-effort routing and timing closure for test signals
- No safety backup mechanism

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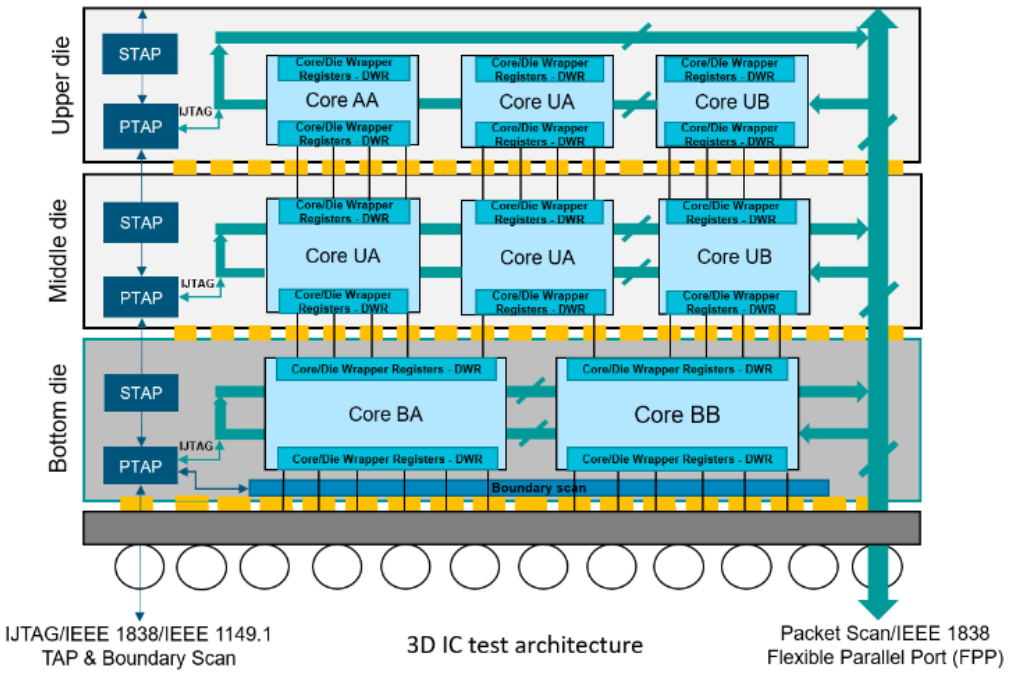
Benefits of the parallel bus



- ✓ FPP allows data packetization for scan data delivery and provides independent test signal sources for each die. Cores within a die can be run concurrently while having a predictable, local timing
- ✓ Parallel access enables multiple-bit bus width. When combined with higher bus clock frequency the bus provides high throughput.
- ✓ Additional data delivery method makes the IJTAG access a backup mechanism in case the bus is inoperative

Possible test time reduction

Bus width	TAP/IJTAG access	FPP access
One bit	1x*	Nx**
M bits	1x (wider bus is forbidden)	(NxM)x

* Test clock without FPP acts as a reference clock

** N is calculated as the frequency ratio of the FPP bus clock to the 1149.1 test clock

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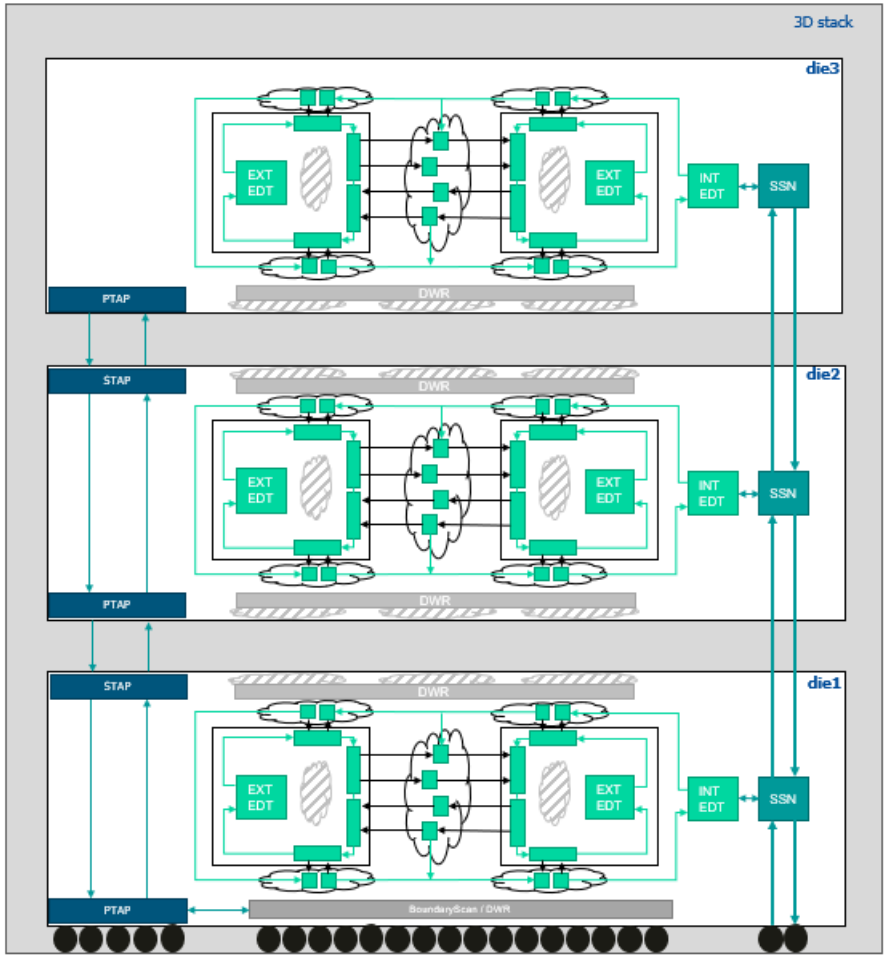
Comparison non-FPP and FPP designs

Description	Without FPP	With FPP
Scan Delivery	Shifted through TAP controllers and IJTAG network	Shifted through the n-bit wide bus (IJTAG network as back up mechanism)
Bus clocking	1149.1 test clock	Independent bus clock
Access to adjacent dies (2.5D)	In-series Test Access Ports (TAPs)	Mux-based parallel bus configuration for bypassing unused die (TAPs as back up mechanism)
Access to upper dies (3D)	In-series Primary TAPs (PTAPs) and Secondary TAPs (STAPS)	Direct access through the dies – mux-based configuration to access the internal die logic
Test signal management	Sourced from stack boundary and routed to all dies	Locally generated for each core in each die
Compression logic	Pin-mux based configuration, dependent on the number of pins	EDT channels are independent from the number of pins connected to FPP logic
Core dependency during tests	All cores dependent on shared global test signal sources	Cores run concurrently thanks to locally generated test signals

Die-level considerations



IJTAG/IEEE 1838/IEEE 1149.1
TAP & Boundary Scan

3D IC test architecture

Packet Scan/IEEE 1838
Flexible Parallel Port (FPP)

- Packetized network is a plug-and-paly architecture
- Cores are encapsulated and unaffected by changes at the top-level
- Addition of new cores or changes at the core level do not affect top-level DFT architecture
- Test signals don't span hierarchy boundaries. This simplifies routing and timing closure at all levels

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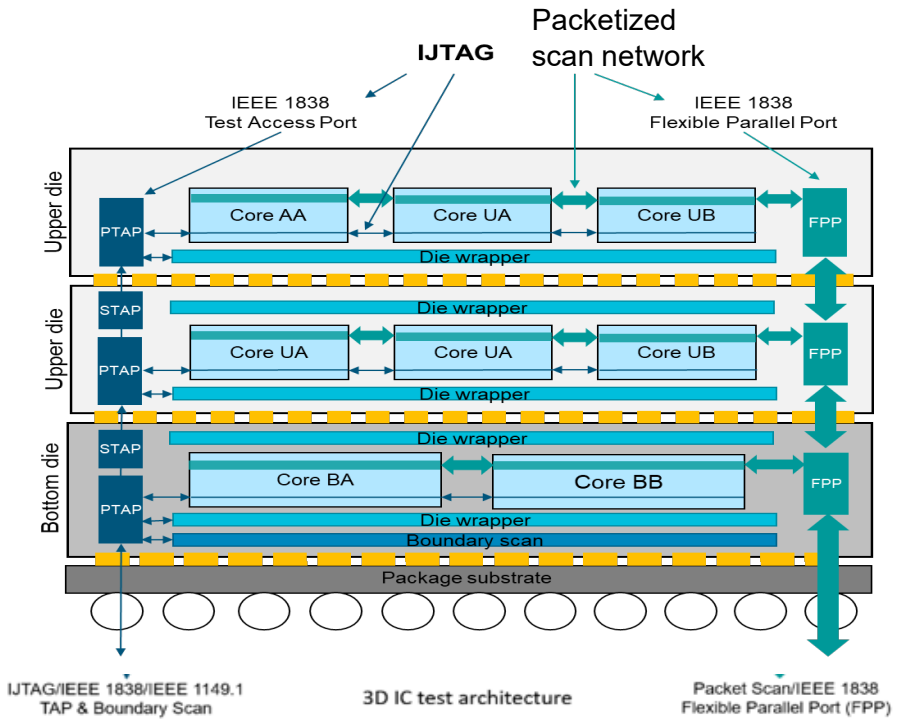
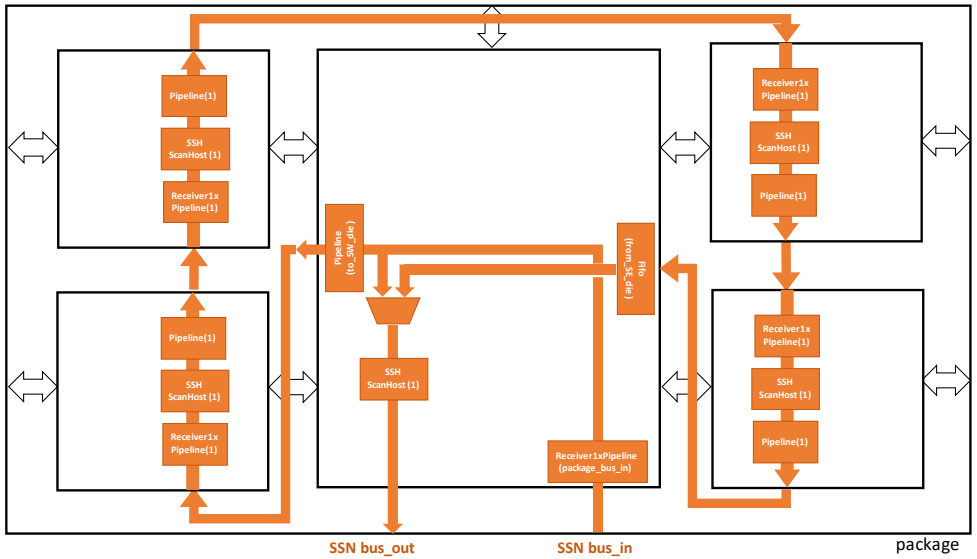
Efficiency of packetized data delivery in 2.5D/3D designs

Summary

- ✓ Compatible with both 2.5D/3D packetized scan network
- ✓ Improves testability through parallel access
- ✓ Locally generated scan signals allows easier timing closure
- ✓ Compliance with tile-based design flows
- ✓ Scalable for multi-dimensional architectures
- ✓ Provide backup mechanism
- ✓ Predictability and dependable access





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Thank you

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Backup slides

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