ITC 2023 PO.42: RTL DFT Analysis and Insertion of Test Points at RTL

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Abstract: Insertion of Design-for-Test (DFT) components at the Register-Transfer Level (RTL) of design abstraction allows downstream software tools to use the same original design view. Doing so also promotes more efficient creation and use of DFT resources and enables synthesis tools to optimize DFT components such as Memory BIST logic, compression logic, core wrapper logic, and test points along with functional logic earlier in the design flow.

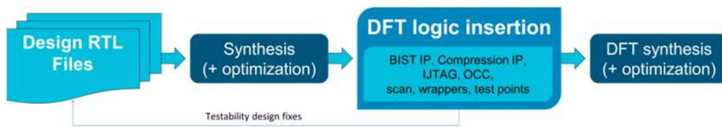
Traditional, gate-Level DFT flow

PROS

- Single-pass DFT insertion
- Fully editable date-level design

CONS

- Multiple synthesis runs
- Lengthy time-to-coverage and time-to-pattern count
- Timing and area impact of DFT logic unknown initially
- Test Coverage and pattern count known only after multiple synthesis passes



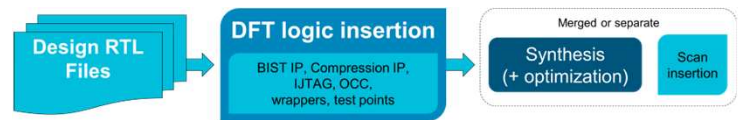
Improved, shift-Left DFT flow

PROS

- Single-pass DFT insertion
- Timing and area impact of DFT logic known up front
- Initial coverage and pattern count can be estimated using quick synthesis
- Single synthesis run
- Improved timing closure, PPA, and TTM
- RTL-based verification flows see the same view of the design

CONS

- Some RTL-based structures difficult to edit (e.g., macros)



Key components to RTL DFT Analysis and DFT Insertion

Design Rule Checks (DRCs)

Clock / Set / Reset controllability
Clock node editability
Low-power DFT connectivity

Design-for-Test (DFT) IPs

MBIST / MBISR / LBIST / OST
Compression / OCC / DFT Interface IP
Wrappers / Test Points / X-Bounding

Other RTL testability considerations

Outlier Identification (coverage/pattern count)
Design editing & ECO implementation
Same RTL used for Synthesis & Verification (RTL in → RTL out)

Test point effectiveness on several industrial designs, seen achieving similar gate-level results when implementing at RTL

	Design gates	Scan cells	Compression ratio	RTL TP suitability	Compressed ATPG (baseline, no test points) TC [%]	PC	ATPG runtime (s)	Compressed ATPG (Gate-level test points) TP (CP, OP)	# patterns @ BL TC	PC reduction [%] @BL TC	ATPG runtime (s)	Compressed ATPG (RTL test points) TP (CP, OP)	# patterns @ BL TC	PC reduction [%] @BL TC	ATPG runtime (s)
D1	1.12M	44k	123	**High**	93.1	8387	418	(386, 557)	3071	**63.4**	229	(385, 557)	4799	**43**	262
D2	3.4M	150k	135	**High**	94.9	2579	688	(1241, 1790)	704	**72.7**	628	(1486, 1483)	960	**63**	624
D3	0.57M	22k	125	**Medium**	96	18560	914	(191, 248)	8743	**53**	345	(234, 205)	8932	**52**	400
D4	5.3M	255k	134	**High**	97.32	10291	2352	(1813, 3275)	4717	**54**	1018	(3550, 1514)	6130	**40.5**	1183
D5	1.2M	43k	123	**High**	99.26	18526	1435	(456, 405)	11102	**40**	1318	(455, 406)	11006	★ **40.6**	896
D6	10M	440k	246	**High**	93.7	29256	22419	(1659, 2118)	23618	**19.3**	8301	(742, 563)	13169	★ **55**	13177
D7	3.7M	208k	125	**High**	98.27	10125	3265	(2094, 2205)	7194	**29**	2200	(1638, 2653)	7923	**22**	2088
D8	1.74M	119k	141	**High**	95.49	14217	787	(957, 1429)	5788	**59.3**	860	(751, 1635)	8516	**40**	1790
D9	3.4M	103k	128	**High**	96.66	63381	63381	(1630, 469)	38133	**40**	7586	(1309, 790)	43317	**32**	6624
D10	9.36M	458k	138	**Medium**	98.61	8226	5639	(4012, 5762)	5808	**29.4**	6389	(3487, 3835)	6463	**22**	9179
D11	10.6M	739k	188	**High**	99.08	14238	6102	(5042, 9780)	9787	**31.3**	6765	(6972, 7877)	9970	**30**	7216
D12	4M	222k	140	**High**	99.32	16584	3011	(2133, 2364)	10005	**39.7**	2103	(3240, 1103)	9395	★ **43.35**	2392

Industrial design results comparisons:
44.25% average pattern count reduction with GL test points
40.3% average pattern count reduction with RTL test points

Additional RTL test point observations:
Improved area due to fewer test points in some designs
Some design show Improved results when compares with gate-level test points

Conclusion: It is possible to insert all major DFT components at RTL. This leaves only scan insertion and shared wrapper cell logic to be inserted at the gate level, making "shift-left" a reality. Synthesis and verification flows can use the same RTL, and experimental results from RTL test point insertion show that it is possible to get similar results to gate-level.