SIEMENS DIGITAL INDUSTRIES SOFTWARE

Siemens EDA **IC Package Design Consulting**

Enabling electronics manufacturers to get the full value out of their EDA tools

Benefits

- Enables electronics manufacturers to maximize their EDA tool investment
- Enhances advanced packaging design flows
- Develops custom package and chiplet test vehicles used for package reliability analysis
- Provides signal and power integrity analysis
- Integrates supply chain and enterprise design processes

Summary

Semiconductor packaging is undergoing a huge disruption; a variety of new technologies and mechanisms for integrating capabilities on a single substrate are now available and these technologies leverage the design space between integrated circuit (IC) and advanced packaging design technology. Organic build-up substrates, fan-out wafer-level packaging, high-density flip-chip system-in-package, 2.5 and 3D heterogeneous integration and chiplets with silicon-based substrates following IC manufacturing design flows all have their own unique design challenges.

Designers are being challenged by rapid changes in manufacturing technologies. Many find they may not have the expertise to address these complex substrate types, or to work effectively with a chosen outsourced assembly and test (OSAT) or foundry given the learning curve and overhead of interpreting and translating design rule manuals, process design kits (PDKs), etc.

Siemens EDA IC Package Design Consulting team offers compelling services in package design planning, implementation and flow recommendations used by numerous fabless integrated device manufacturer (IDM) semiconductor and system companies. Our diverse set of service offerings are part of the Xcelerator™ portfolio, the comprehensive and integrated portfolio of software and services from Siemens Digital Industries Software, and address the following key aspects of IC package and high-density advanced packaging design flows:

Design capture and planning

Our teams are experienced at capturing 2.5 and 3D package designs in a technology-specific packaging flow and perform planning functions to drive a physical design implementation, which is optimized for signal integrity with a minimum number of substrate layers. Key services include capturing the logical conductivity of a system, defining the physical topology and component placement, defining and optimizing pin-out assignments and smoothing collaboration between printed circuit board (PCB), interposer and application-specific integrated circuit (ASIC) design teams. Defining the Calibre® 3DSTACK software deck for design rule checking (DRC) and layout versus schematic (LVS) conductivity validation during the design process can also be performed.

Substrate layout

Our teams have significant experience in executing the physical layout and verification of an HDAP substrate. This may include importing a package substrate design from xSI or ODB++™ data format plots, and the package design rules and assembly design kits for a target substrate vendor technology. Additionally, the physical design layout of the package substrate, including DRC analysis and layout optimization for power and signal integrity compliance, may be executed. We can also run and correct design-for-manufacturing (DFM) rules to meet the manufacturer's requirements and validate the design, including conductivity and alignment checks using the post-layout substrate design database.

We have implemented these services for a wide range of customer requirements, including traditional package substrates, 2.5D interposer technology, chiplets and silicon-based substrates.

Signal and power integrity analysis

We offer various levels of signal integrity analysis for multi-die system designs that require composite and extraction of the 3D package and PCB and system level signal integrity/power integrity (SI/PI) analyses. Our expertise includes parasitic extraction (PEX) of organic and interposer designs of both the PCB and the silicon interposer. We also corroborate these analysis results to optimize the design layouts as required for an entire system.

Package thermal and stress analysis

Our services include a wide range of crucial analyses of die-to-die thermal interaction between ASIC and/or chiplets in a system design as well as thermomechanical stress for large interposer-based 2.5D/3D designs. Additionally, our teams are experienced in pre-layout thermal planning, die-package thermal analysis/verification and detailed die-level thermal analysis and optimization. Relevant analyses can include simulation for package level warpage, stress and fatigue analysis results using imported thermal analysis results and performance of thermal stress simulation and optimization across the entire system.

Custom package ADK development

These services can provide HyperLynx design rule checks and Valor™ software rules from vendor-supplied PDKs for organic, buildup and silicon-based manufacturing technologies. We also offer deck development services, with key technologies including:

- HyperLynx PEX substrate and interposer
- PCB extraction
- Calibre xACT interposer extraction

Additionally, we offer development of Calibre Programmable Electrical Rules Checking (PERC) ASIC ERC checks and custom PERC 3D chip decks to evaluate the system, and conversion of Calibre decks designed for silicon-based technologies for use by our Xpedition package design tools.

These decks can be created regardless of whether the substrate technology is developed using traditional packaging, interposer or silicon-based chiplet methodologies.

Package test vehicles

Offerings in this space include development of custom package and chiplet test vehicles used for package reliability analysis. From working with the customer to providing a methodology and strategy for package test vehicle creation, we develop custom flows to design and validate the test structures and implement these tests structures in our packaging design tools. Then we provide thermal and stress analysis support for those package test designs prior to use.

2.5D and 3D test vehicles

Our teams leverage our Tessent™ software tool suite to provide a wide range of design-for-test (DFT) services for 2.5D and 3D system designs, including:

- Boundary scan planning test input/output (IO) mapping
- SSN/JTAG bus routing and support die-to-die conductivity redundancy and repair
- Embedded die/chiplet system-on-chip (SOC) level tests for both chip and chiplet IOs in 2.5D and 3D designs
- High-speed IO testing (loopback)

As needed, we also verify simultaneous switching noise (SSN)/JTAG timing and provide functional timing simulation, probe pad IR drop validation and probe pad planning support for 2.5 and 3D designs.

Customers across the electronics industry have chosen the capabilities, expertise and knowledge of Siemens EDA Consulting Services to achieve technical success and improved productivity.

For more information on how we can help you achieve your next success, contact your Siemens EDA representative, or email us at EDAServices.sisw@siemens.com

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