Using Tessent for Tile-based designs

Vidya Neerkundar
Product Manager, Tessent

September 2022
Tile Based Designs / Abutment based Physical blocks

• Description
  – Physical blocks placed using abutment
  – No logic at chip-level

• Challenges
  – Each core with varied input/output compression channels
  – Allocation and routing chip IO pins
  – Dealing with identical cores with different pipeline stages
  – Clocking architecture for external mode of tiles
  – Memories with repair from different power domain
  – Tiles with embedded IOs
  – Tiles without any embedded IOs
Tessent Streaming Scan Network (SSN)

- Cut DFT development time in half or more
  - Decouple core and chip level DFT
  - Define core grouping at retargeting time
  - Bus can be any width, even 1 bit

- Eases routing and timing closure
  - Eliminates top-level test mode muxing
  - Supports tile-based design with abutment

- Up to 4X test time and volume reduction
  - Packets are 100% scan data payload
  - Reduces padding in test data
  - Optimal core compression
  - Time multiplexing
  - Identical cores tested at constant cost, with diagnosis support
Clocking during Logic Test

- Each tile is wrapped during scan insertion
  - Wrapper cells added
- One OCC per clock source in each tile
- During Internal test, each tile is tested independently
Clocking during **internal** test of tiles

- Each tile is wrapped during scan insertion
- One OCC per clock source in each tile
- During Internal test, each tile is tested independently
- An OCC bypass clock mux is needed to run in parallel
  - Verified by R27
- Multiplexer inserted at the same time as OCC
Clocking during external test of tiles

- OCC bypass clock multiplexers returned to functional path during external test
- All OCCs used in shift-only mode except for the one at the root of the clock in C3
- Inter-tile timing paths naturally tested using functional timing
Inserting IJTAG network into the tiles

• The flow is identical to the non-tiling flow
  – Need to include insertion of SIBs (thc, th, tc) to tile-based designs

• IJTAG clocking localized to each tile
  – TCK clock sent outward from central tile
  – Forward timing in outward paths
  – Loop timing on the return paths

th – tile host
thc – tile host collector
tc – tile client
sti – scan tested instrument
sri – scan resource instrument
Inserting Memory BIST and BISR into the tiles

- Memory BISR has one chain per power domain

- BISR clocking localized to each tile
  - BISR clock sent outward from central tile
  - Forward timing in outward paths
  - Loop timing on the return paths

- BISR chain creation controlled by specifying memory bisr host list and reading UPF file that assigns power domains

- BISR chain ordering controlled by specifying memory bisr host list and reading DEF file
Boundary Scan insertion within tile followed by BSDL extraction at the chip level

- Embedded Boundary Scan (EBScan) chains inserted into each tile that has pads
- Sub-block wrapper modules around groups of pads in C3 for
  - EBScan insertion flow
  - BSDL extraction flow
- EBScan segments reused as dedicated wrapper chains during logic test
- Auxiliary pad logic inserted for SSN bus clock and data
- Internal BScan cells used as pipelines when crossing tiles without pads (C2)
Summary

- Streaming Scan Network (SSN) for scan delivery with identical core support
- BSDL extraction from Embedded Boundary Scan segments
- Embedded Boundary Scan segments reused as wrapper cells
- SecondaryHostScanInterface in IJTAG network
Thank You