Test Generation for an Iterative Design Flow with RTL Changes

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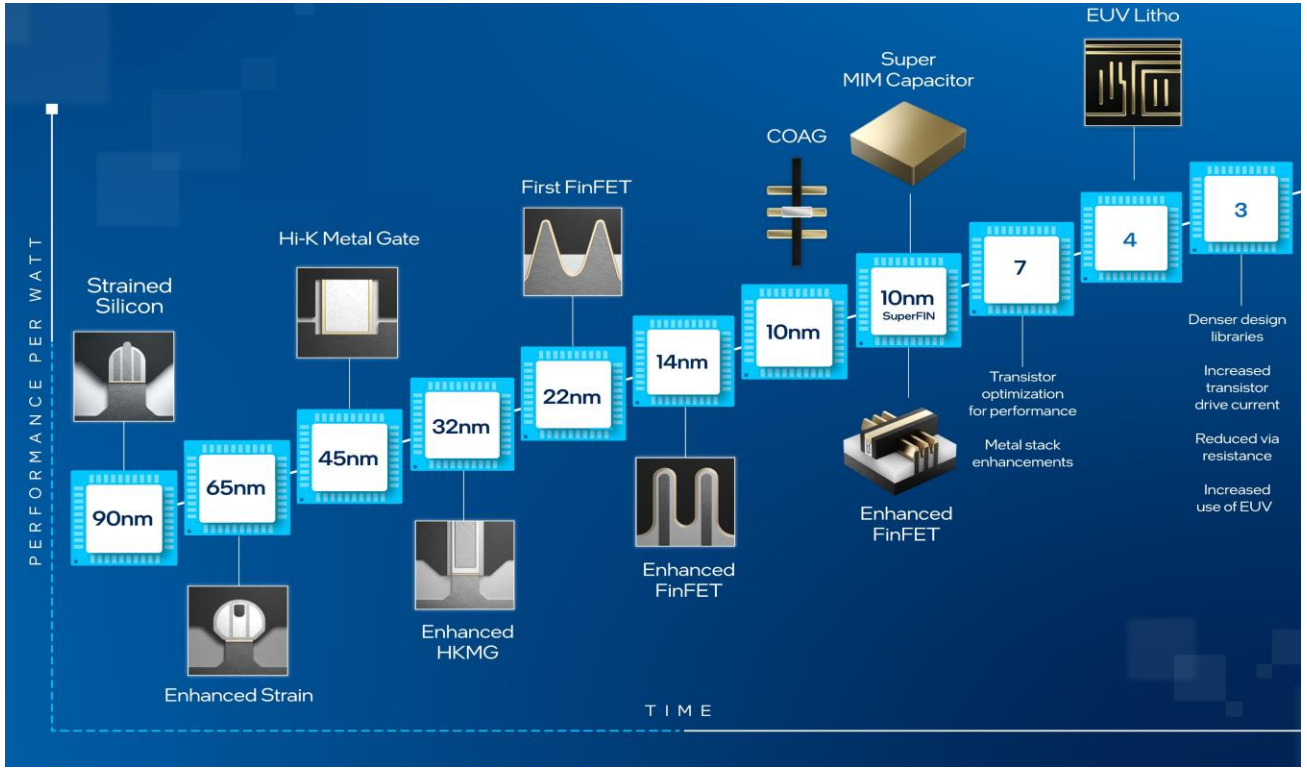
Outline

- Introduction
- Motivation
- Test generation procedure
- Experiment Analysis
- Conclusion

Moore's law

- Complexity of designing increases, especially with lower technology nodes



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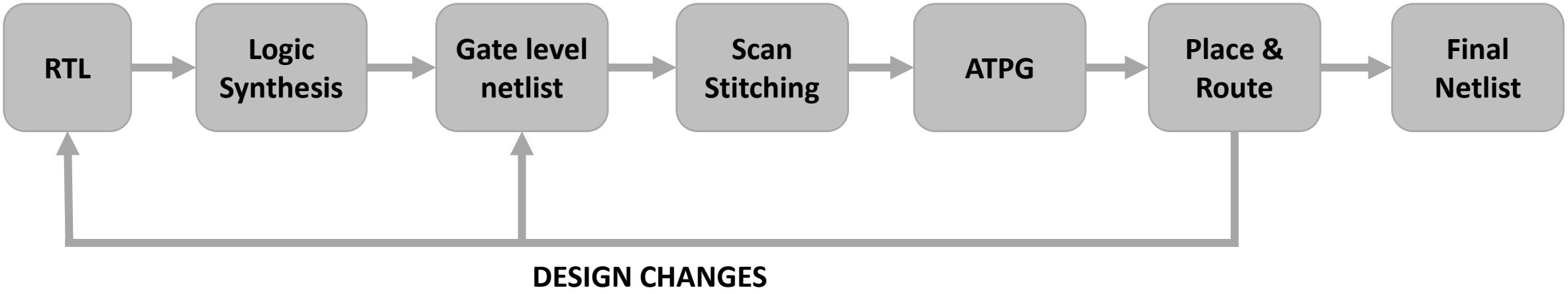
VLSI Design Flow

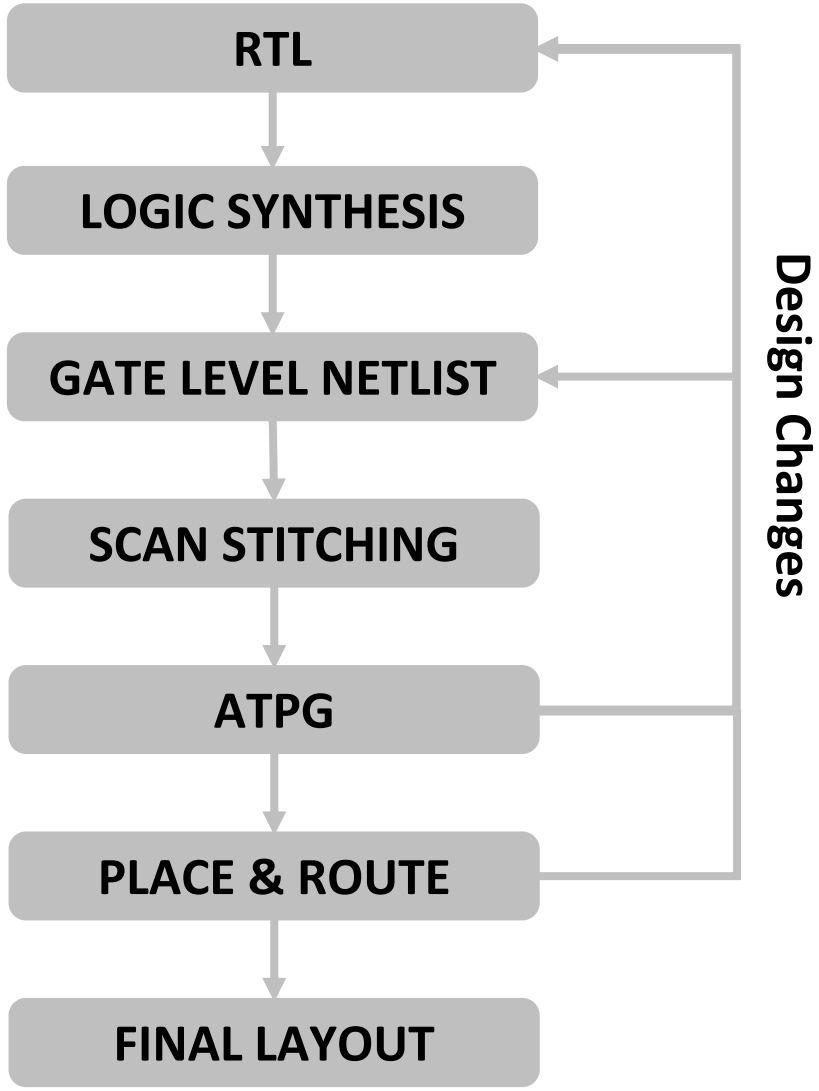
- Designing complex circuits consists of numerous steps



[1] H. Reyserhove and W. Dehaene, “Efficient Design of Variation-Resilient Ultra-Low Energy Digital Processors”, Springer, 2019
[2] K. Chakravadhanula et al., “Advancing test compression to the physical dimension,” 2017 IEEE International Test Conference (ITC), 2017, pp.1-10.

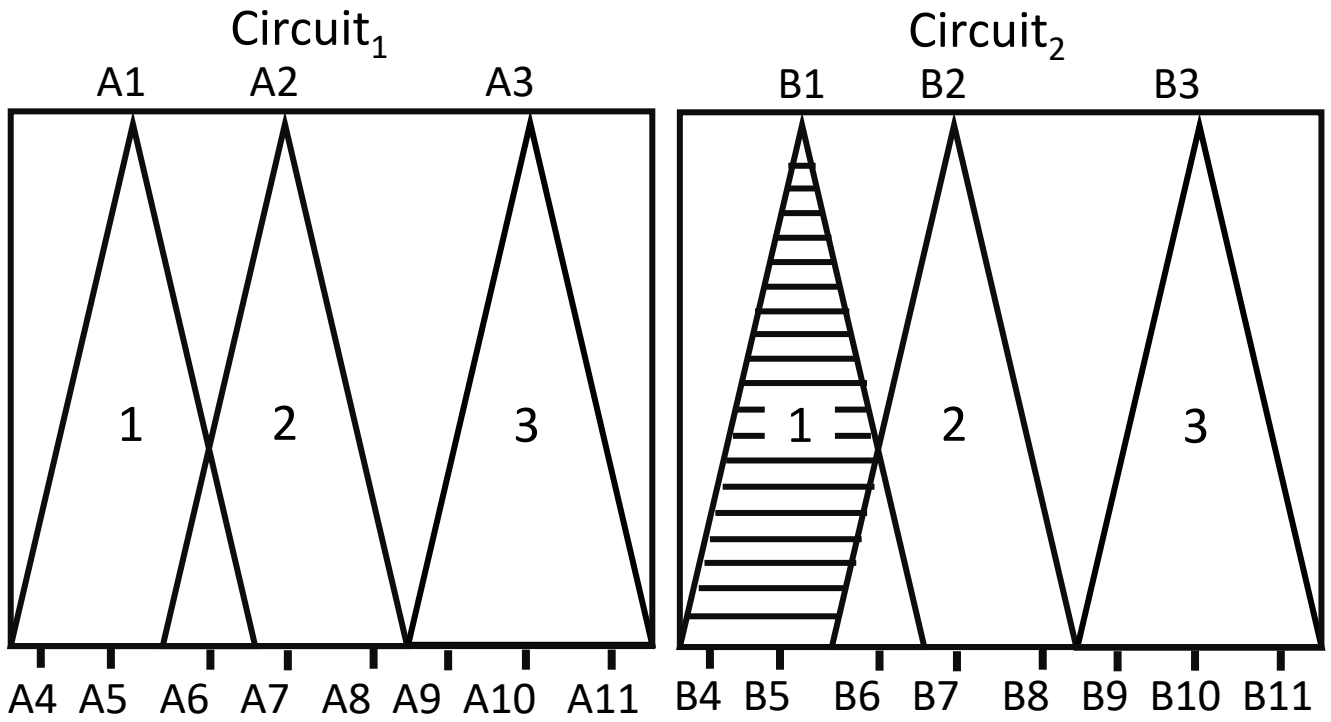
Test Generation

- At Gate-level netlist
- Iterations till Fault Coverage is met
  - Iteration 1: Test Pattern Generation
  - Iteration 2: Test Pattern Generation
- ATPG run from scratch on a modified netlist



Testability of a structurally similar circuit

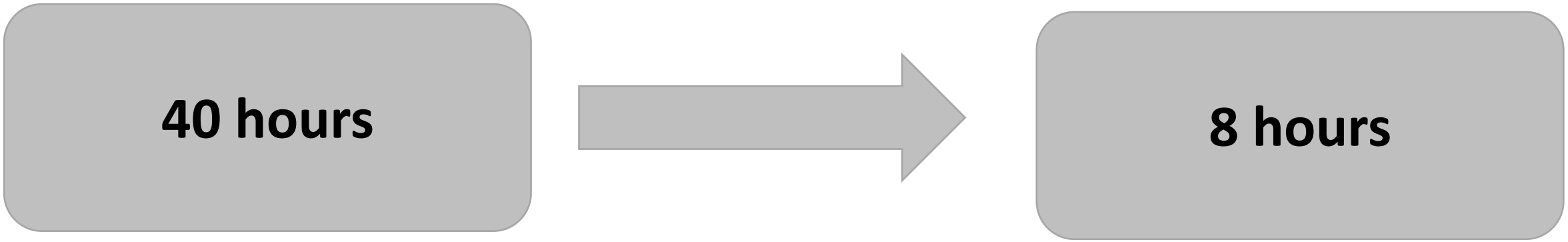
- $Circuit_1$: original circuit
- $Circuit_2$ has some changes
- Testability of $circuit_2$



Motivation

- Structural similarity between circuits is not utilized

- After a modification done at RTL, the entire test generation is run from the beginning to determine the testability of the circuit

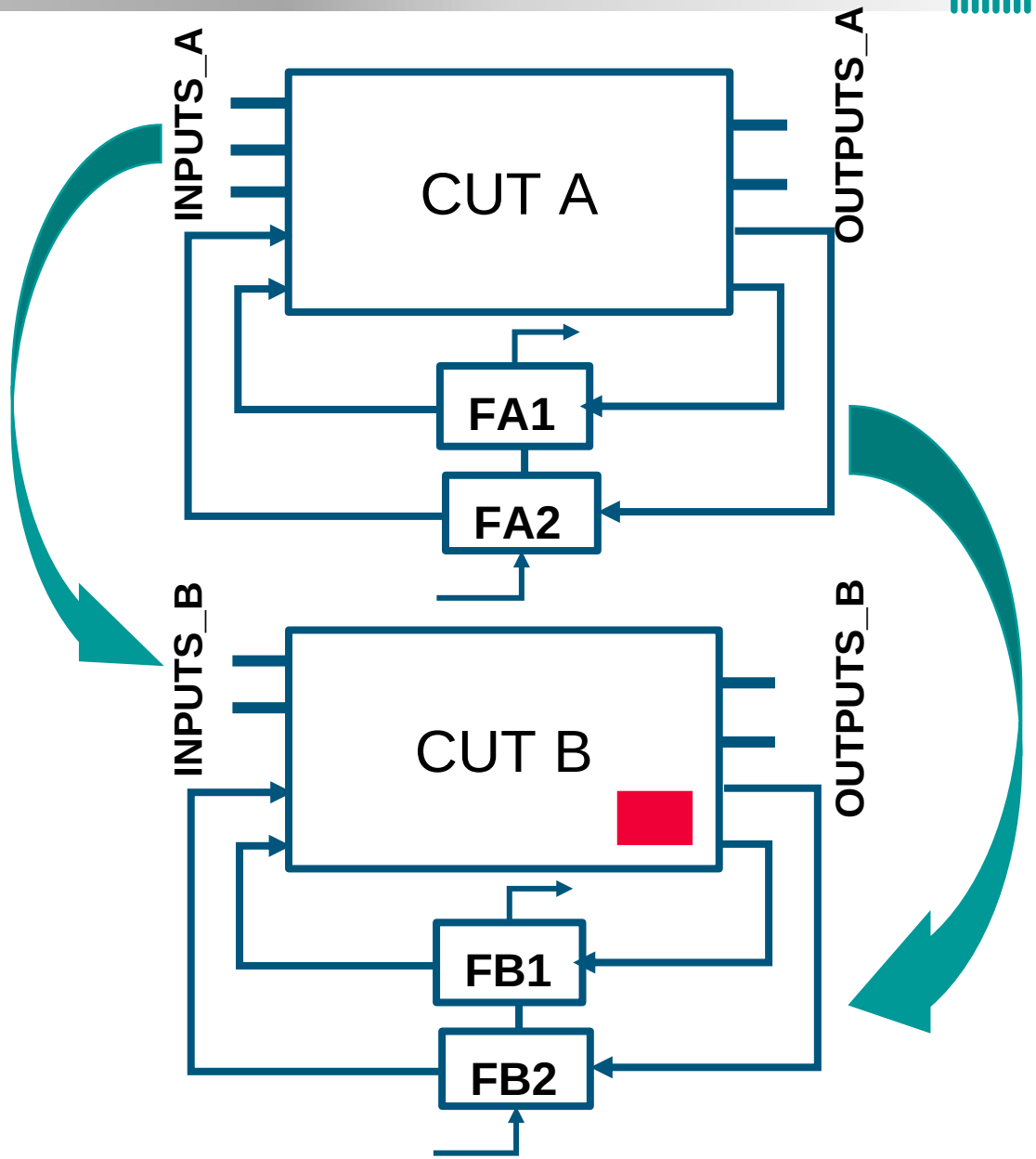


How can we reduce the time?

Establish mapping between $circuit_A$ & $circuit_B$

Transform the test pattern set T_A to T_B and fault simulate

Incremental ATPG on the undetected faults from modified cones



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Requirements for the Algorithm

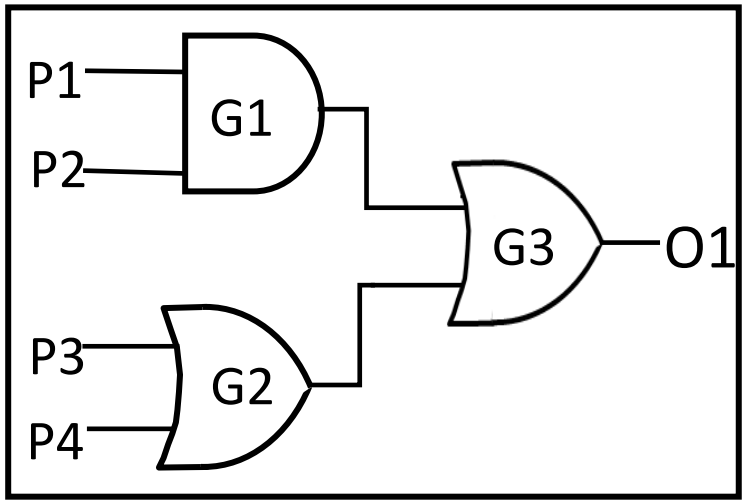
- Depend on the structural property of the design
- Signature Analysis [1] :
  - An integer-arithmetic based computation done on each gate of a logic cone [2]
  - Output and input signatures
  - Forward or backward traversal of cone

[1] J. Joe, N. Mukherjee, I. Pomeranz and J. Rajski, “Fast Test Generation for Structurally Similar Circuits,” 2022 VLSI Test Symposium (VTS), Sandiego, USA, 2022
[2] A. Dutta, N. Tuttle and K. Anandh,“Canonical ordering of instances to immunize the FPGA place and route flow from ECO-induced variance,”International Symposium on Quality Electronic Design (ISQED), Santa Clara, CA, 2013, pp. 359-363

How signature captures a cone's structure!

$$\text{Rotate}\left(\sum_{j}\left(\text{Rotate}\left(\text{Output Signature of fanin}_j\text{ of Gate}_i\right)\right) + \text{Group Gate Mask of Gate}_i\right)$$

- Independent of order
  - Addition of signature of gates



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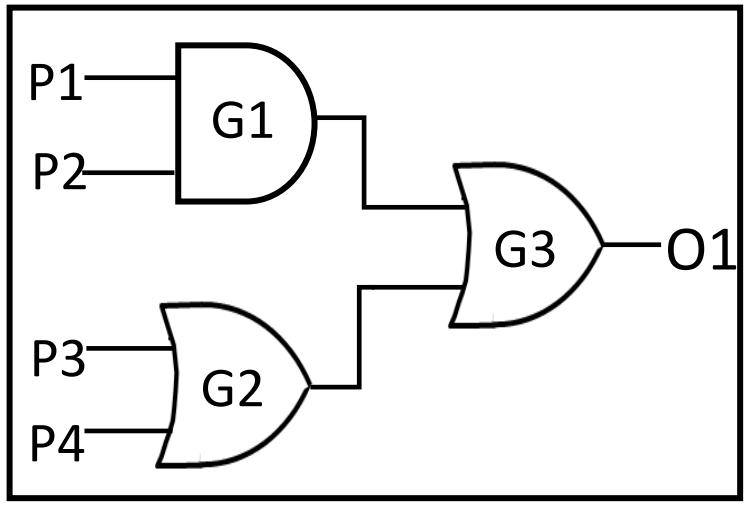
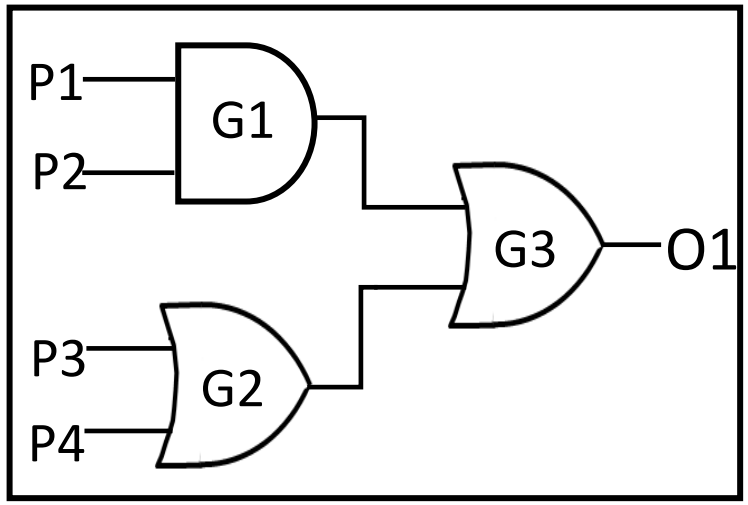
- Independent of order
  - Addition of signature of gates
- Level of a gate
  - Rotating the value of signature of gates



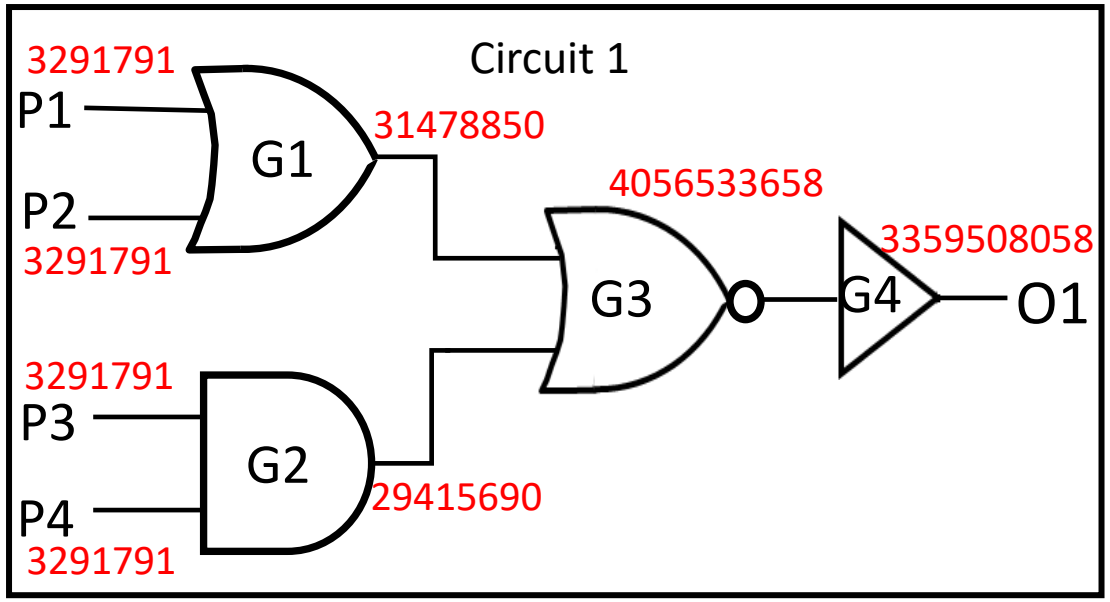
How signature captures a cone's structure!

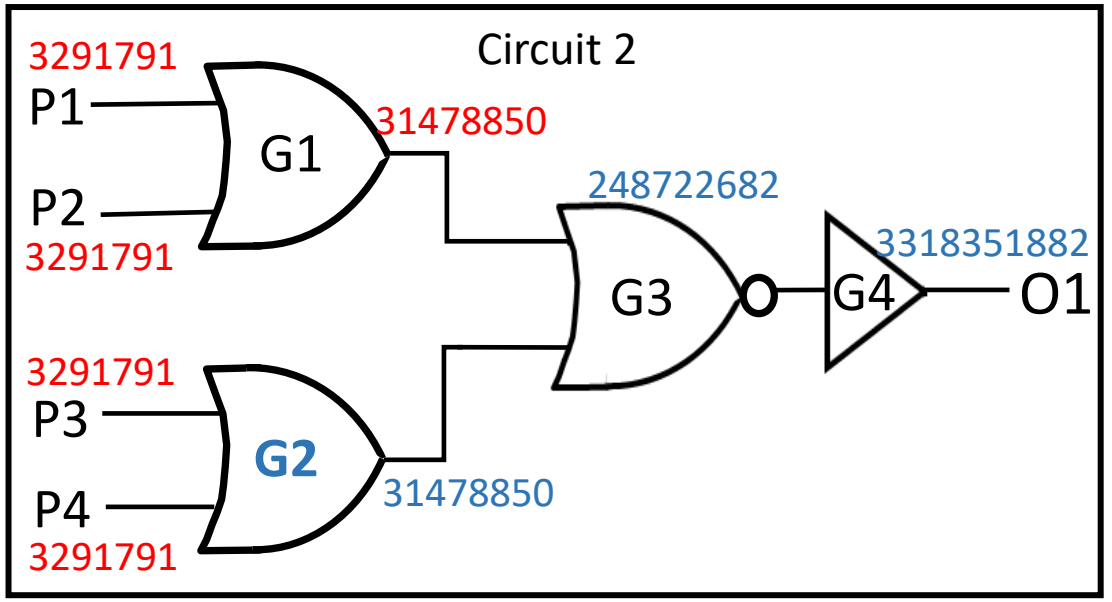
$$\text{Rotate}\left(\sum_{j}\left(\text{Rotate}\left(\text{Output Signature of fanin}_j\text{ of Gate}_i\right)\right) + \text{Group Gate Mask of Gate}_i\right)$$

- Independent of order
  - Addition of signature of gates
- Level of a gate
  - Rotating the value of signature of gates
- Gate type
  - A unique value called the mask is assigned for every gate type



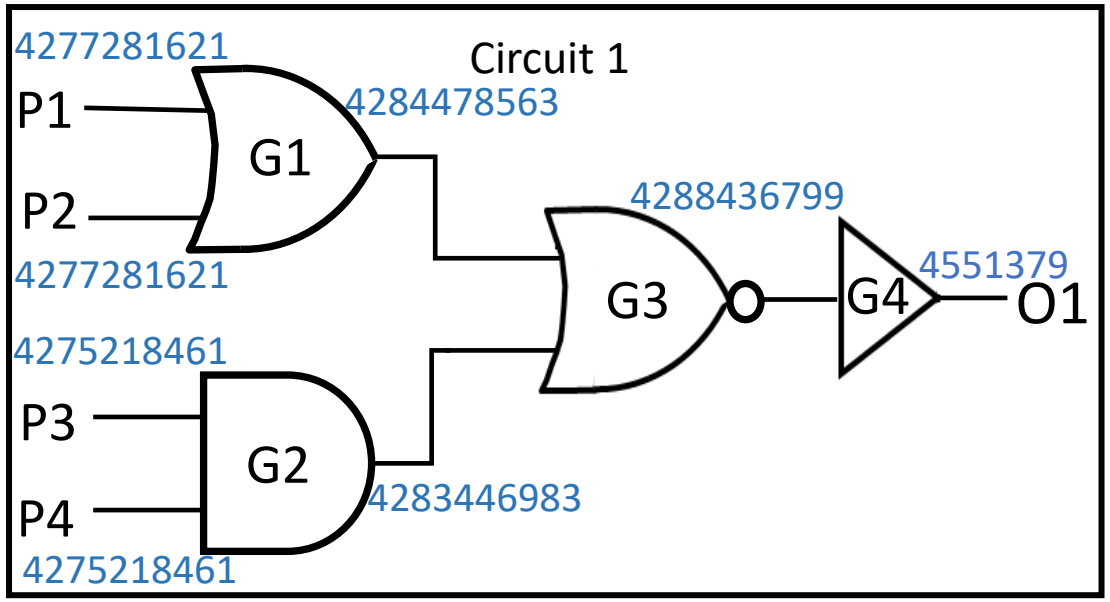
An example of signature computation

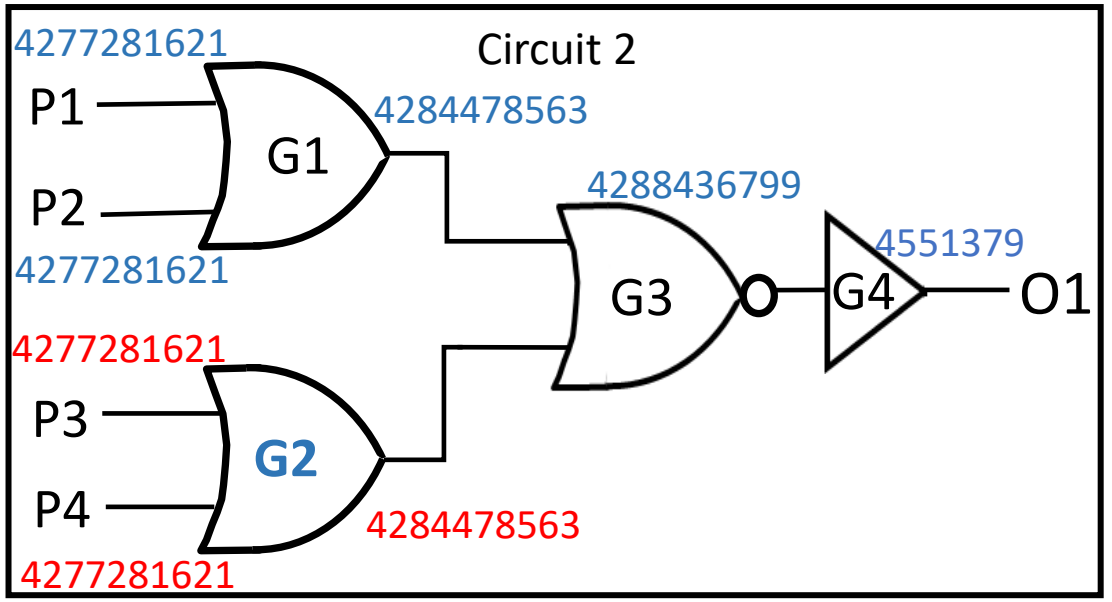




$$= \text{Rotate}\left(\sum_{i}(\text{Rotate}(\text{Output Signature of fanin of Gate}_i) + \text{Group Gate Mask of Gate}_i)\right)$$

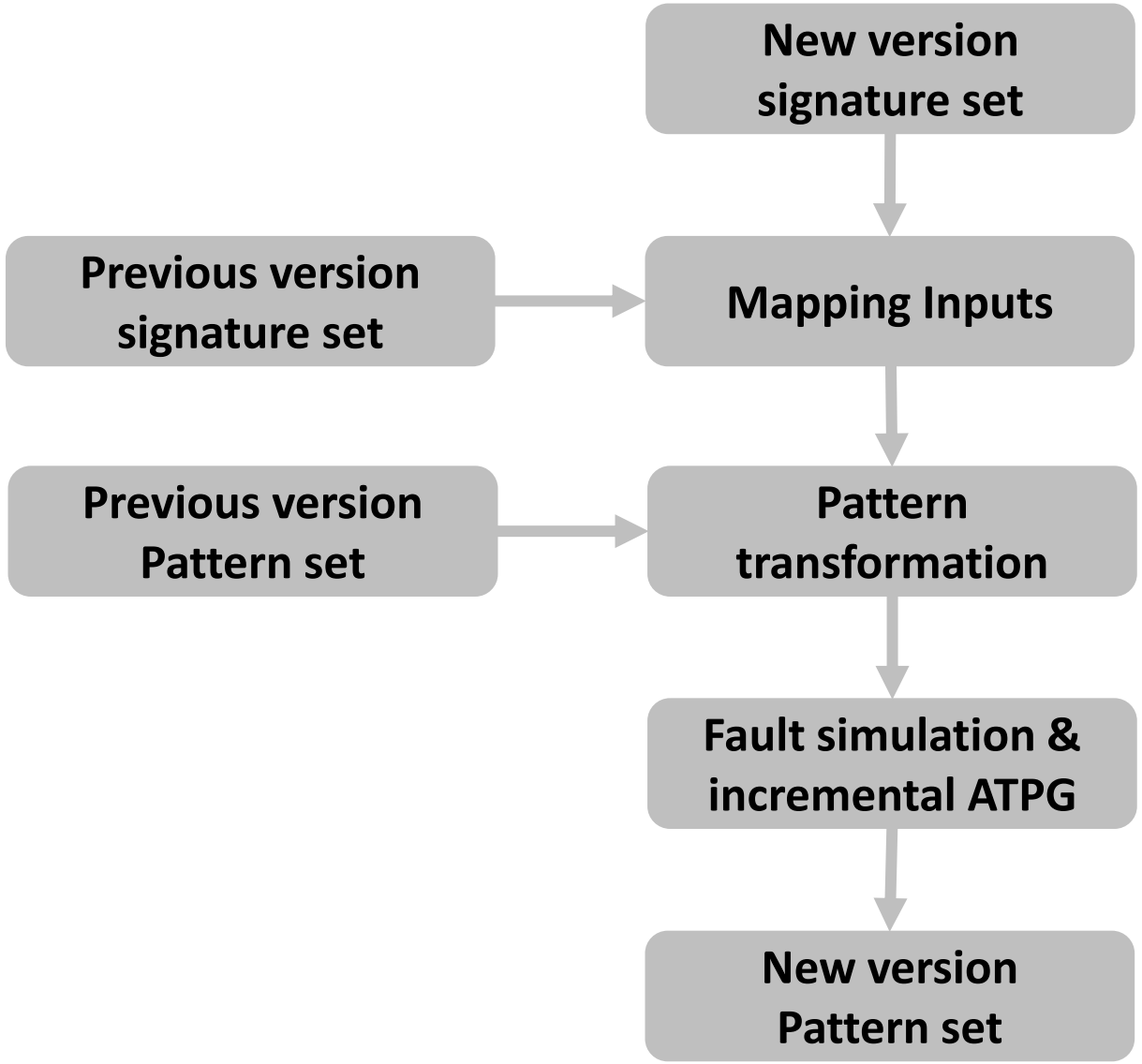
An example of signature computation





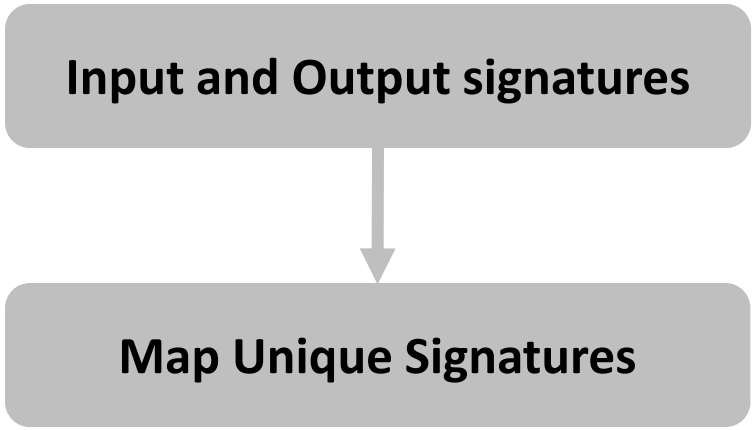
$$= \text{Rotate}\left(\sum_{i}(\text{Rotate}(\text{Output Signature of fanout of Gate}_i) + \text{Group Gate Mask of Gate}_i)\right)$$

Overview of ATPG Flow



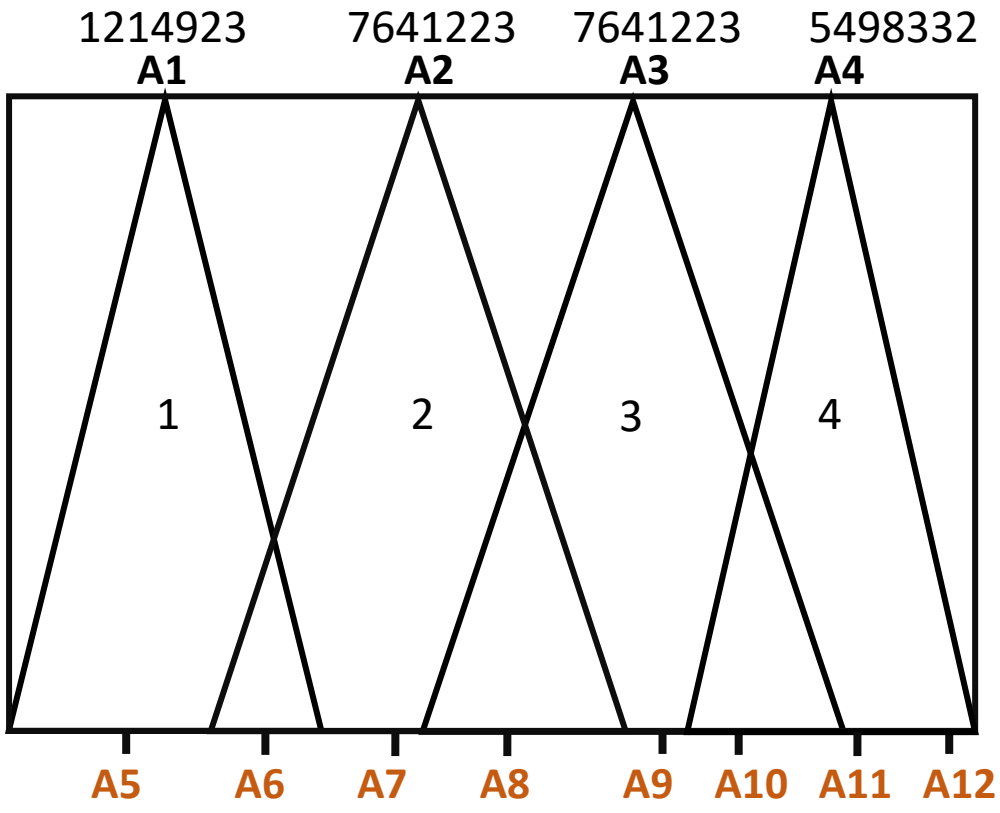
[1] J. Joe, N. Mukherjee, I. Pomeranz and J. Rajski, “Fast Test Generation for Structurally Similar Circuits,” 2022 VLSI Test Symposium (VTS), Sandiego, USA, 2022

Mapping of Inputs - Overview

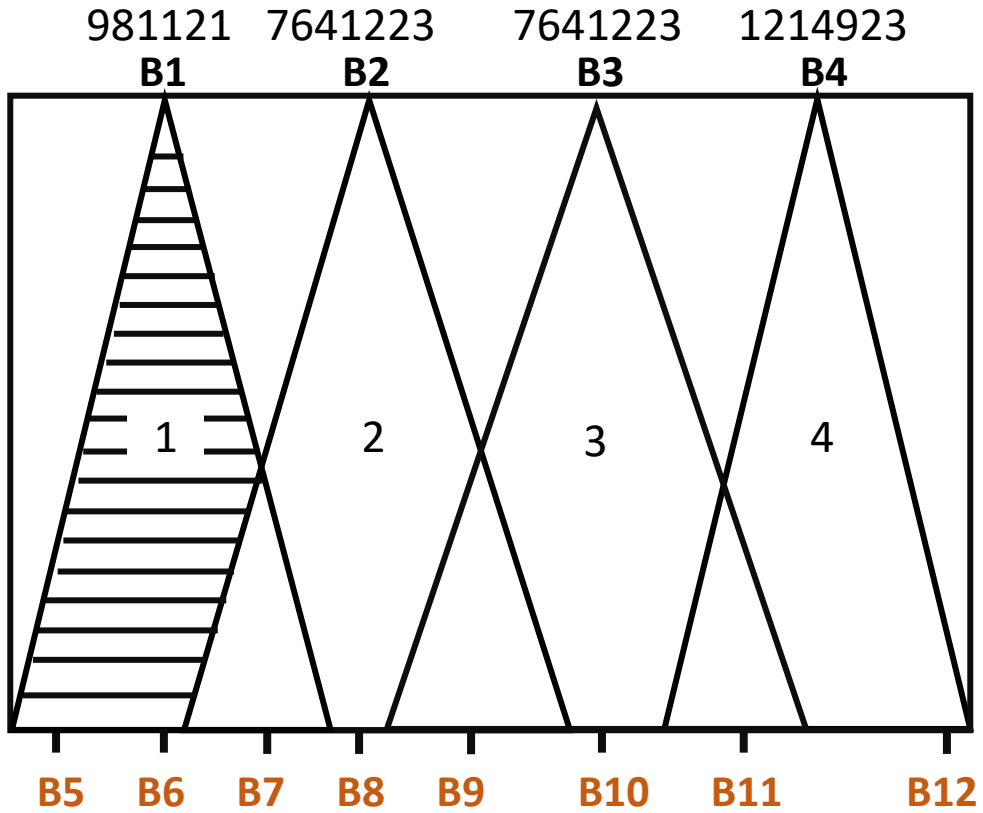


Unique Mapping

Circuit 1



Circuit 2



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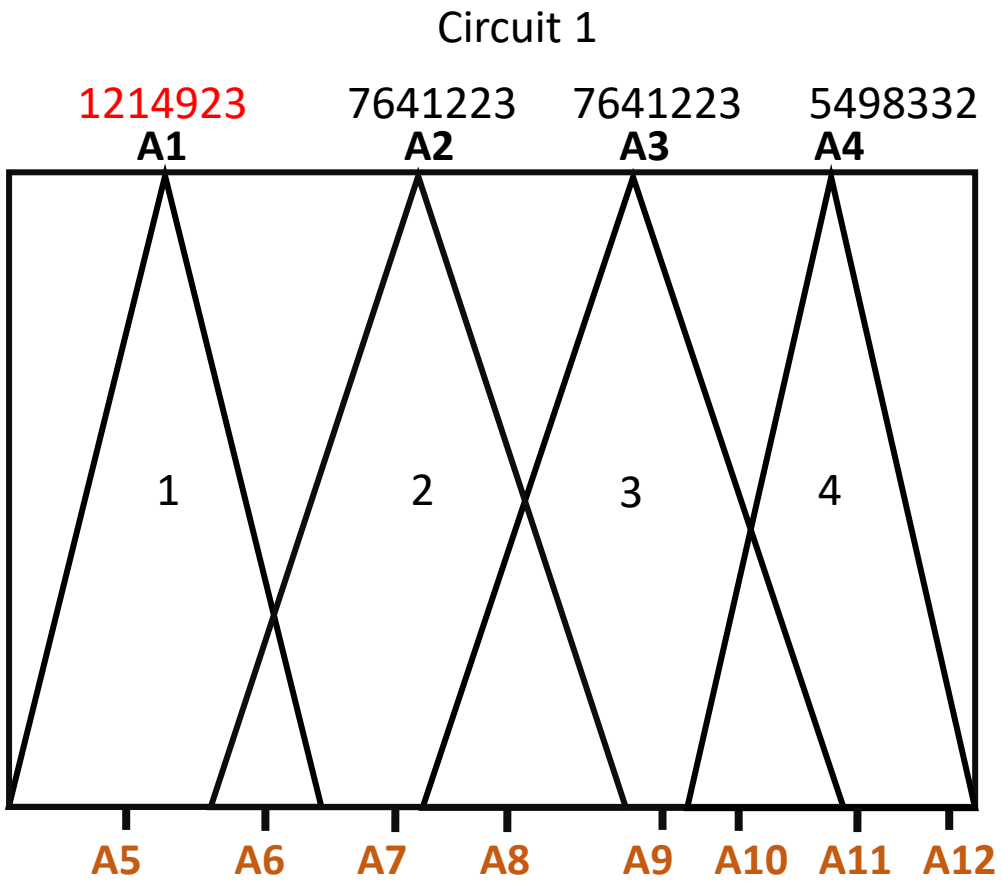

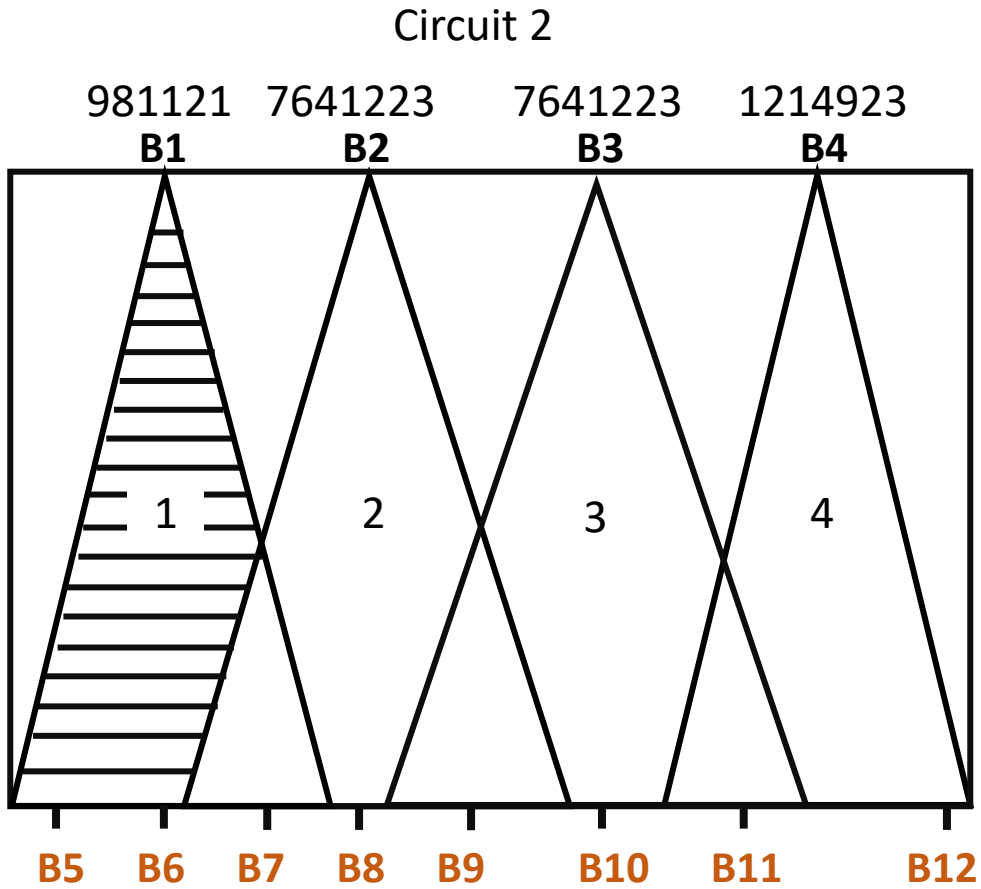

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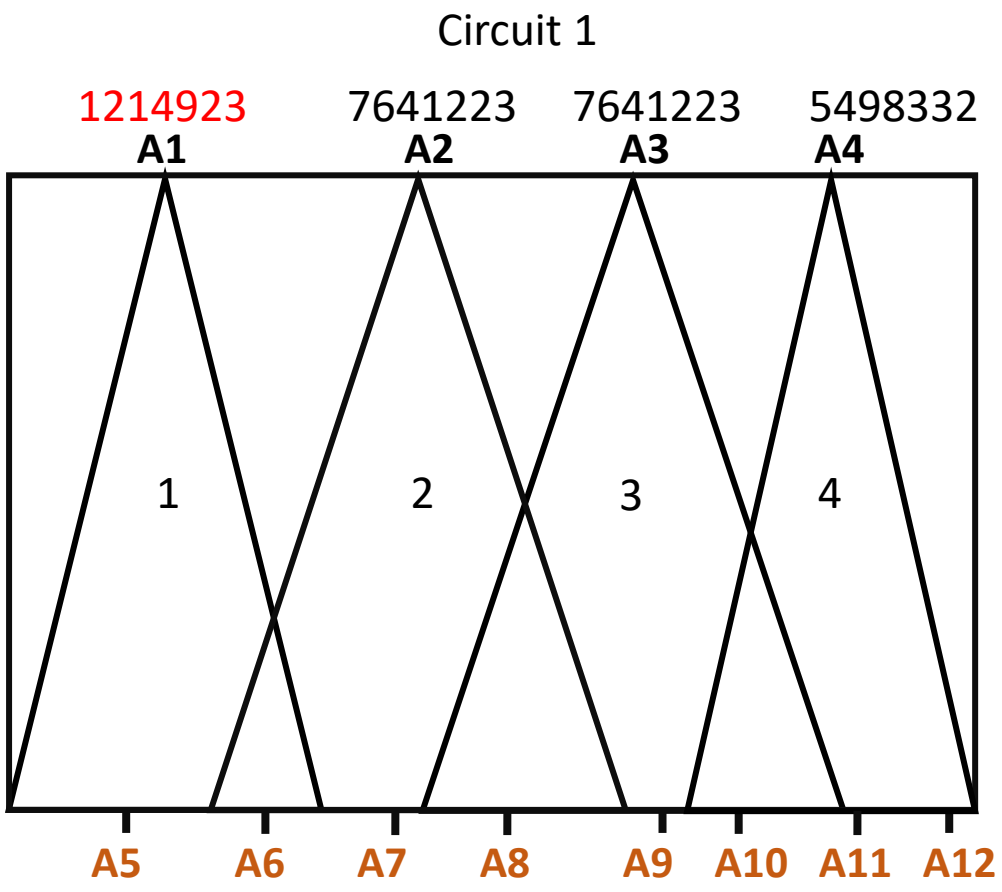

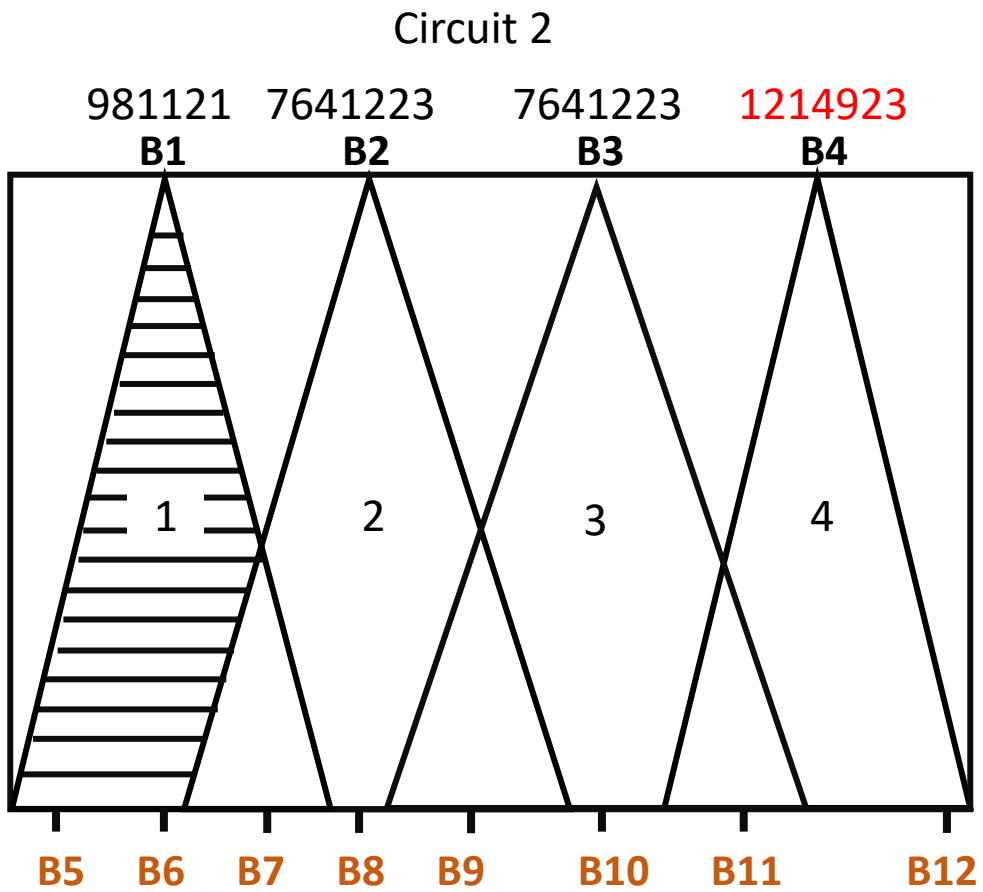

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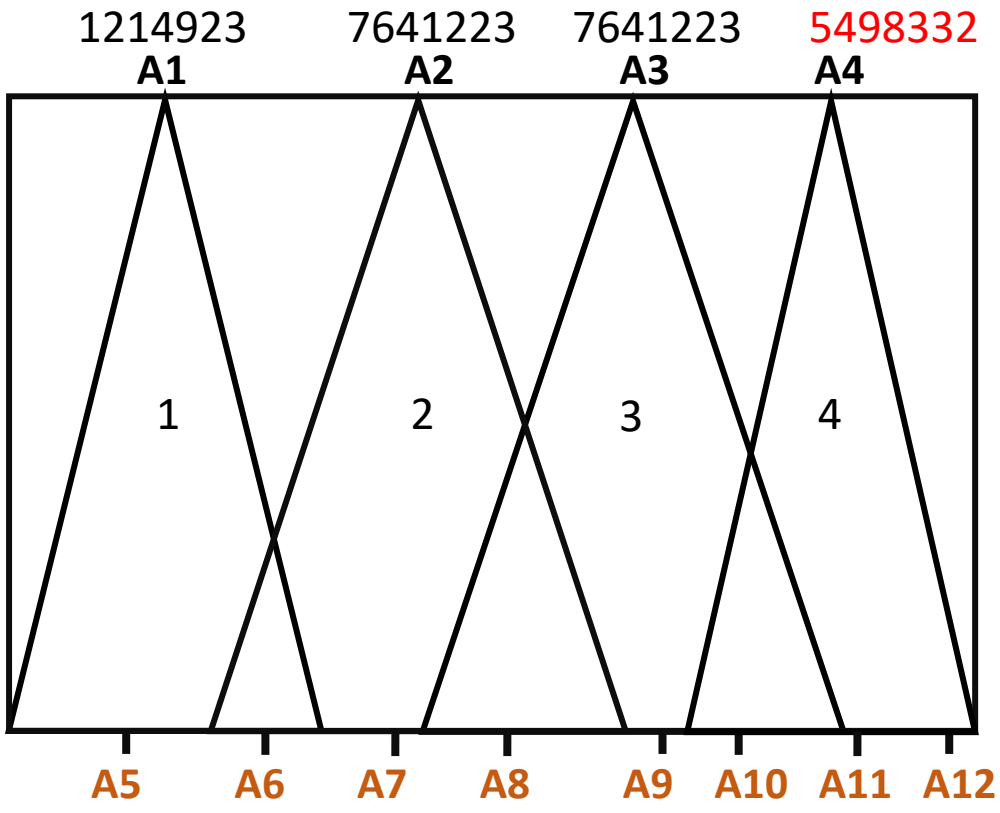
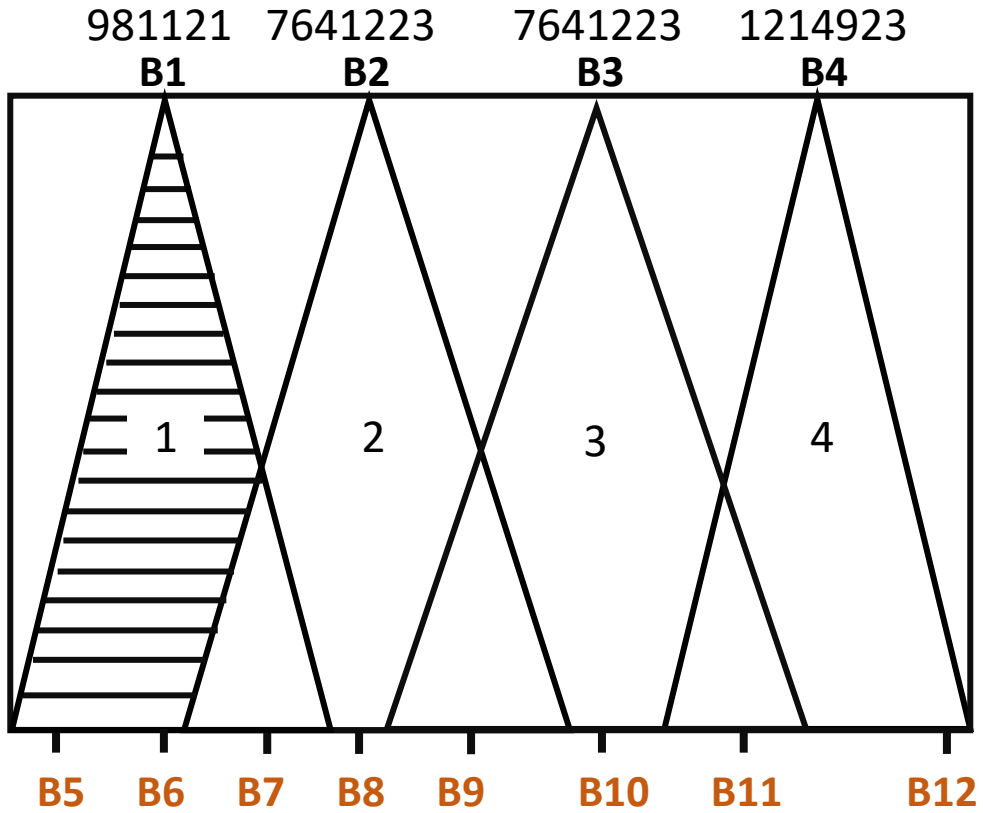


Circuit 2



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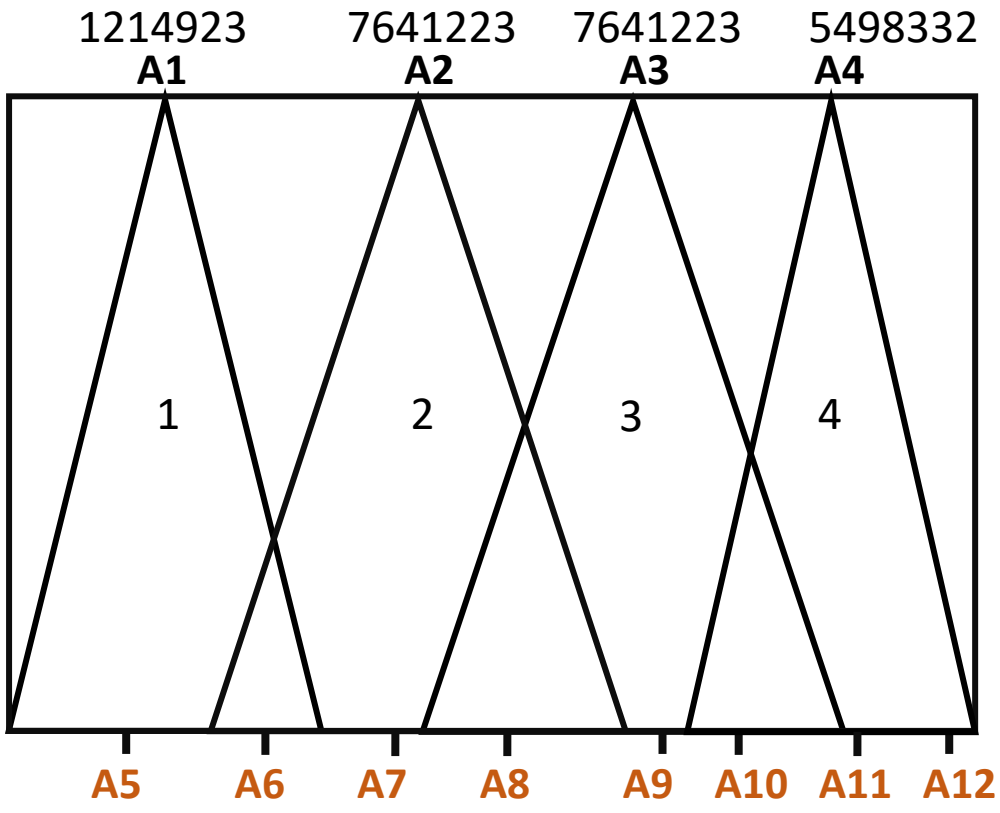
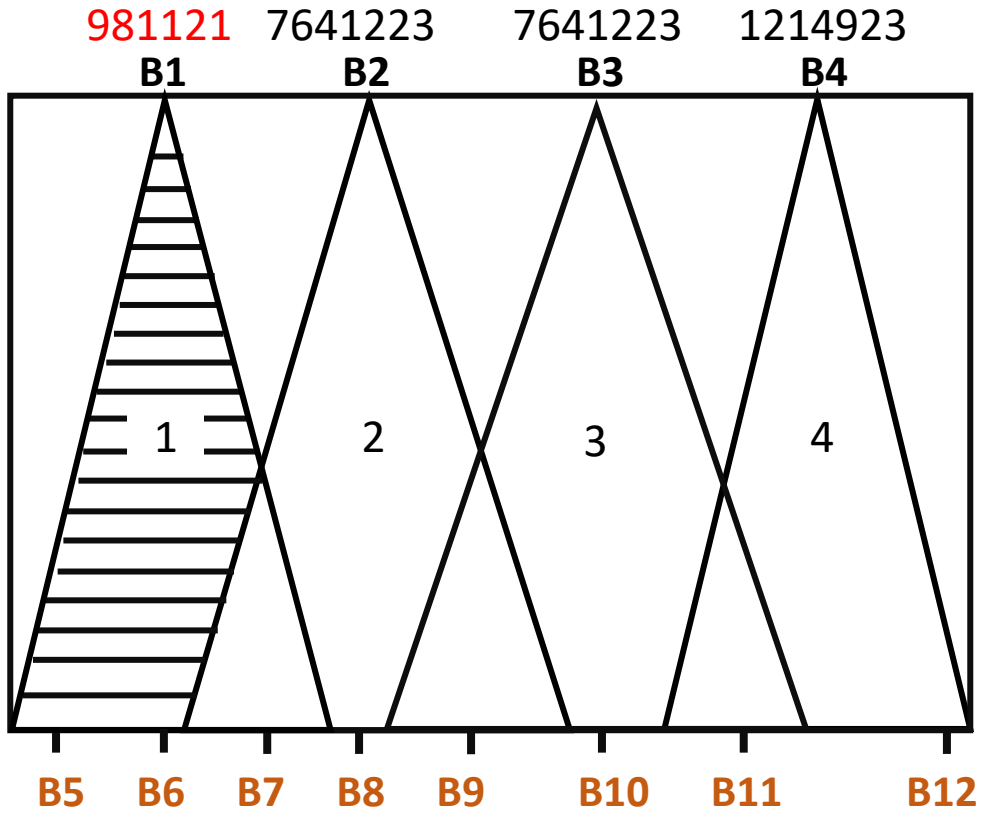


Circuit 2



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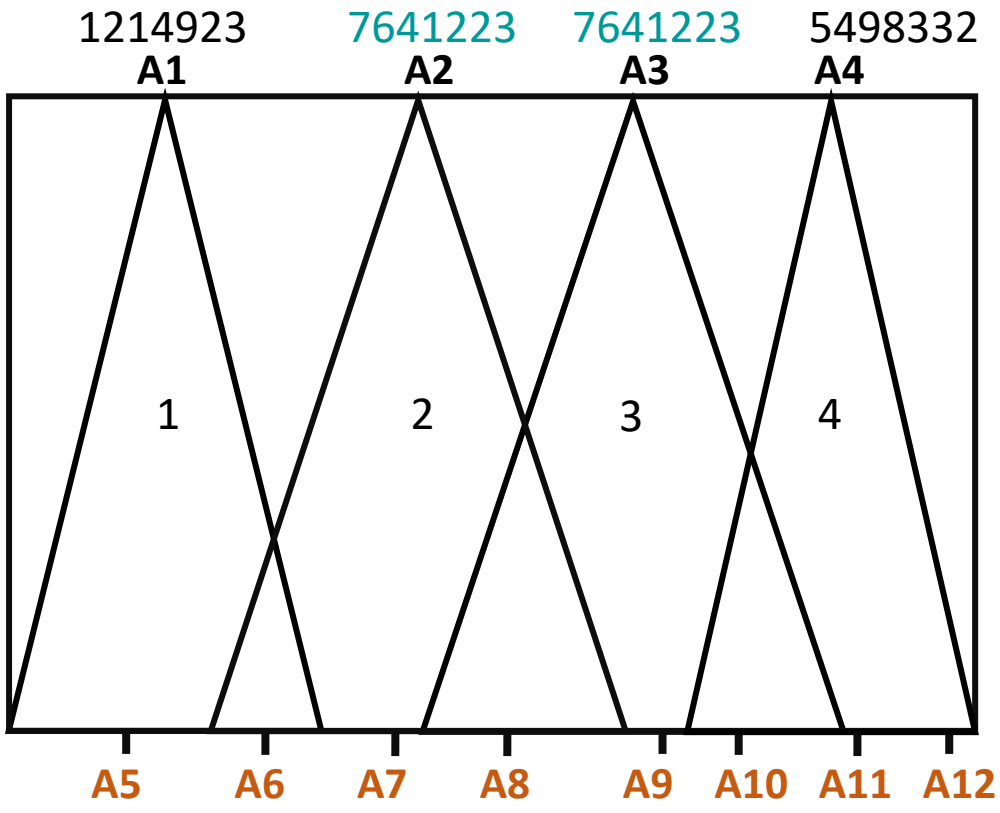
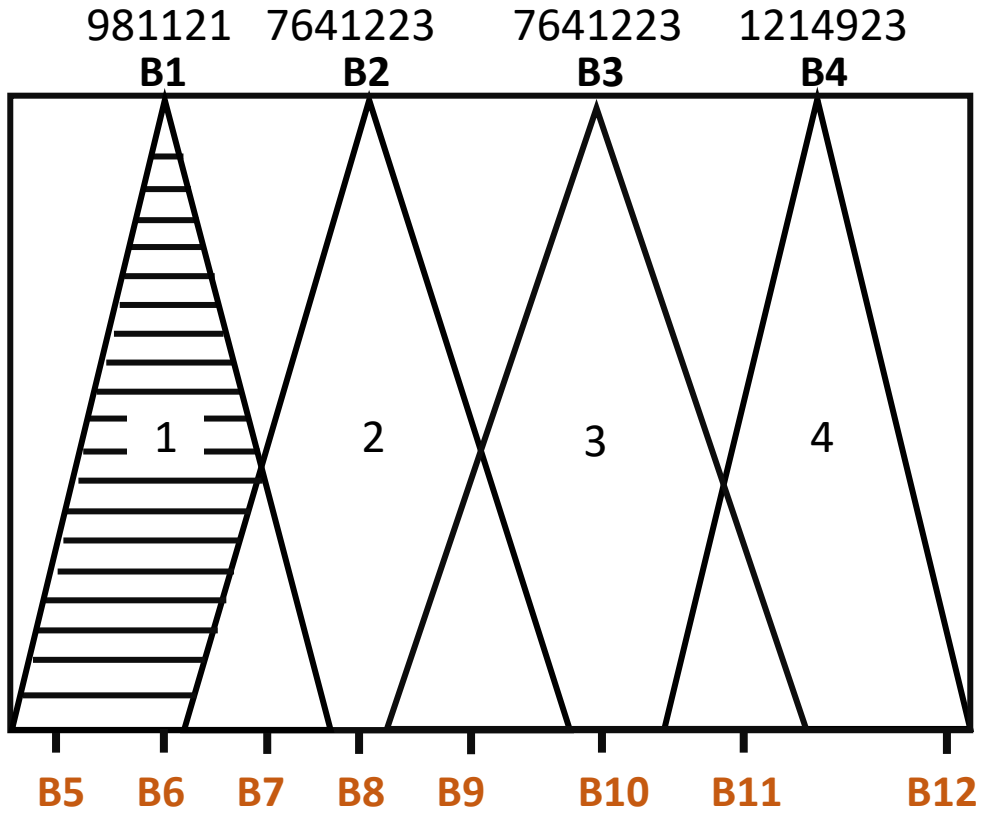


Circuit 2



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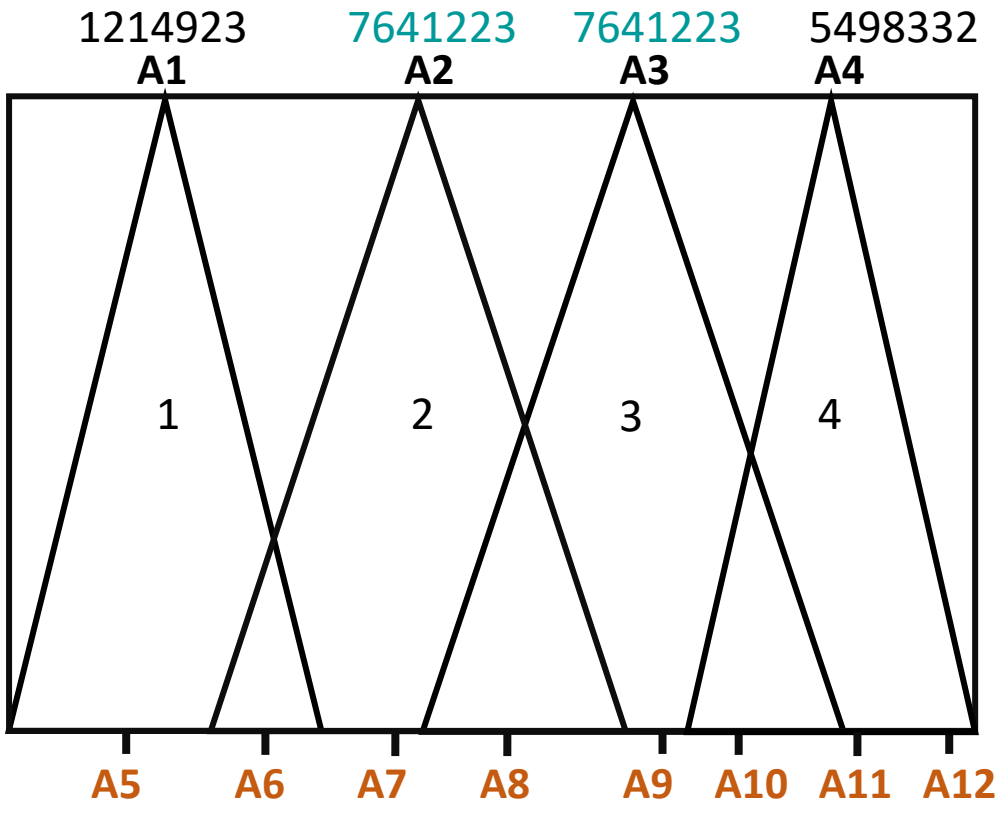
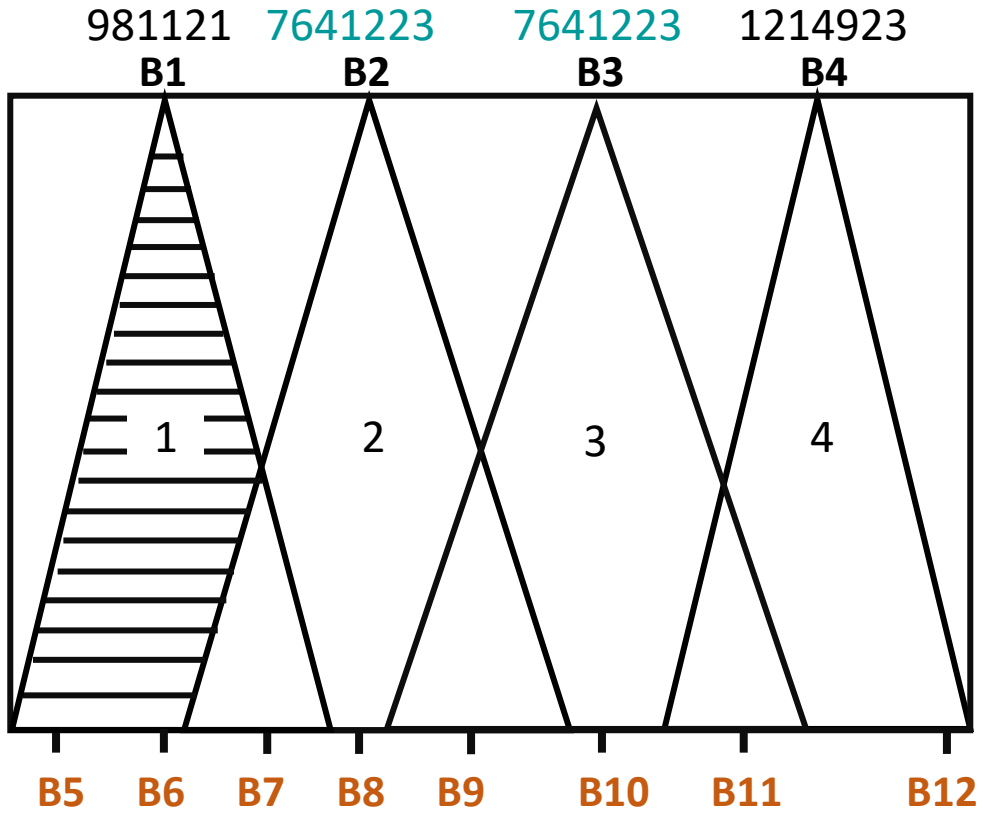


Circuit 2



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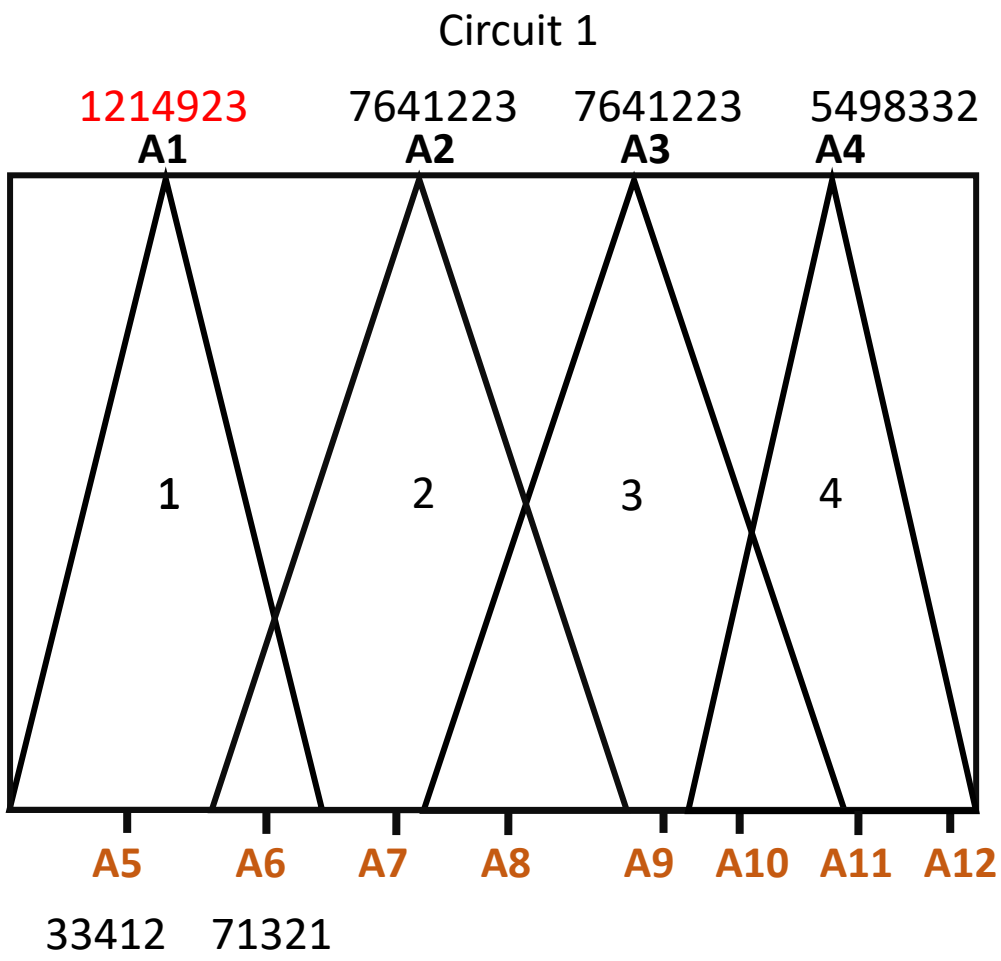

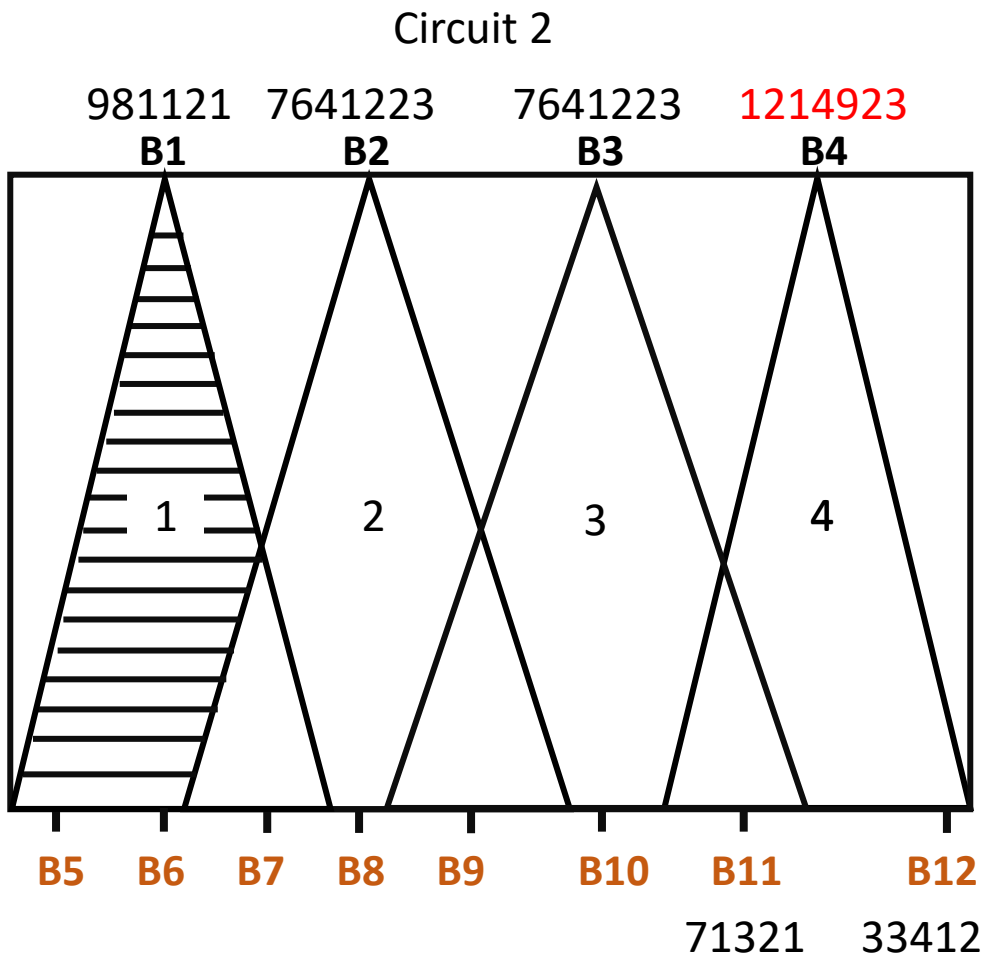

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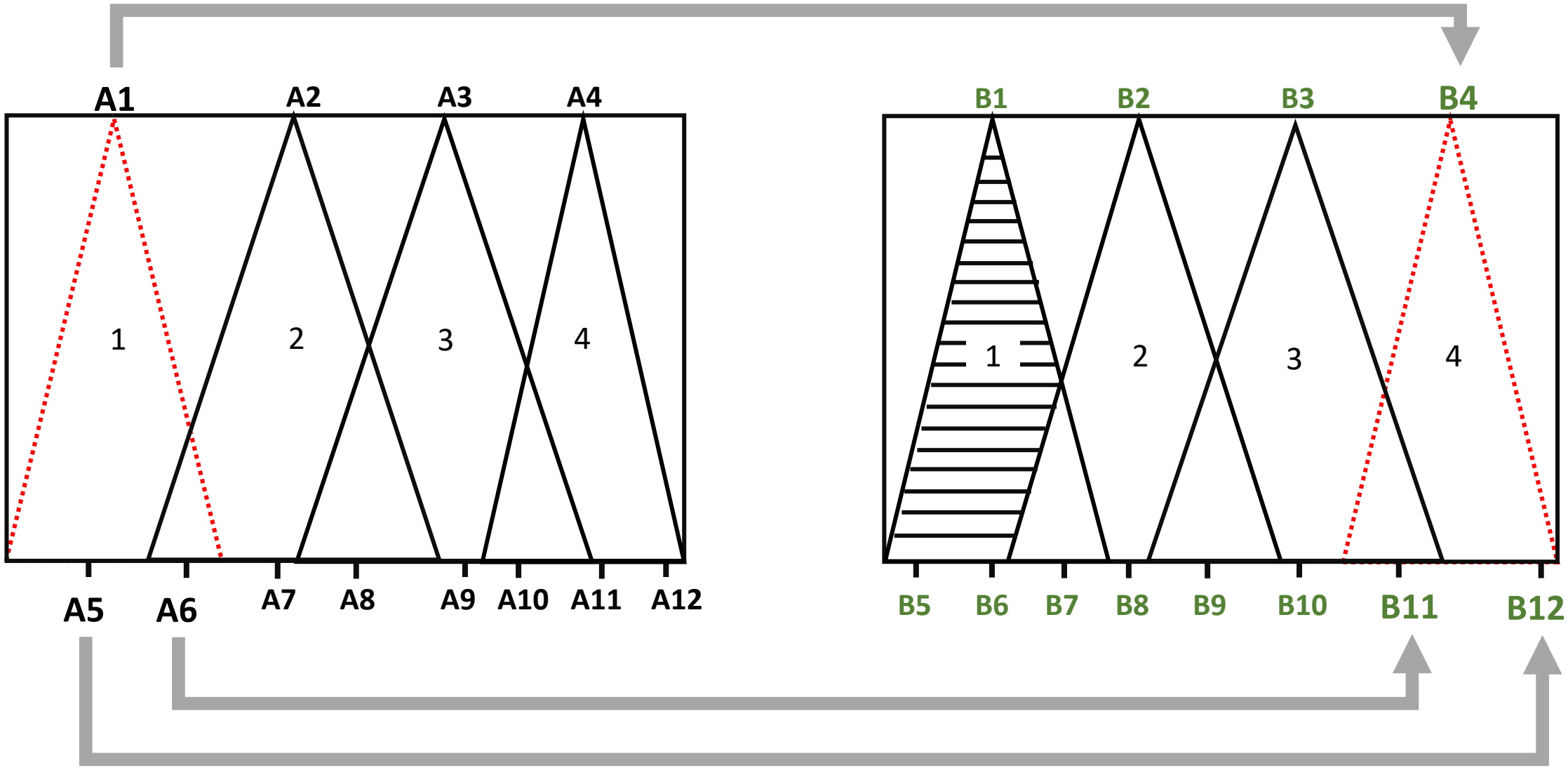

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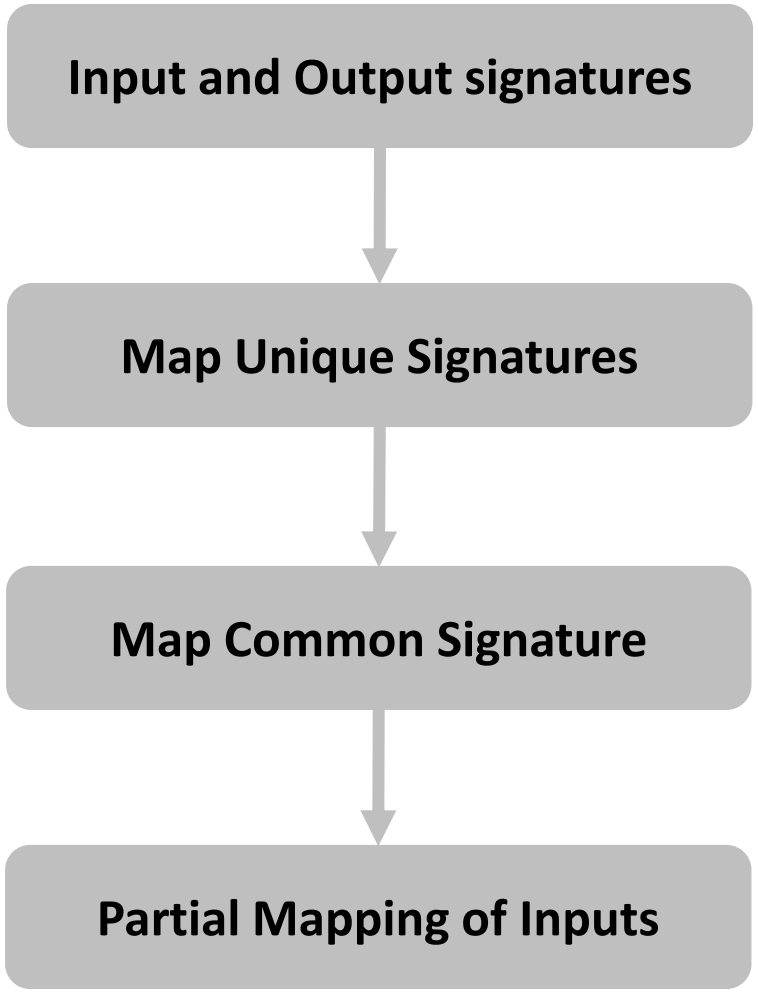
Mapping of Inputs - Contd



Transformation of a Pattern

Circuit 2	B1	B2	B3	B4	B5	B6	B7
Mapping	**A1**	x	**A4**	x	**A5**	**A6**	**A2**

Circuit 1	A1	A2	A3	A4	A5	A6	A7
Pattern	**1**	0	**0**	1	**1**	**1**	**1**

Circuit 2	B1	B2	B3	B4	B5	B6	B7
Transform	**1**	x	**1**	x	**1**	**1**	**0**

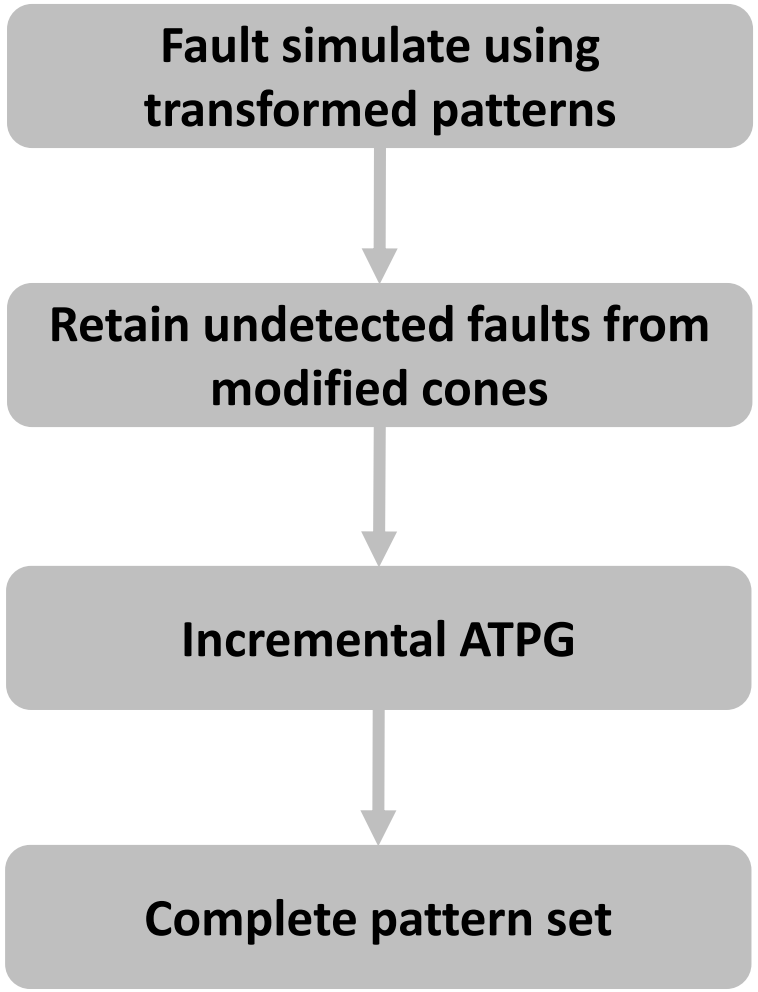
Transformation of a Pattern

Circuit 2	B1	B2	B3	B4	B5	B6	B7
Mapping	**A1**	x	**A4**	x	**A5**	**A6**	**A2**

Circuit 1	A1	A2	A3	A4	A5	A6	A7
Pattern	**1**	**0**	**0**	**1**	**1**	**1**	**1**

Circuit 2	B1	B2	B3	B4	B5	B6	B7
Transform	**1**	x	**1**	x	**1**	**1**	**0**
Random fill	**1**	1	**1**	0	**1**	**1**	**0**

Overview of Incremental ATPG



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Evaluation of test generation procedure

- Changes are done at RTL
- Addition or removal of logic gates and sequential cells
- 10 industrial digital circuits
- 10 different modification is done on each design

Average combinational and sequential changes

Circuit	Circuit 1	Average Change in New version	
	Size	Number of Gates	Number of Scan Cells
D1	1,521,890	4,276	6
D2	968,281	2,366	5
D3	5,266,903	1,585	5
D4	2,369,026	1,604	6
D5	6,411,557	1,474	6
D6	1,121,605	1,230	4
D7	1,089,511	10,527	4
D8	1,492,011	2,159	5
D9	3,836,692	9,935	5
D10	735,616	747	6

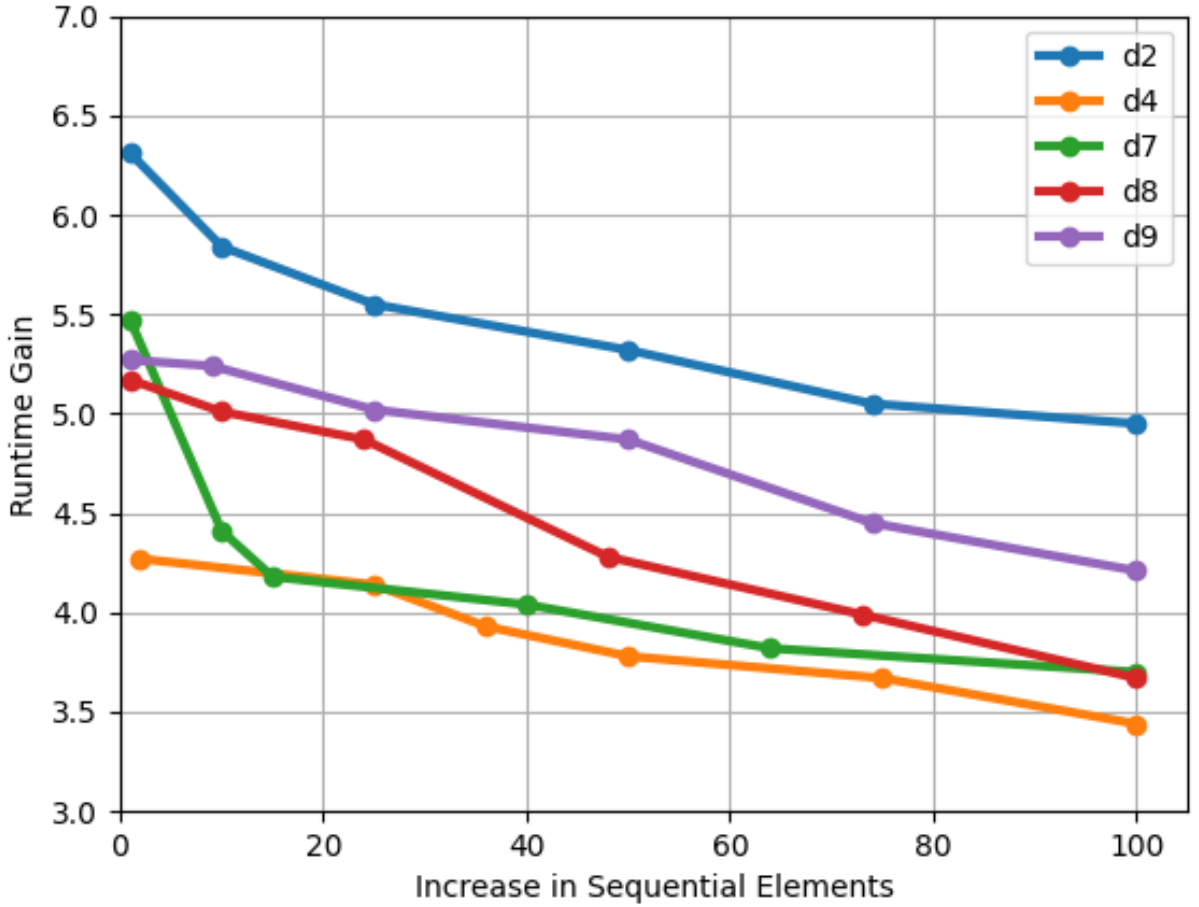
Results of RTL Changes

	Tot Cones in Circuit 1	Diff Cones in Circuit 2	Run Time(seconds)			Fault Coverage		Test Patterns		
			Circuit 1	Circuit 2	Gain ratio	Circuit 1	Circuit 2	Circuit 1	Circuit 2	Increase (%)
D1	113,172	6,756	512	113	4.53	94.76	94.76	8,751	11,290	29.01
D2	48,162	5,309	399	51	7.82	93.41	93.41	4,656	6,167	32.45
D3	255,025	3,818	1,892	433	4.37	95.63	95.63	5,682	6,758	18.94
D4	119,069	13,146	481	76	6.33	96.61	96.69	2,874	3,642	26.72
D5	294,863	3,847	1,198	245	4.89	94.12	94.13	5,320	5,896	10.82
D6	52,931	3,296	321	56	5.73	94.76	94.76	4,519	4,767	5.49
D7	44,116	3,706	389	95	4.09	92.31	92.31	2,824	3,405	20.46
D8	86,854	4,920	312	62	5.03	93.72	93.71	2,461	3,251	32.10
D9	224,977	8,998	2,597	494	5.25	94.51	94.51	9,240	11,741	27.06
D10	37,337	3,129	386	104	3.71	98.55	98.55	1,856	2,217	19.45

Avg = 5.17x

Avg = 22.45%

Runtime gain for larger changes



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Conclusion

- A **fast** way to **determine the testability.**

- On average, more than a **5-fold** reduction in runtime.

Thank you