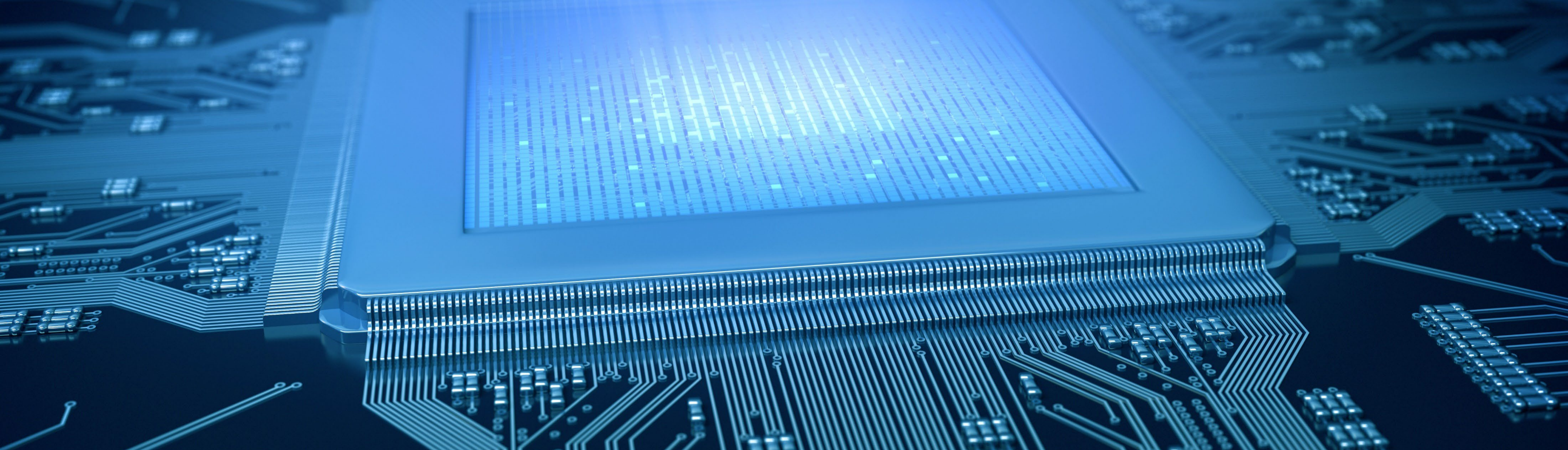

Adaptive DFT technology in use with ATE

Peter Orlando, Kacper Grubich

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Challenges of test on ATE

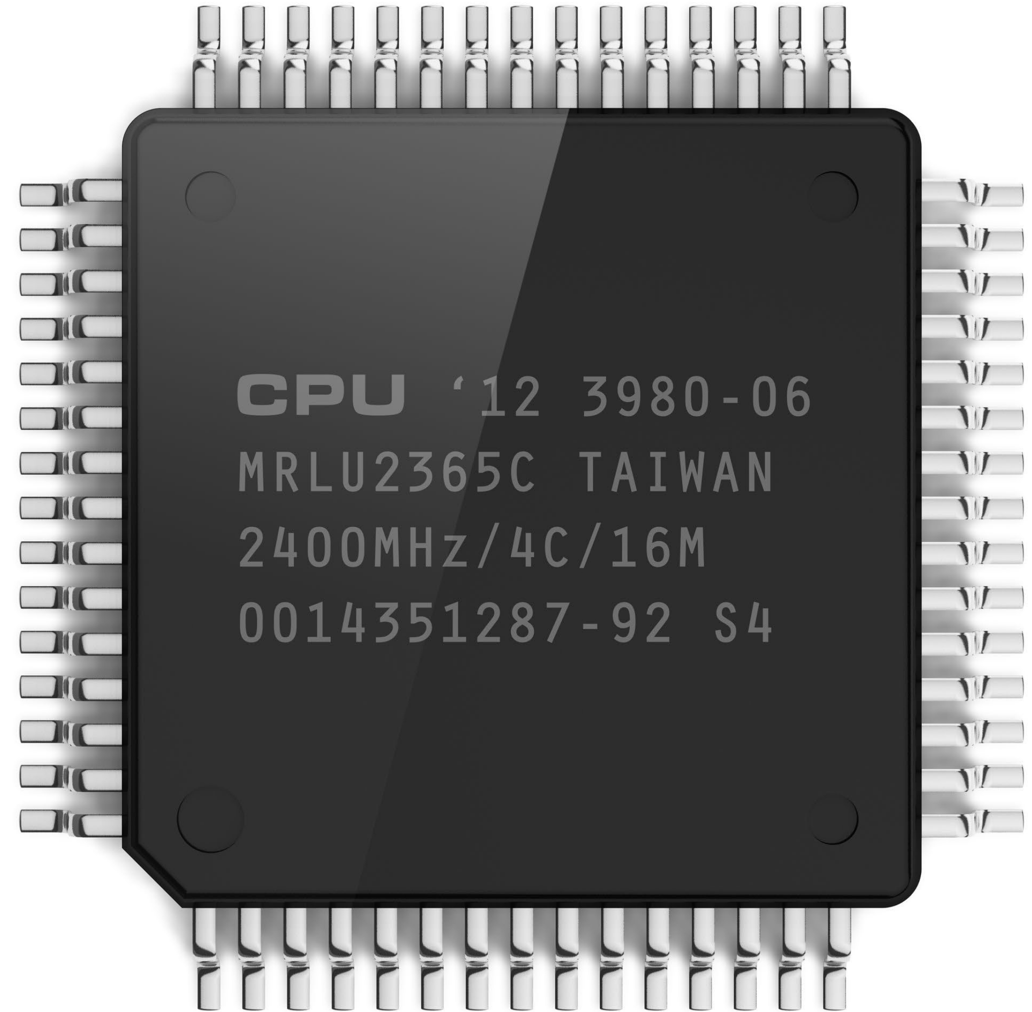
Growing complexity

Designs are growing in size and complexity

DFT required to meet those design complexities and quality standards

- Require minimal chip resources
- Efficiently provide access to test structure
- All fault models

While maintaining the ability to adapt to the conditions on the ATE



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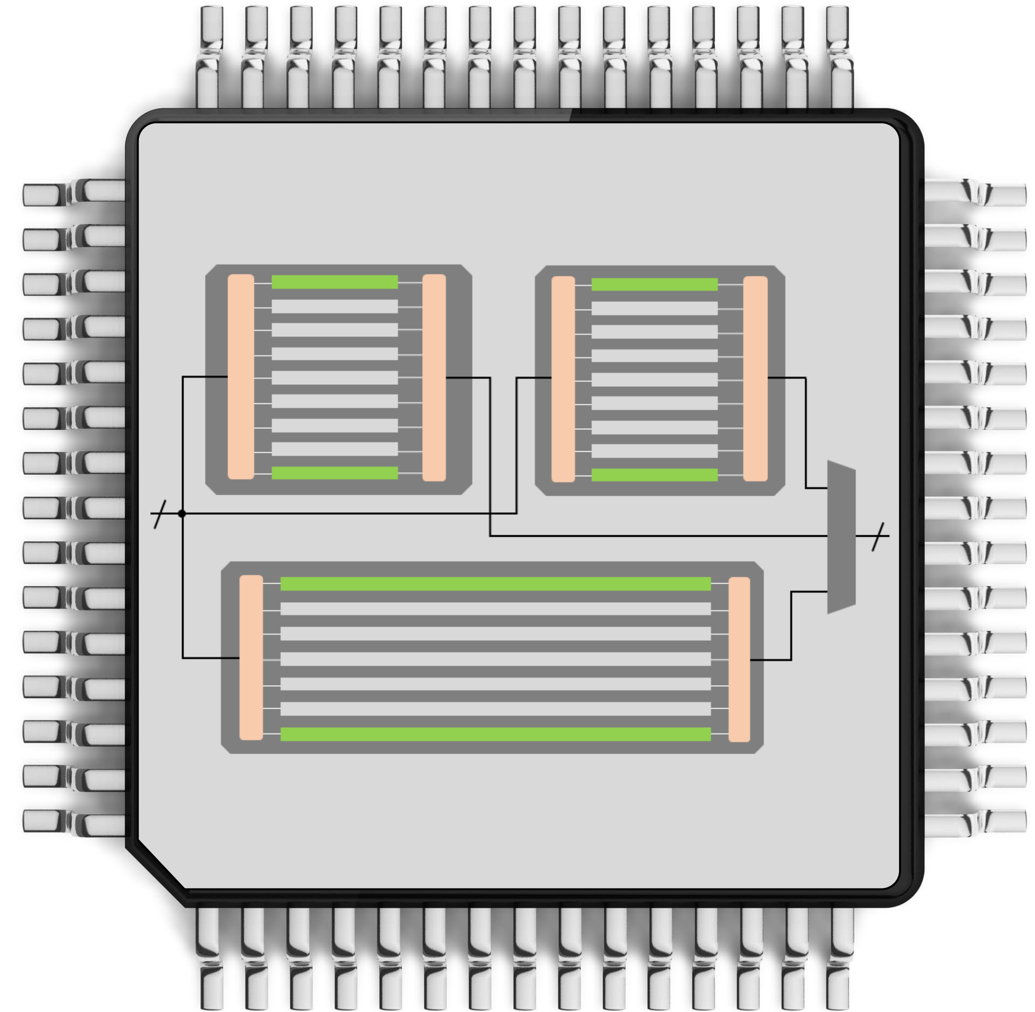
Challenges of test on ATE

Problems to consider

- Static programming
- Changes require pattern regeneration
- Inefficient use of resources for identical cores
- No flexibility – test time improvement, decreased power dissipation, etc.



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Scan Delivery Using Packetized, Bus-Based Networks

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Adapting to conditions on the ATE

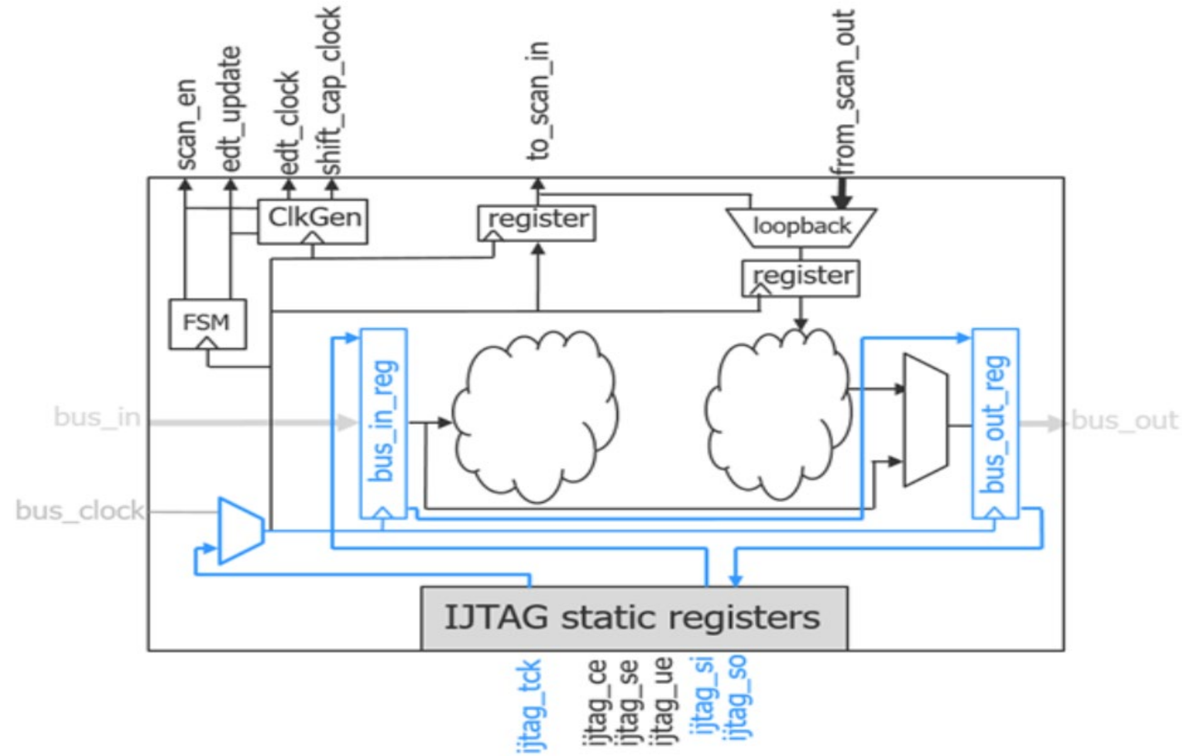

Fig.1 – Streaming through IJTAG

- ✓ Reuse IJTAG interface as streaming interface (*shown*)
- ✓ Cores to retarget at time of retargeting
- ✓ Change core shift timing at time of retargeting
- ✓ Scale the parallel bus even down to a single bit

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Not only for scan testing

- ✓ Support for Laser Voltage Imaging/Probing (LVI/LVX)
- ✓ Broadcast data to all scan chains or one specific scan chain
- ✓ Delivery of burn-in patterns
- ✓ Operation mode set with IJTAG protocol

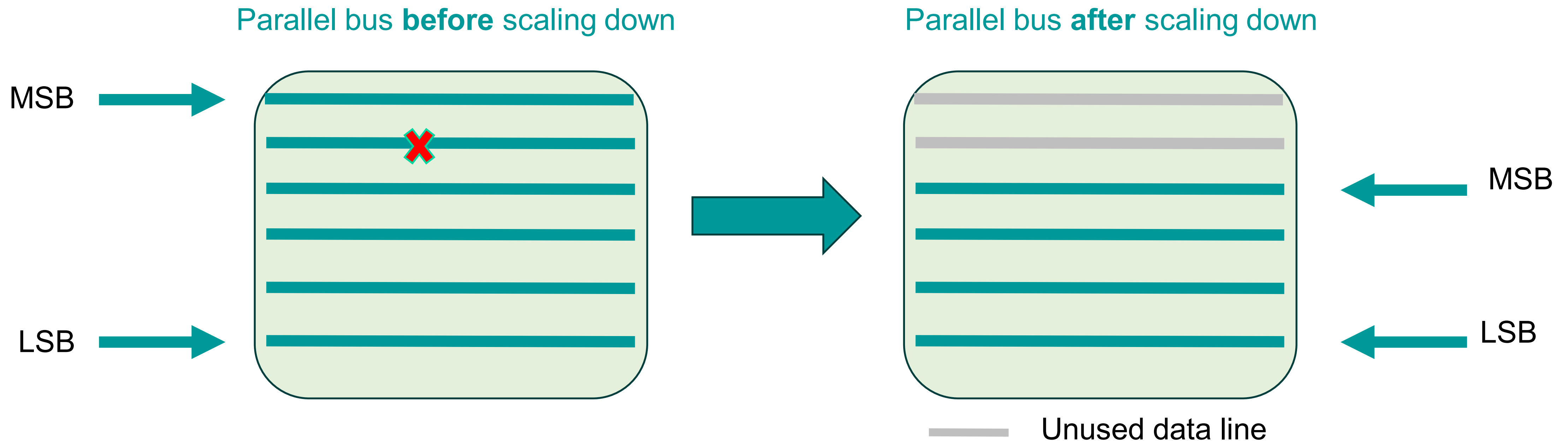

Fig.2 – Bus scaling example

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Efficient identical core testing

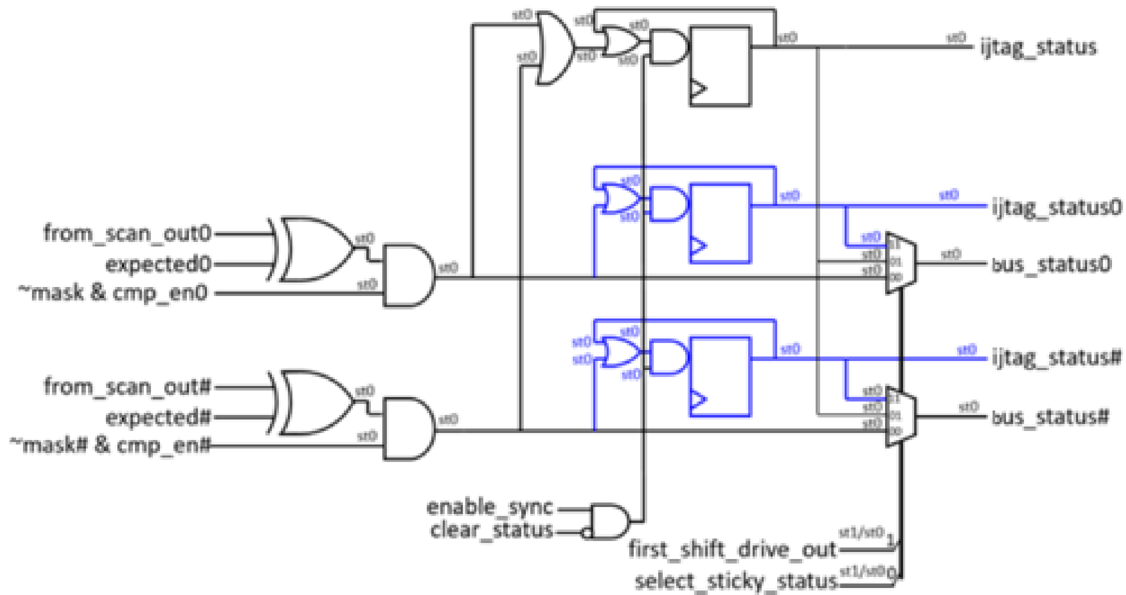

Fig.3 – On-Chip compare logic

Using On-Chip Compare

- ✓ Test any number of identical cores at constant cost
- ✓ Stored internally with on chip compare logic (*shown*)
- ✓ Output scan data collected immediately through transmission protocol
- ✓ Reuse the same efficient pattern for retargeting and on chip compare retest method
- ✓ Retest method to collect individual failing cores

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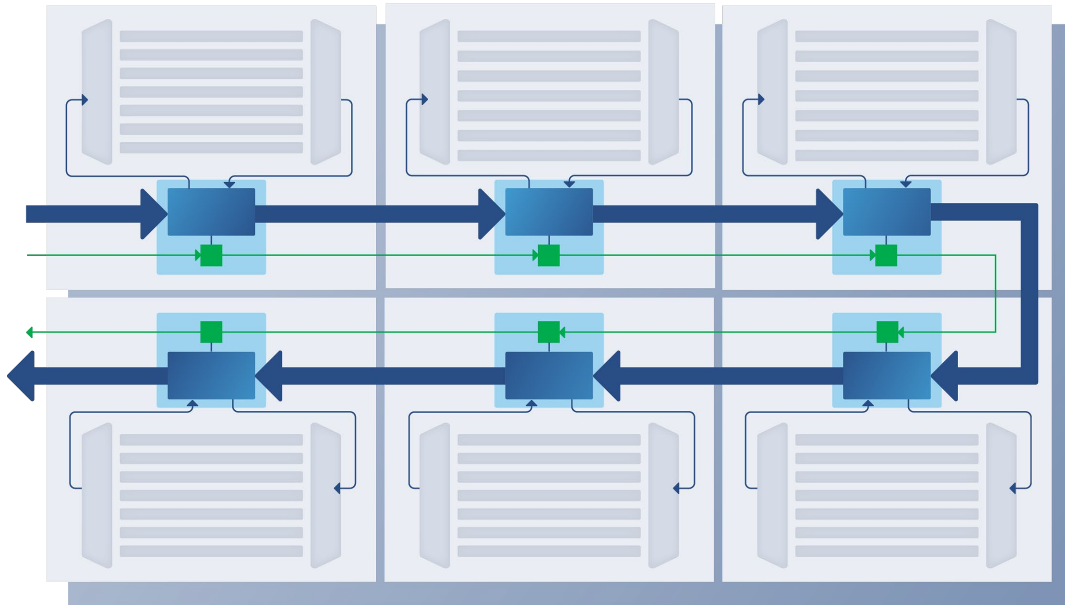
Adaptive to late design changes



- ✓ Plug-and-play architecture
- ✓ Addition of new core or changes to existing cores have no affect on chip-level DFT architecture
- ✓ Changes to the top-level design have no impact on chip-level DFT architecture
- ✓ Changes at core-level are fully encapsulated – have no change to top-level DFT
- ✓ No impact to the patterns of cores which are unchanged

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Adaptive DFT technology

Summary

Improve quality of testing through the flexibility of the DFT structures

Scalable solution to meet today and tomorrow quality standards :

- ✓ Determine cores to retarget at time of retargeting
- ✓ Change timing of scan pattern at time of retargeting
- ✓ Bus scaling
- ✓ Reuse same pattern through IJTAG interface
- ✓ Allows design and DFT changes late with no impact to the top-level DFT architecture
- ✓ Post silicon debug

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Thank you

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