ITC 2022 SIEMENS Booth Presentation
Analog Defect Coverage Improvement Using Tessent DefectSim

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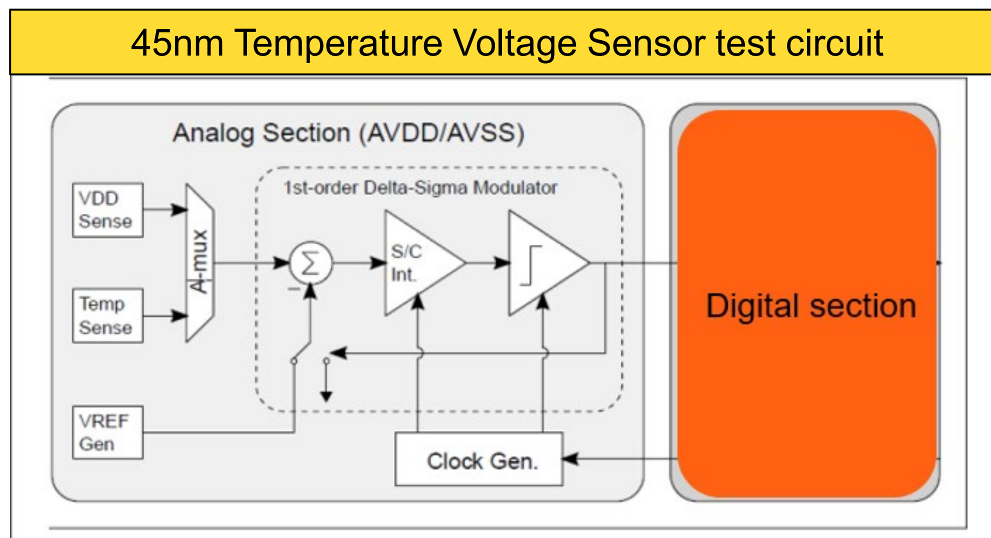
Background

- Goal - Evaluate defect coverage on an analog test circuit
  - Helping our analog IP designers to easily identify low coverage sub-blocks
  - Improve initial coverage if considered too low
- Circuit information
  - Temperature Voltage Sensor test circuit designed in differentiated 45nm GF technology
  - Focus only on the analog section for defect coverage analysis
  - Standard 3rd-party analog design environment
  - Functional testbench format - design measurements/expressions



Design size	
Component	**Instance count**
Resistor	53
Capacitor	29
Mosfets	1341
Total	**1423**

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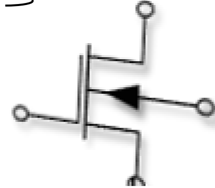
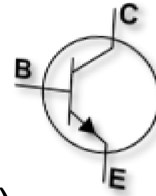
Defect Modeling – IEEE P2427 (HARD)

Up to 11 per MOS transistor:

- Short between drain & gate
- Short between gate & source
- Short between drain & source
- Open gate
  - Resistive open
  - Complete open
- Open drain or source (one model, double weight)
  - In the transistor (or M parallel transistors)
  - In 1 out of up to N transistors in parallel.
    e.g., if N ≥ 5, open causes ≤ 20% variation
- Short between bulk & drain
- Short between bulk & gate
- Short between bulk & source
- Open bulk

No short injected when terminals are connected to same node in design





Supports defect models involving bulk or substrate node

Up to 12 per bipolar transistor:

- Short between collector & base
- Short between base & emitter
- Short between collector & emitter
- Open base
- Open collector
  - In the transistor (or M parallel transistors)
  - In 1 out of up to N transistors in parallel.
    e.g., if N ≥ 5, open causes ≤ 20% variation
- Open emitter
  - In the transistor (or M parallel transistors)
  - In 1 out of up to N transistors in parallel.
    e.g., if N ≥ 5, open causes ≤ 20% variation
- Short between substrate & collector
- Short between substrate & base
- Short between substrate & emitter
- Open substrate

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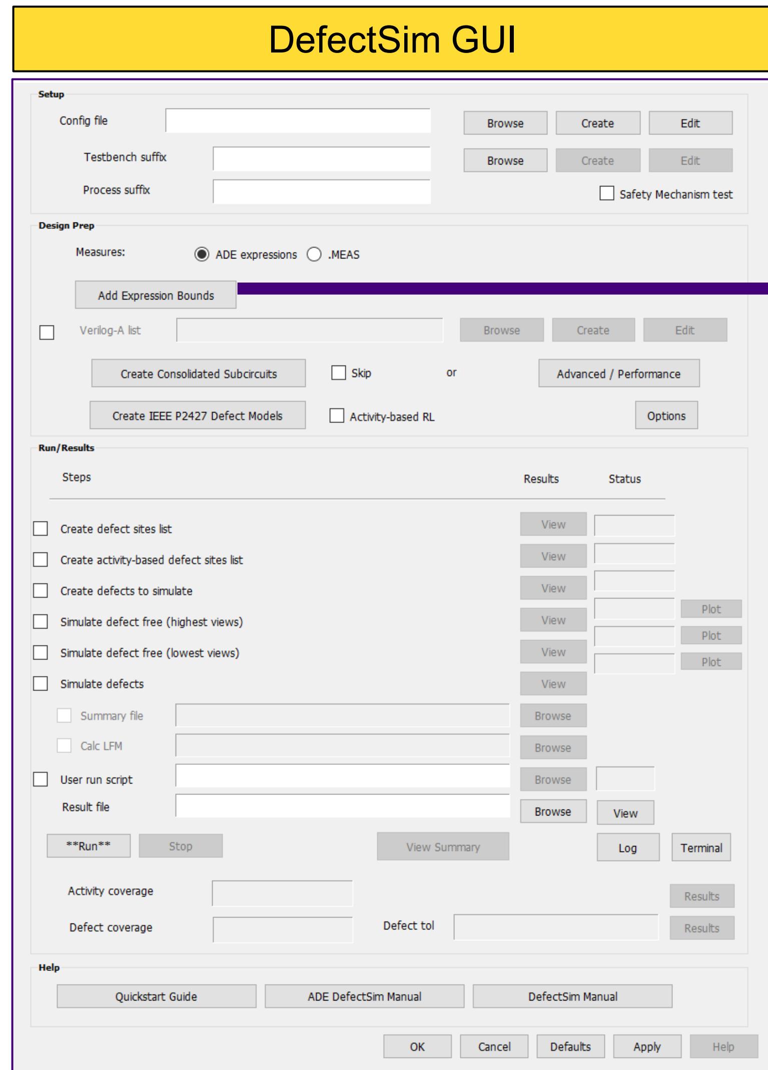
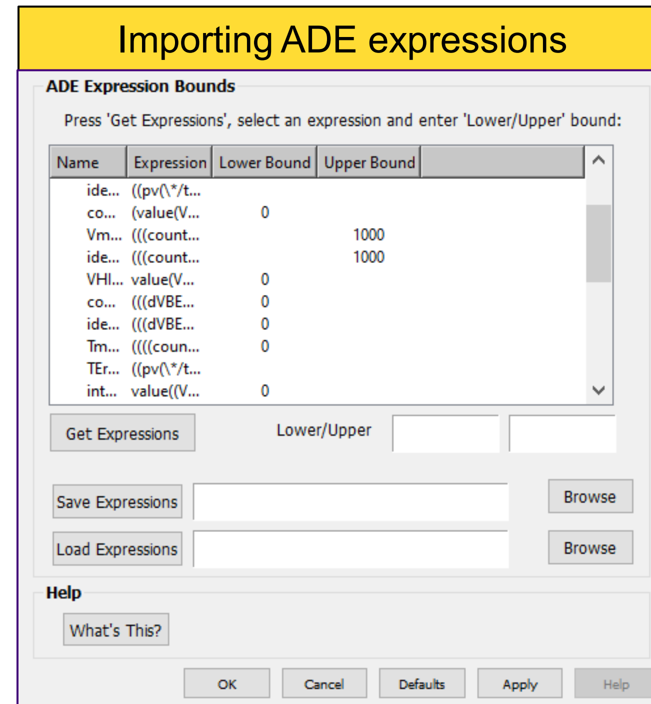
How – Using DefectSim GUI





- Imported testbench expressions to DefectSim GUI.
- Used IEEE P2427 (hard) defect models.
- Easy to setup and execute the entire flow

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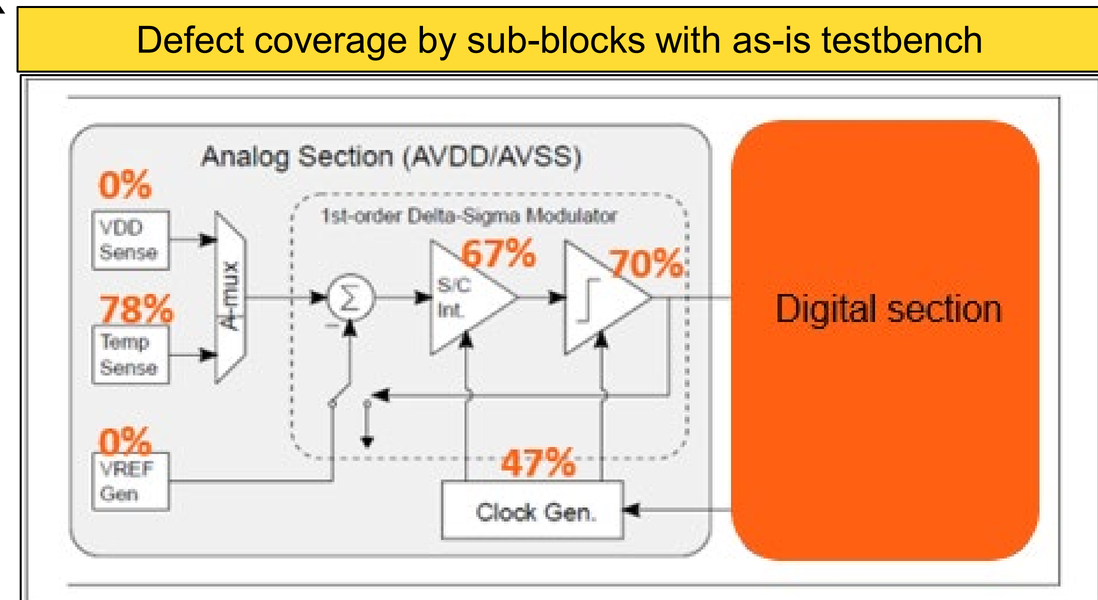
Defect coverage with as-is testbench

- 93% activity coverage (likelihood-weighted percentage of sites that are ACTIVE)
  - Activity coverage high enough to justify running defect-injected simulations
  - Standard sampling for defect size - 250 out of 13450 possible defects
- 56% overall defect coverage with as-is testbench
  - Low coverage sub-blocks identified by the tool
  - Designer chose to focus on VREF Gen block

Defect Statistics		
Component	**Instance count**	**Defects Count**
Resistor	53	4
Capacitor	32	64
Mosfets	1341	13382
Total	**1426**	**13450**

Defect coverage by sub-blocks with as-is testbench



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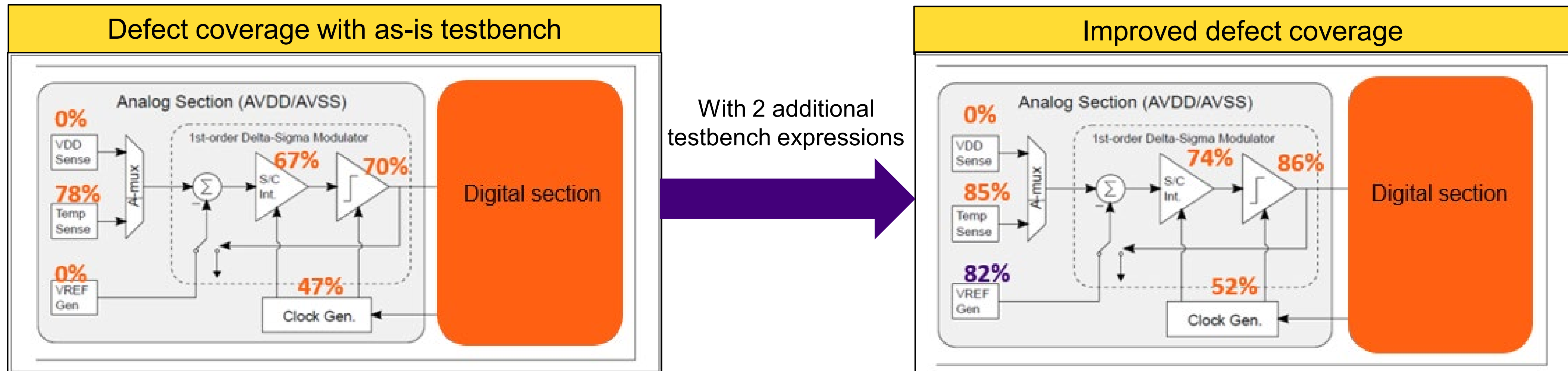
Coverage improvements

- Additional 2 testbench expressions created
  - Increased coverage from 0 to 82% on targeted VREF Gen block.
  - 9% increase in overall defect coverage



- Simulated all testbenches and extended to FF corner
  - 42% of undetected defects at TT detected at the FF corner
  - Combined the defect coverage across both process corners
  - 14% increase in overall defect coverage.

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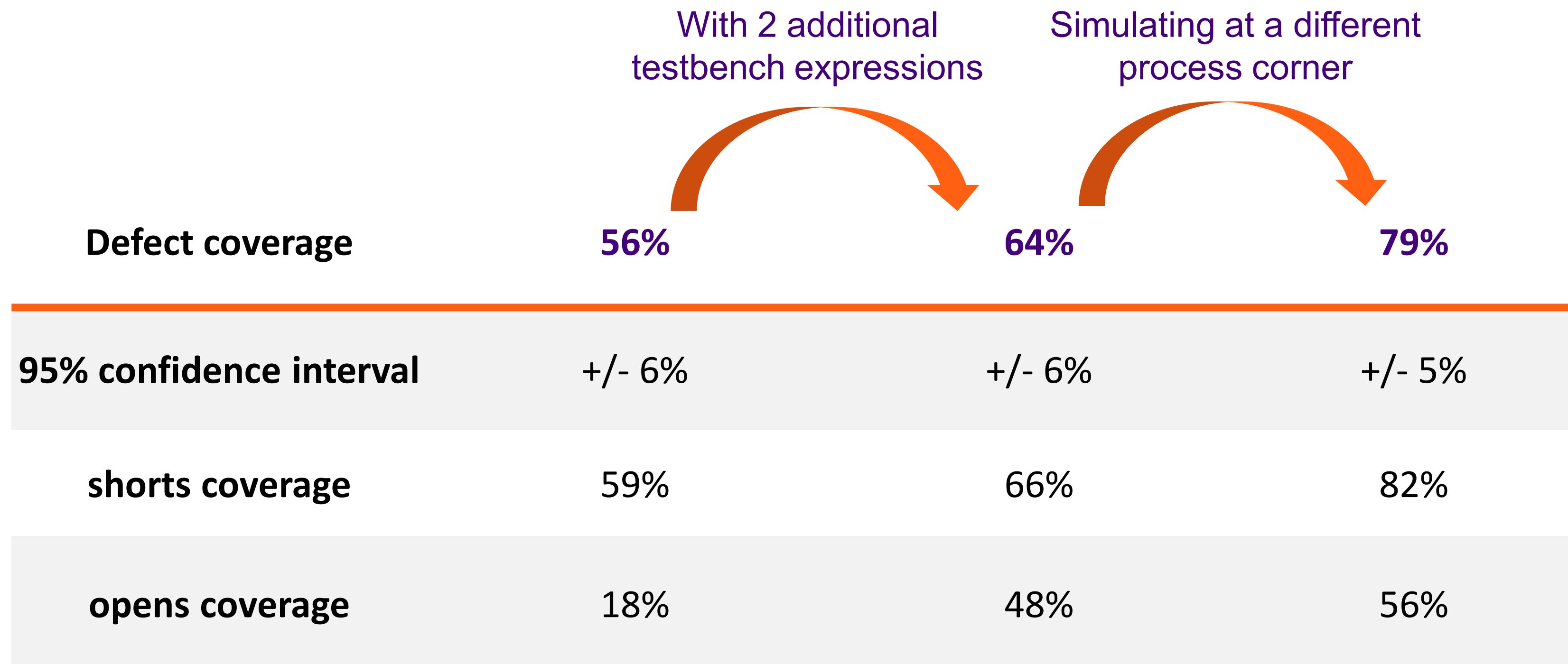
Summary

- 56% analog defect coverage with as-is designer testbench
- 23% coverage improvement achieved
  - 9% increase by targeting a low coverage sub-block.
  - 14% increase by simulating at a different process corner



Defect coverage	56%	64%	79%
95% confidence interval	+/- 6%	+/- 6%	+/- 5%
shorts coverage	59%	66%	82%
opens coverage	18%	48%	56%

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