Veloce SoC
Tessent SSN Benefits

Tiled Designs architecture

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Agenda

Veloce Overview

Veloce DFT App

Veloce SoC & DFT Challenges

Tessent SSN Benefits

Veloce overview

The Veloce hardware-assisted verification system is the first complete, integrated offering that combines best-in-class virtual platform, hardware emulation, and FPGA prototyping technologies and paves the way to leverage the latest powerful hardware-assisted verification methodologies.

Directly impacts on these use models

- Virtual environments
- Time to visibility and debug
- Simulation acceleration and coverage closure
- Monitors/trackers for data collection
- Power trend analysis and measurements
- Data analytics

Veloce Apps

Take verification to the next level with Veloce Apps

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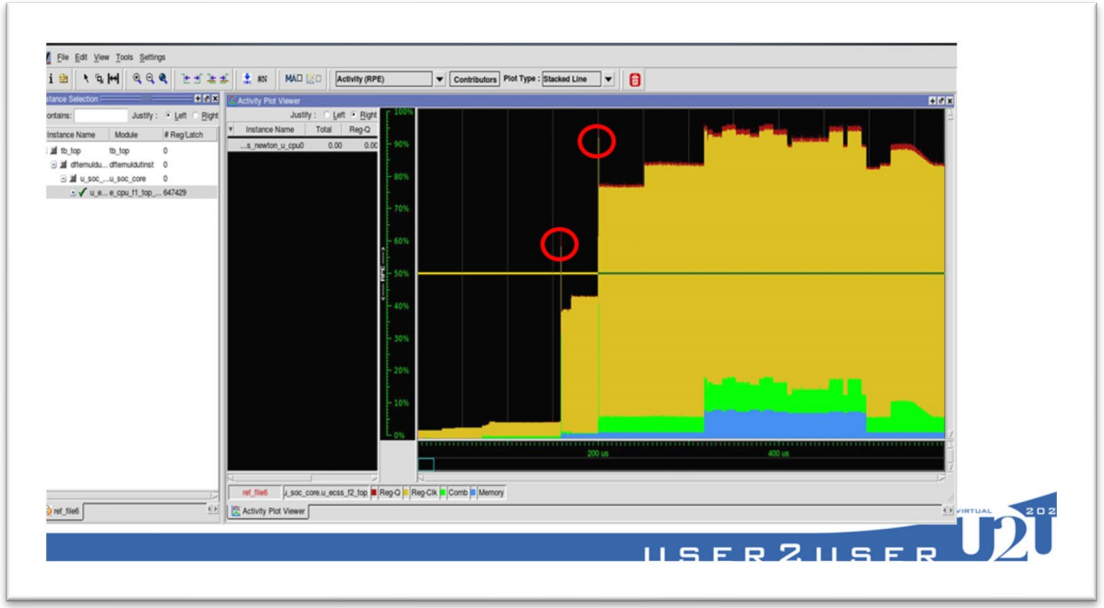
Veloce DFT App

Industry insights

- Time to Market: Long simulation time leads to incomplete pattern validation
- High Test Costs: Long ATE test times leads to high costs, consuming up to 40% of total design costs
- Time To Quality: Customer test escapes due to low fault coverage and power events



Value of the App

- Ease of use, ease of bring up (STIL + Design – fully automated)
- Efficiently handle full SoC, big designs
- Handle gate level netlist
- Several order of magnitude acceleration vs simulation

Veloce DFT App to accelerate DFT goals

Design	DFT Methodology	Design Size	# Cycles	Sim Runtime	Veloce Runtime	Improvement
GL Sensor	ATPG	2	2M	3.1 days	90s	3000X
RTL WideIO	MBIST	1	8B	83.3 days	120m	1000x
GL GPP	ATPG	1	90K	12 hrs	5s	10000x
GL GPU	ATPG	1	780K	2.7 days	58s	4000x
GL SoC	MBIST	6	183K	26 hrs	6s	16000x

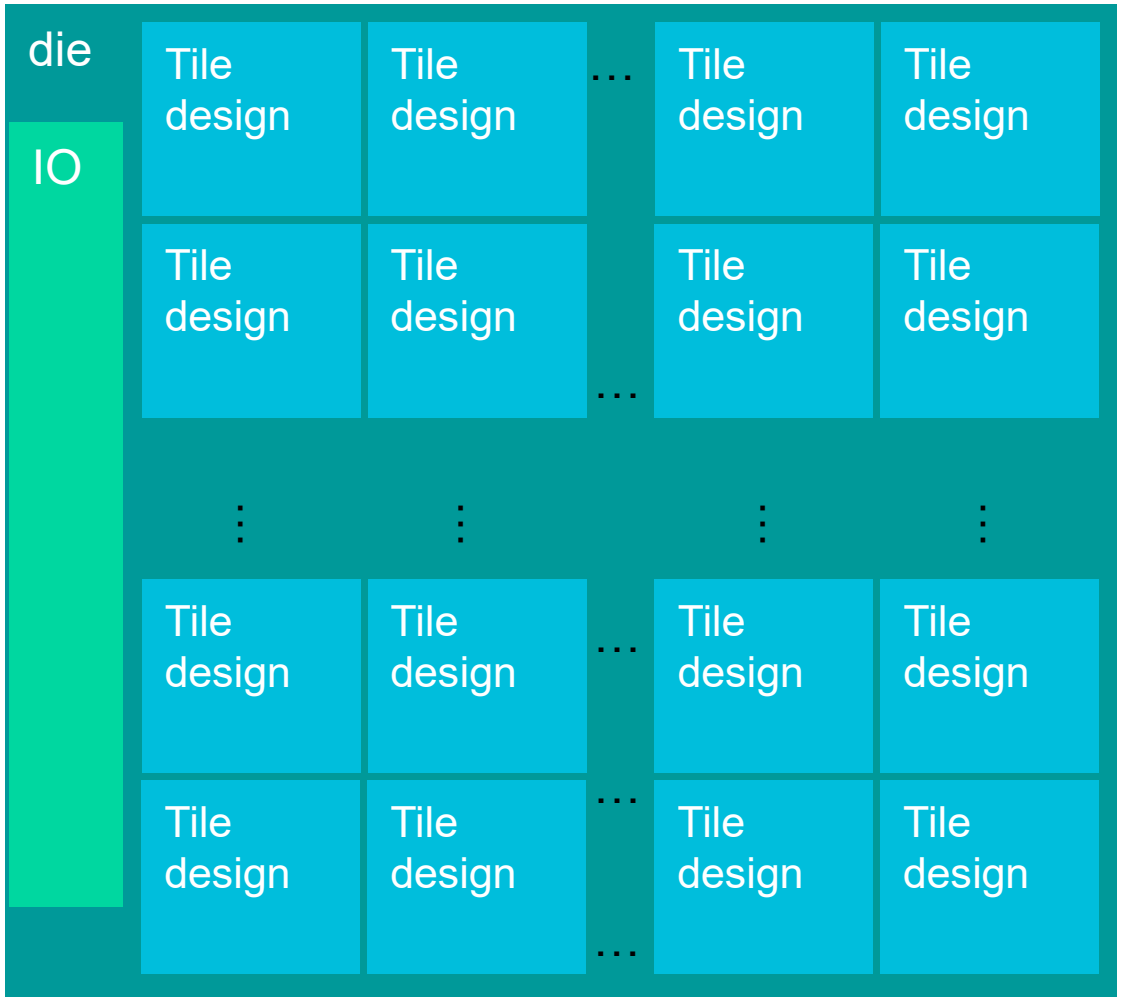
Achieve speed-up from days to seconds

Veloce SoC

DFT Challenges

Veloce SoC & DFT Challenges

- **Multi-die SoC with multi billions gates**
- **Multi hierarchical level and identical cores**
- **High speed IP management**
- **High memory capacity**
- **Implementation of different DFT features (IJTAG, MBIST, LBIST, Scan Compress …)**
- **Tiled designs with challenging place & route**
- **Very High test data volume**
- **Complex clock tree with thousands PLLs**
- **Complex timing closure and difficult to route DFT signals to IO Pads**



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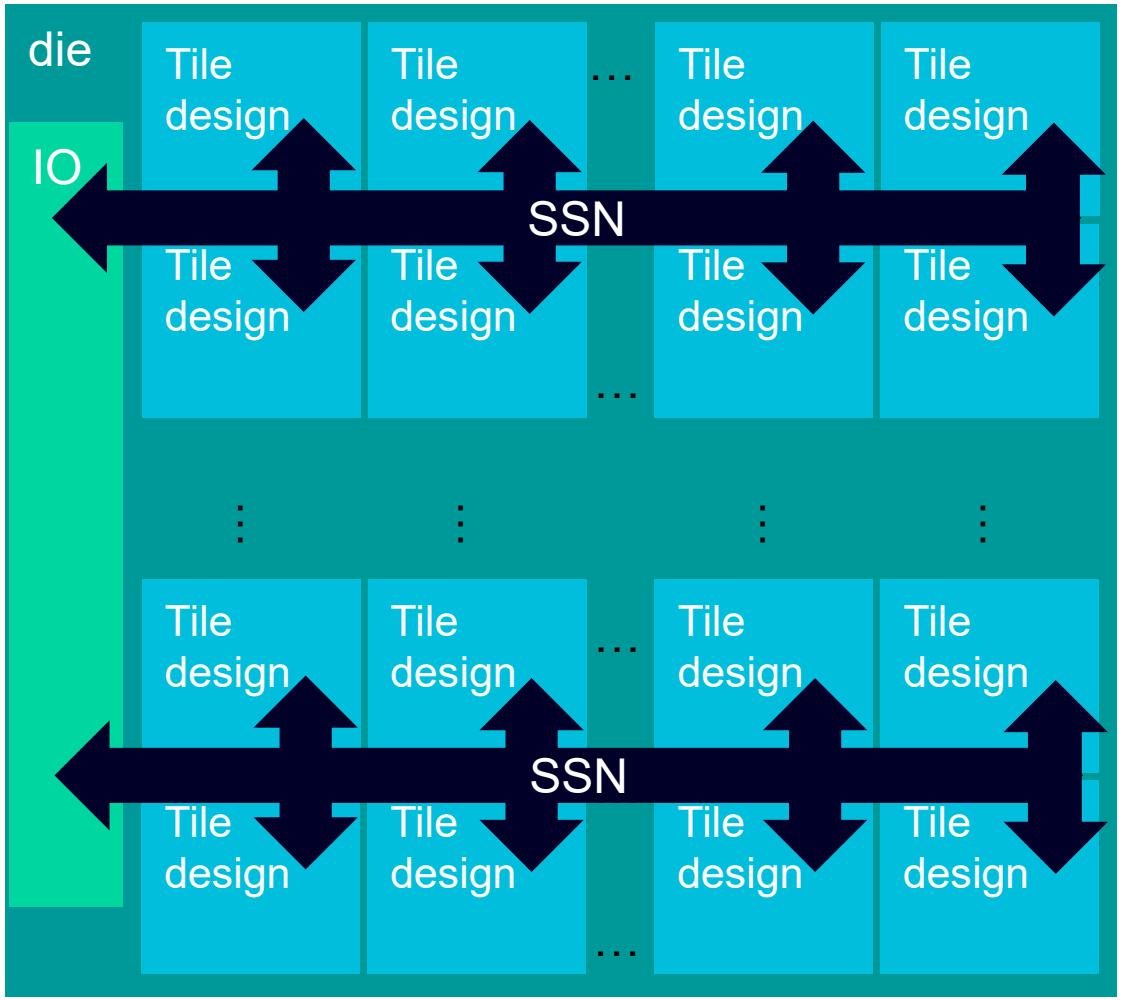
Tessent SSN Benefits

- **Full SSN & IJTAG configurable Network**
- **Uniform bus travels the chip in a plug & play matter**
- **No need to directly route DFT signals from every tile block to IO pads**
- **Inter-tile timing paths naturally tested using functional timing**
- **SSN clocking implemented to follow functional clock path**
- **Optimized test data volume**



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