ITC 2024 PO 35: Driving deterministic In-System Test using Advanced Peripheral Bus (APB)

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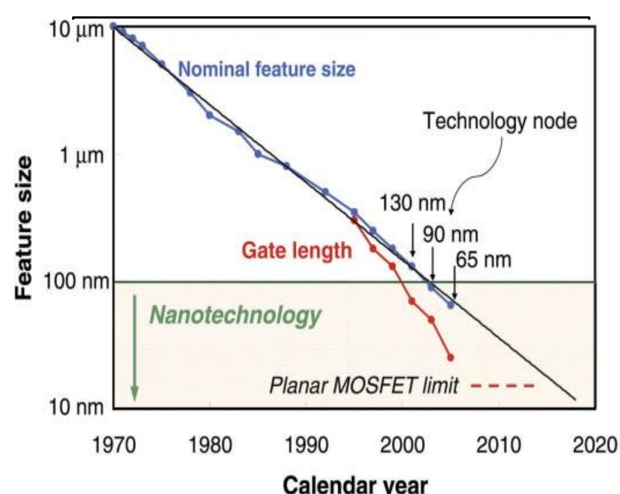
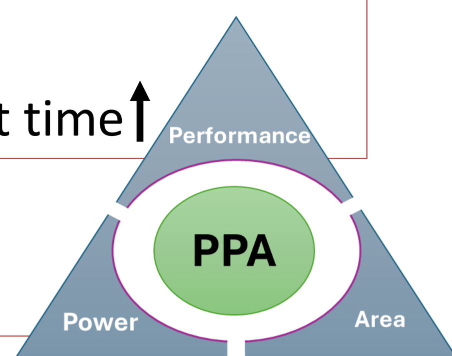
(1) Challenges to Running In-System Test (IST) on Automotive Designs



- Semiconductor Technology Nodes ↓
- Design Complexity ↑
- Pin Limited Design, test time ↑



- Automotive designs (ISO 26262) have aggressive test quality and test time requirements
- IST techniques are required to achieve high test coverage

(2) Pseudo-random patterns v/s Deterministic patterns for IST

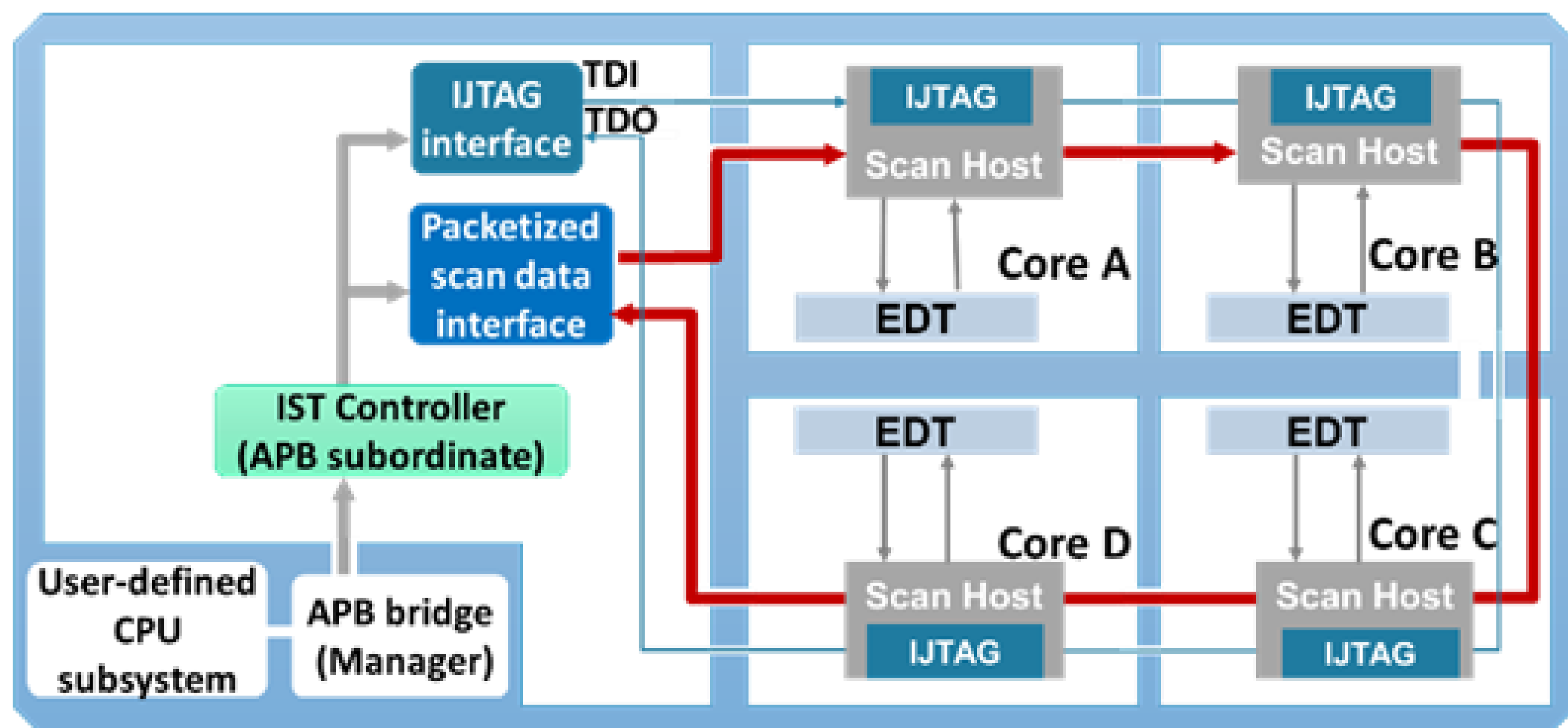
Pseudo Random Patterns (Logic BIST)

- Miss subtle defects
- Employ test points to enhance test coverage
- Requires X masking – worsening impact on PPA

Deterministic Patterns

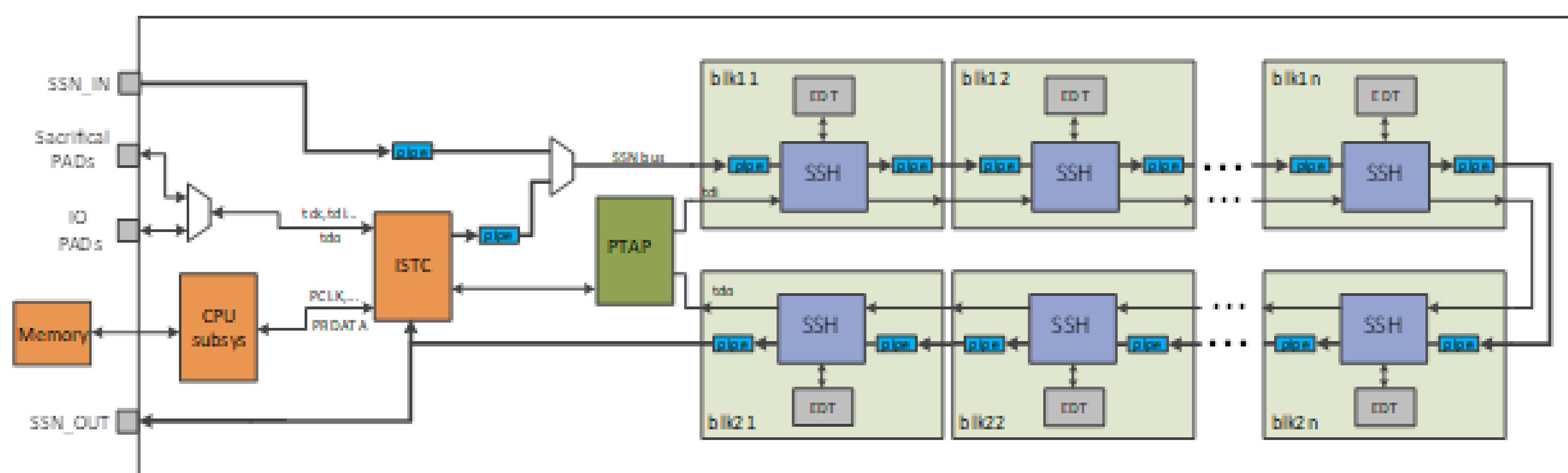
- High quality test set targeting subtle defects
- Meet high test quality and test time requirements for safety critical applications (ASIL D)

(3) Applying deterministic IST patterns with Advanced Peripheral Bus (APB)



- IST controller operates APB subordinate conforming to the ARM ® AMBA APB protocol
- Packetized data for delivering deterministic (scan) data on parallel SSN bus
- Configuration data via IJTAG (IEEE 1687) network

(4) Integrating with CPU Subsystem and PTAP

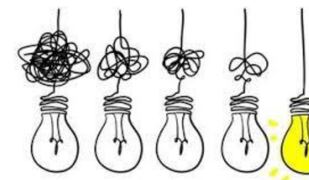


- 2 test modes
  - GPIOs : ATE driven, for manufacturing test
  - On-chip CPU for IST
- CPU fetches test data from external memory and delivers to the ISTC

(5) Merits of deterministic IST

- Reduces test time when compared to logic BIST

- Ability to update test content in-field based on learned defectivity rates



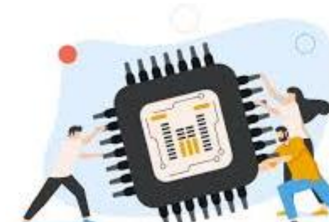
- Reduced area overhead
- Simplified DFT implementation (no X masking or testpoints required)

(6) Conclusion

- Better test coverage & shorter test application time achieved with deterministic IST
- Easier to meet test requirements for safety critical applications at lower cost

Comprehensive testing for higher test quality

Integration to system software makes pattern validation more robust and reliable



Smaller area overhead, improved flow and better test quality compared to LBIST