Grzegorz Mrugalski • Janusz Rajski • Jerzy Tyszer • Bartosz Włodarczak

X-DIST

Deterministic In-System Test with X-masking

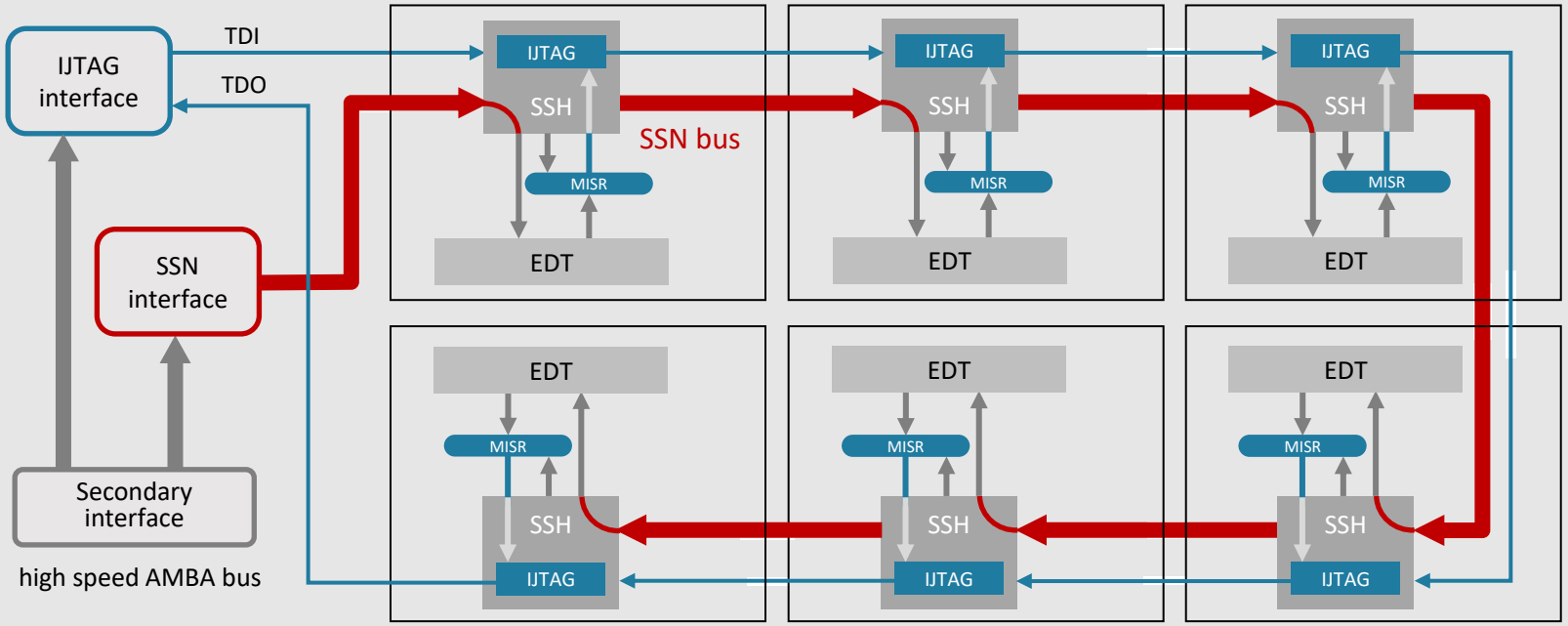
SIEMENS

Why deterministic in-system test?

Deterministic in-system tests expected to gain adoption over the coming years

Requirements	Logic BIST	DIST
Test quality: high test coverage, advanced fault models including defect-aware test	✓	✓✓✓
Test time: ability to achieve target test coverage within a small test window	✓✓	✓✓✓
Test content update: ability to change the test content	✓	✓✓✓
Implementation flow: difficulty in implementing DFT	✓	✓✓
Test storage: memory needed to store test data on-chip or in-system	✓✓✓	✓

SSN-based DIST setup



Motivation

- Unknown states can render test useless
- X-tolerant compactors need to resort to scan chain masking
- Challenges of in-field and in-system test
  - wide range of static and dynamic X state profiles
  - thousands of scan chains to be masked selectively

Purpose

- X-tolerant programmable compactor fed by EDT logic
- Generic scan selection logic to mask, in a fine-grained manner, X states within tunable groups of scan chains
- Help to tolerate Xs missed during design and DFT insertion
- Find the best control settings to reduce test data

Outline

- X-masking so far
- Overall architecture
- Main building blocks
- Selection of controls
- Experimental results
- Conclusions

State-of-the-art solutions

ITC 2001 — OPMISR — Barnhart, Brunkhorst; Distler, Farnsworth, Keller, Koenemann, Ferko

ITC 2003 — Using LFSR reseeding — Naruse, Pomeranz, Reddy, Kundu

TCAD 2004 — X-Compact — Mitra, Kim

ITC 2005 — X-Filter — Sharma, Cheng

ITC 2007 — X-Canceling MISR — Touba

TCAD 2008 — X-Press — Cheng; Kassab, Mrugalski, Mukherjee, Rajski, Tyszer

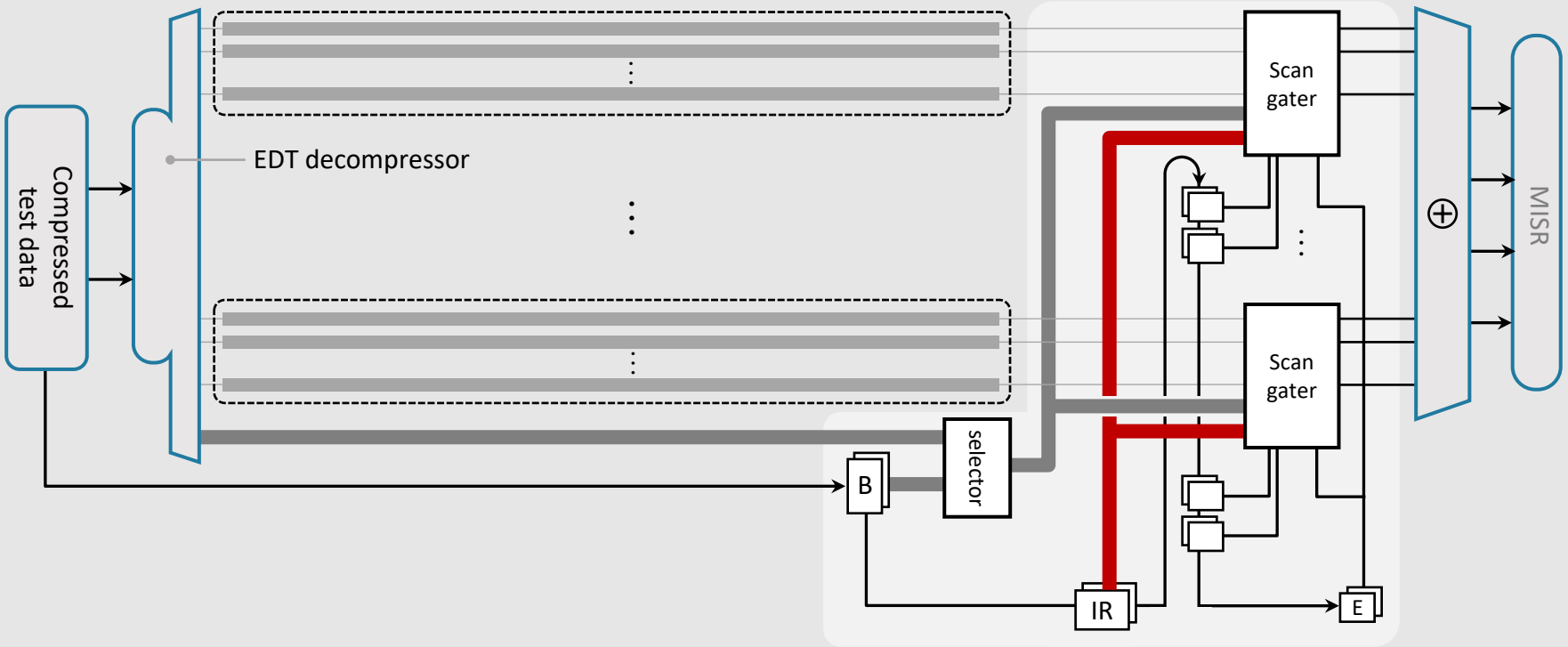
ToC 2008 — X-Block — Wang, Balakrishnan, Wei

ITC 2018 — X-LBIST — Wohl, Colburn, Waicukauski, Maston

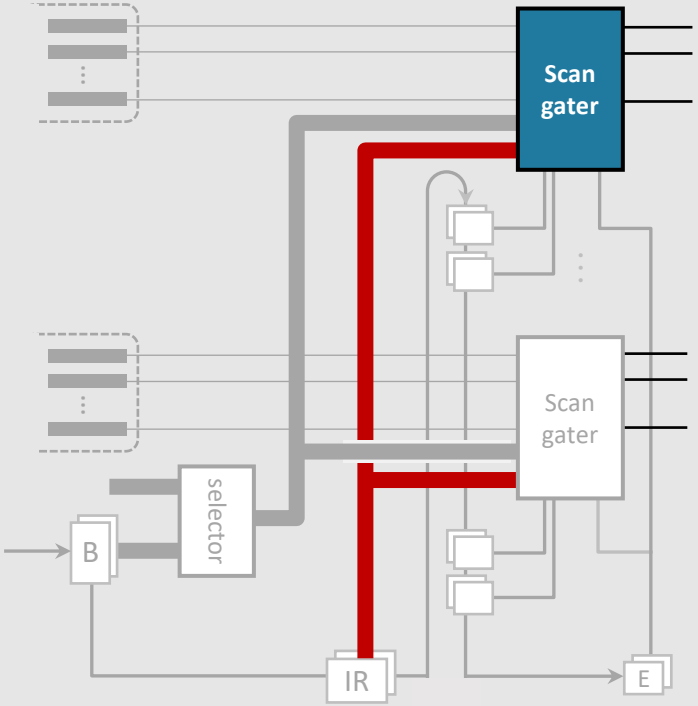
ITC 2019 — Hybrid compactor — Maaz, Sprenger, Hellebrand

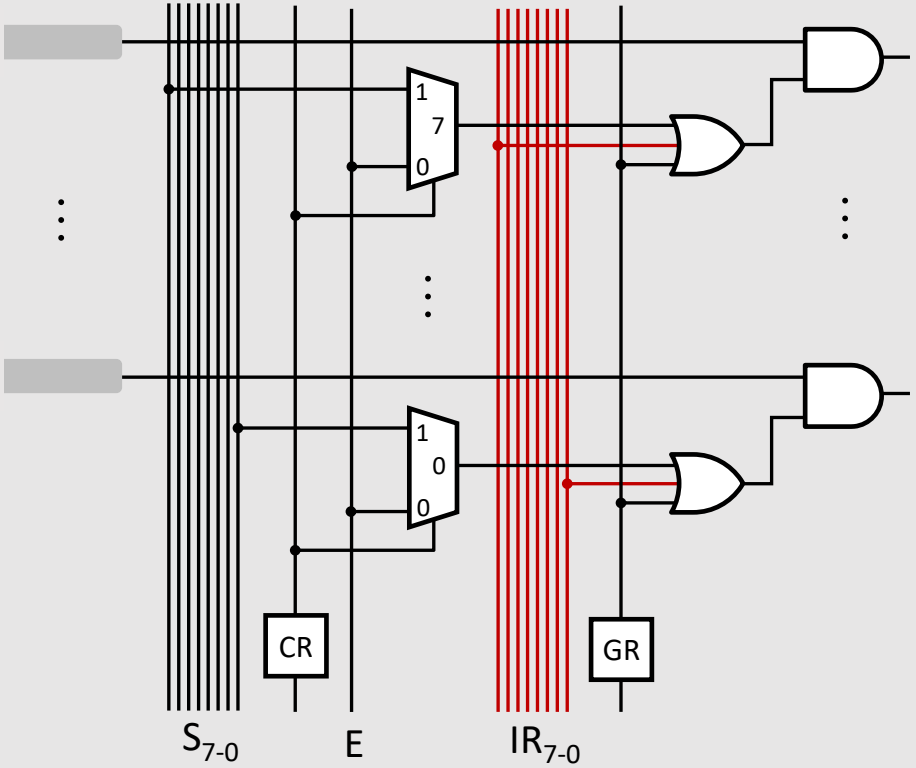
ITC 2020 — maXpress — Liu, Milewski, Mukherjee; Mrugalski, Rajski, Tyszer, Włodarczak

8 Overall architecture

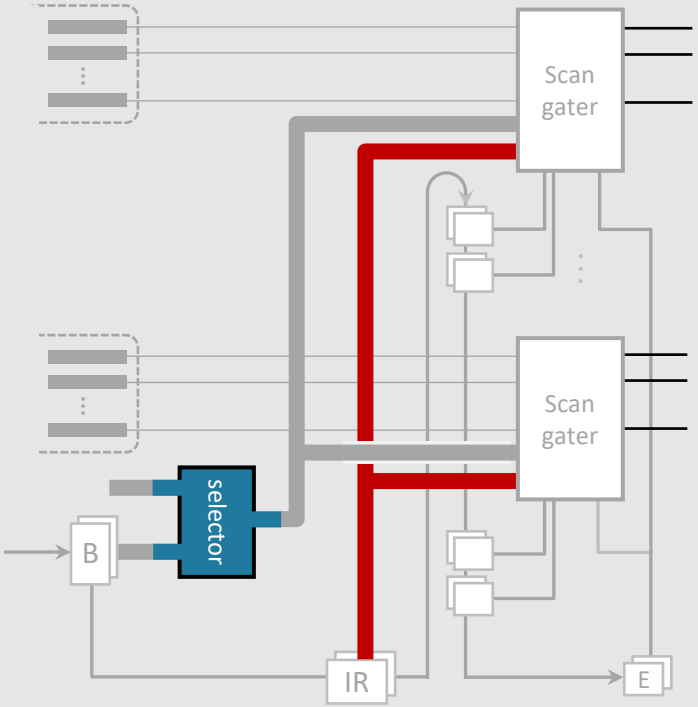


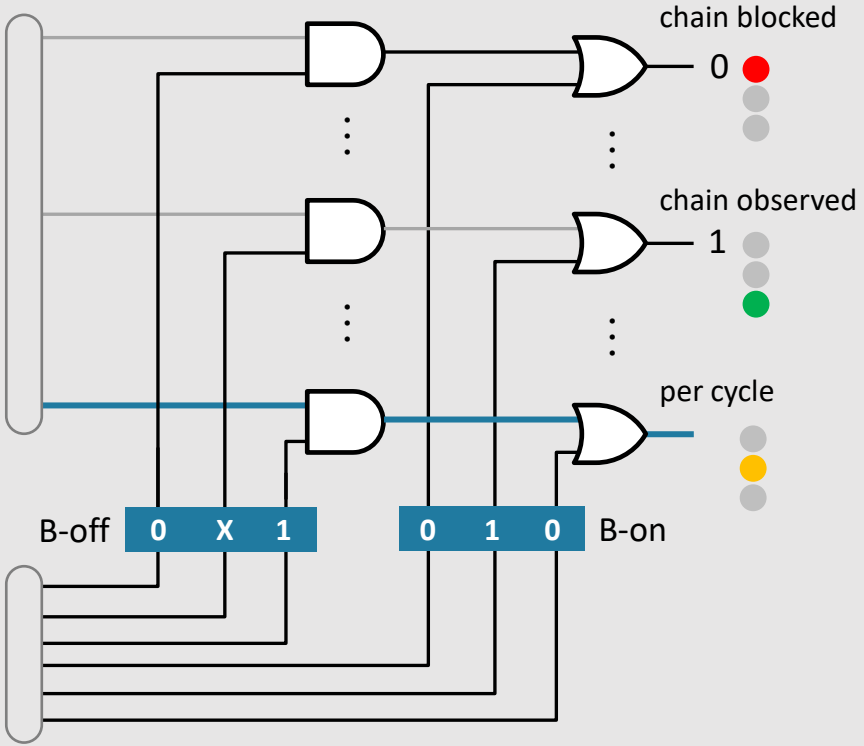
Scan gater


Scan gater
Scan gater
selector
B
IR
E

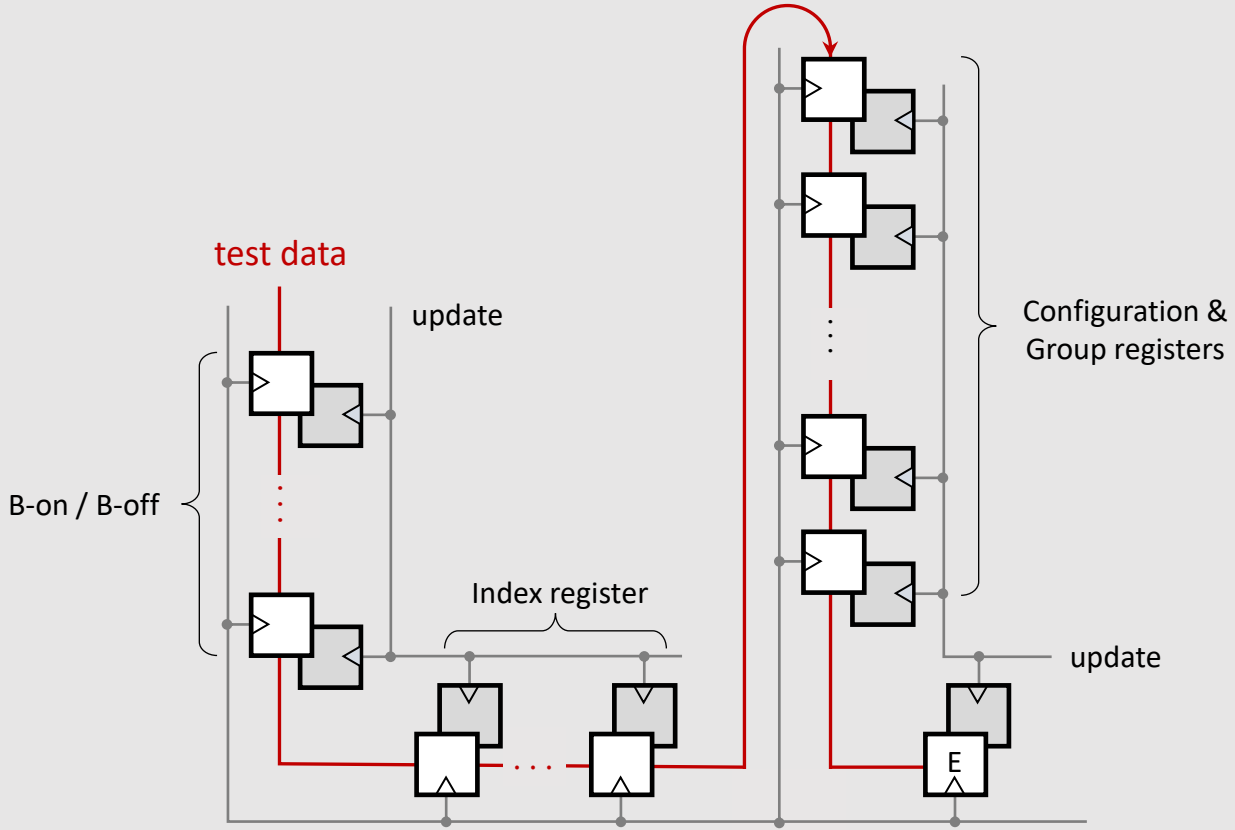

1
7
0
1
0
0
CR
GR
$S_{7\text{-}0}$
E
$IR_{7\text{-}0}$

Selector


Scan gater
Scan gater
selector
B
IR
E

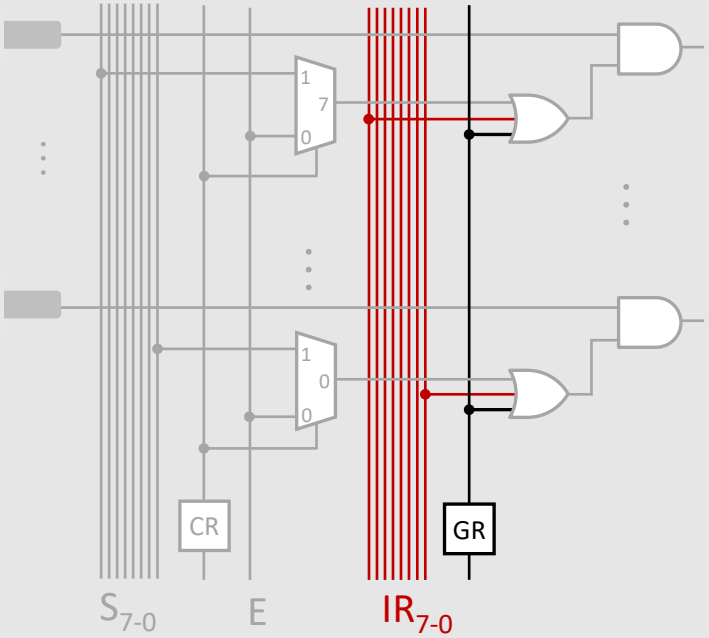

chain blocked
0
chain observed
1
per cycle
B-off
0 X 1
0 1 0
B-on

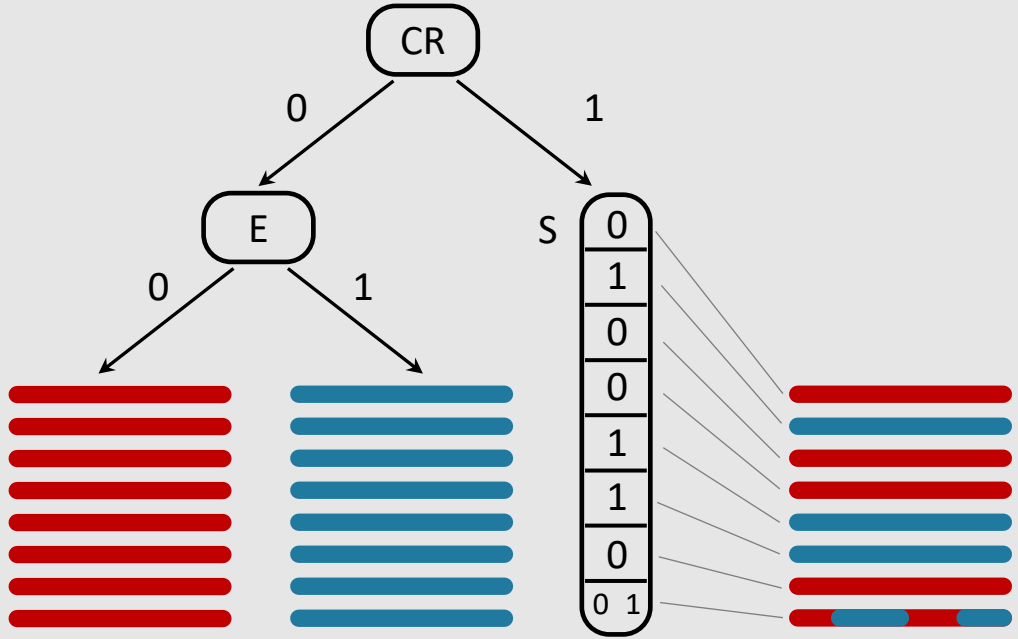
Control registers



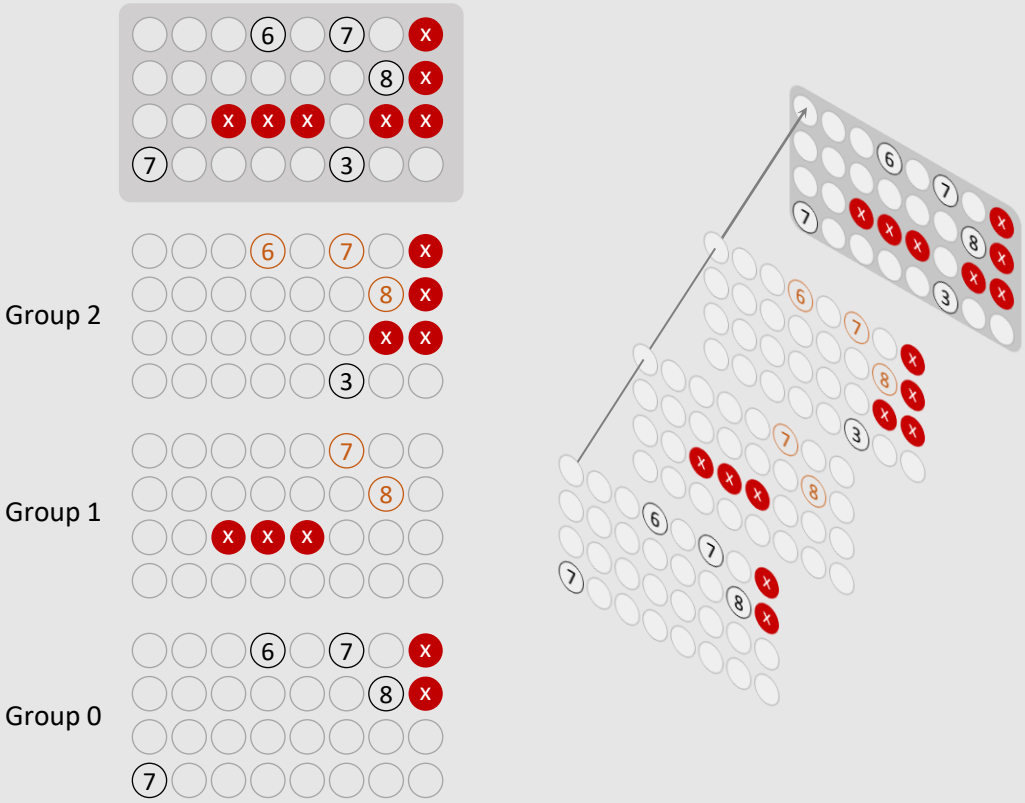
Setting controls

GR and IR determined up front to handle X-free scan chains





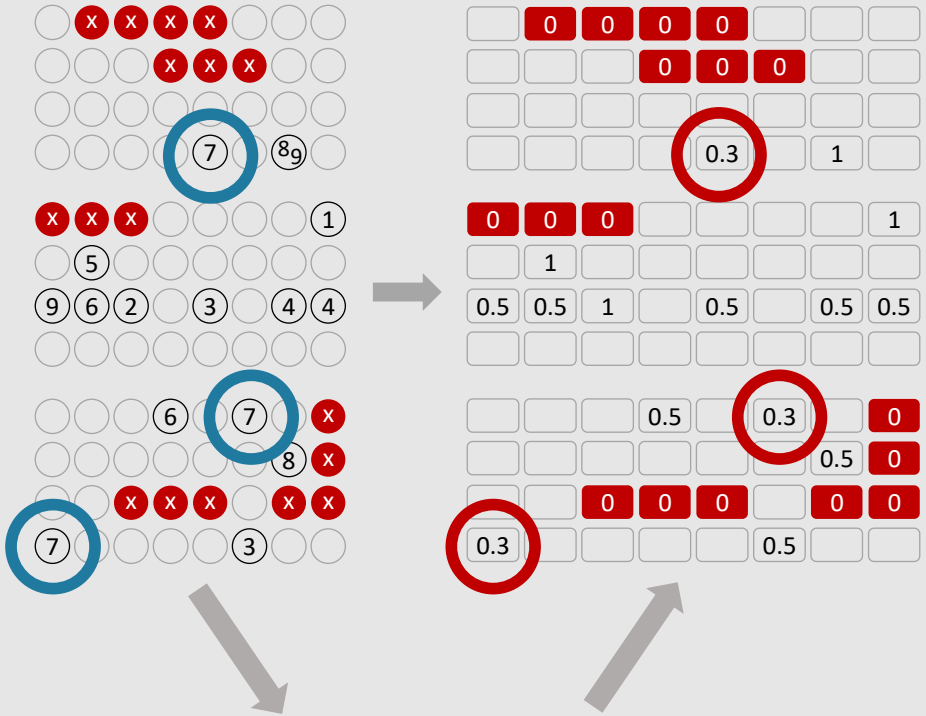
Superposition of groups



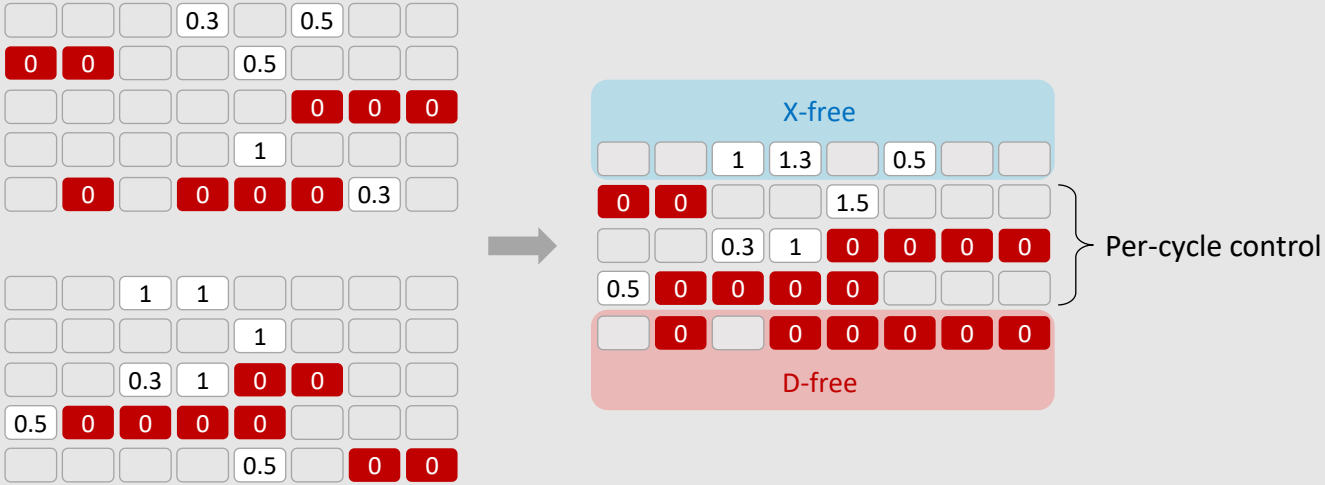
- X superimposed on the same cell in other groups; may cause a collateral damage
- A fault propagating to the same cell in different groups counted once
- If a fault propagates to different cells, all of them are counted

Cell weights

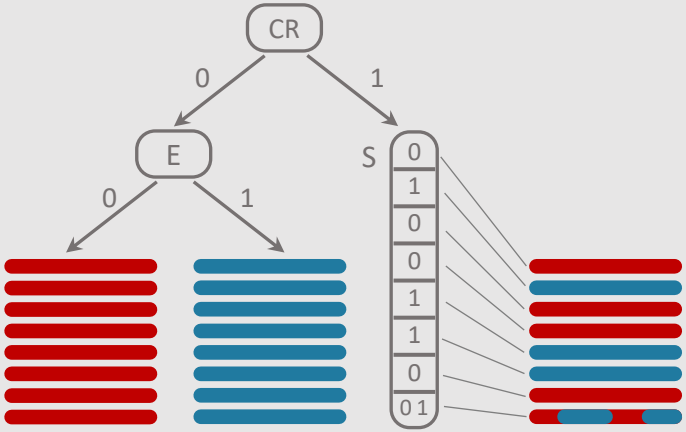
- A cell represented by weights of faults it observes
- A fault weight – inverse of the number of its observation sites
- X-cells have zero weight

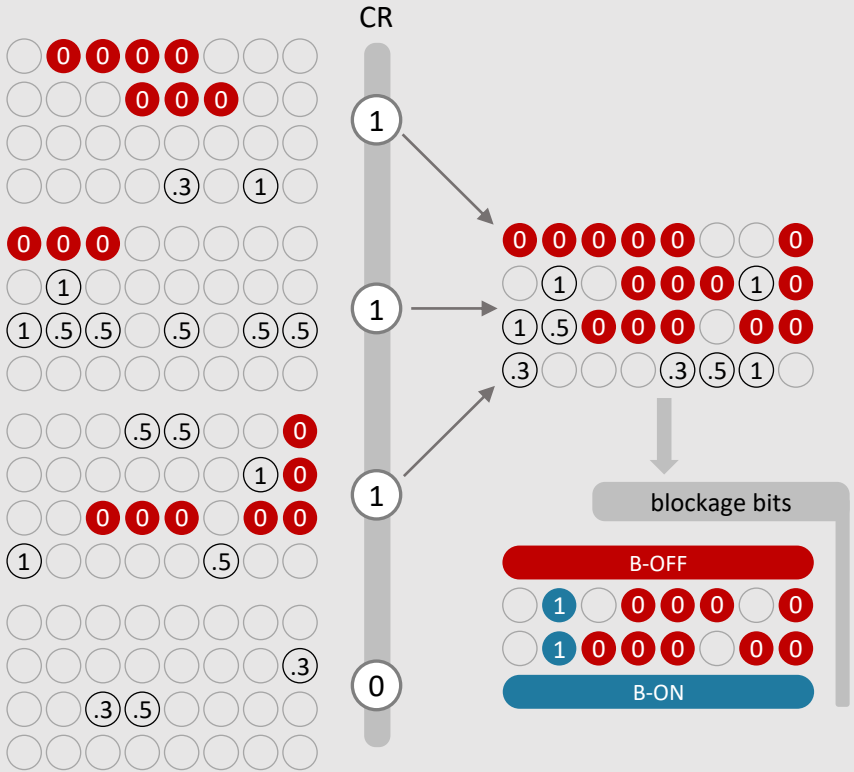


Superposition of weights

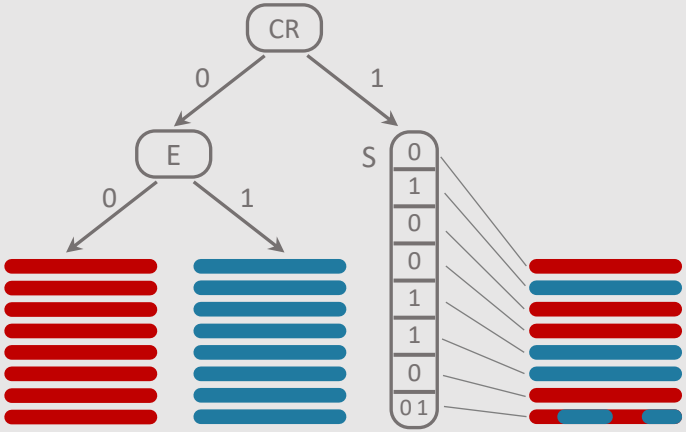


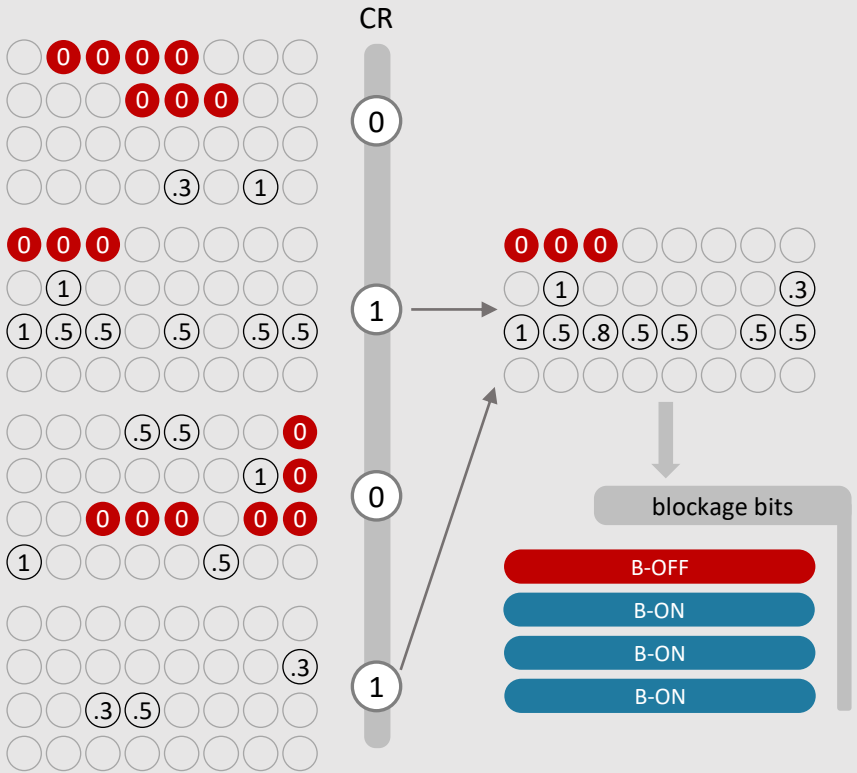
Setting configuration register (E = 1)





Setting configuration register (E = 0)



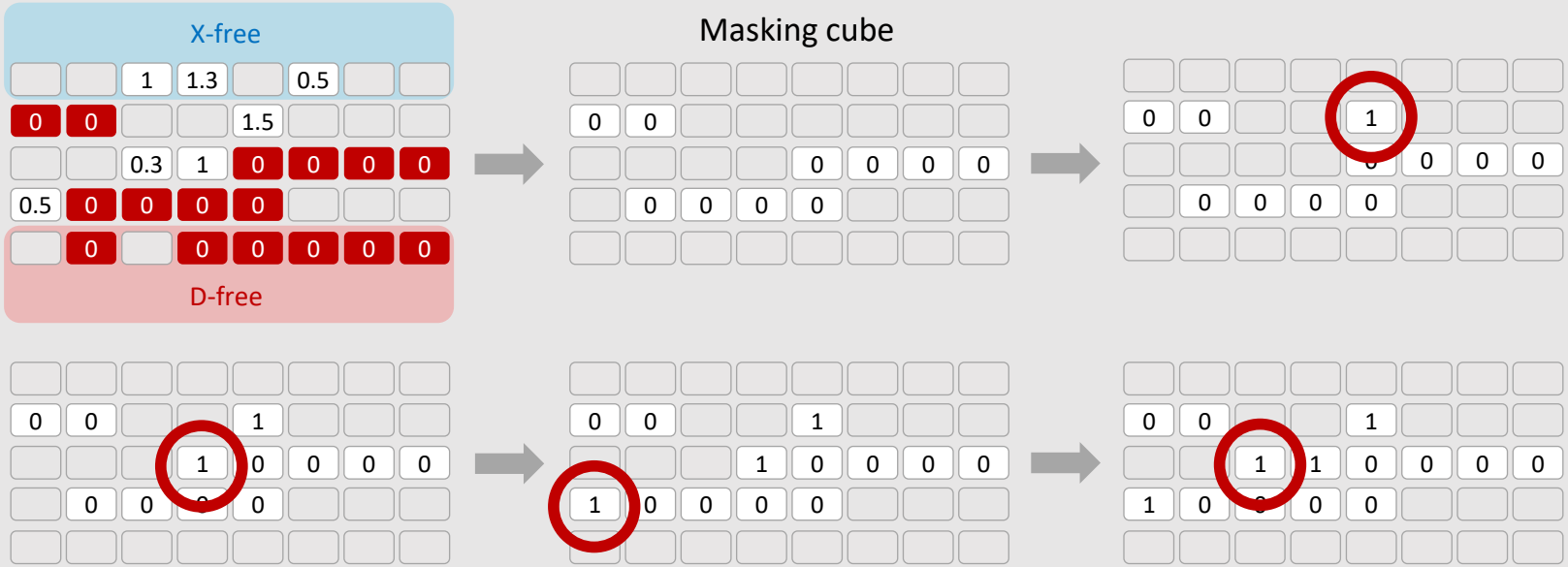


Need to examine 2^g CR setups
g – the number of scan gaters

Hill-climbing to select the best CR setup

Encoding of masking cubes

Masking values provided in a per-cycle mode need to be EDT-encoded
Encoding pattern p precedes encoding masking cube for pattern p – 1
X- masking requires a tiny fraction of all EDT variables



Test cases

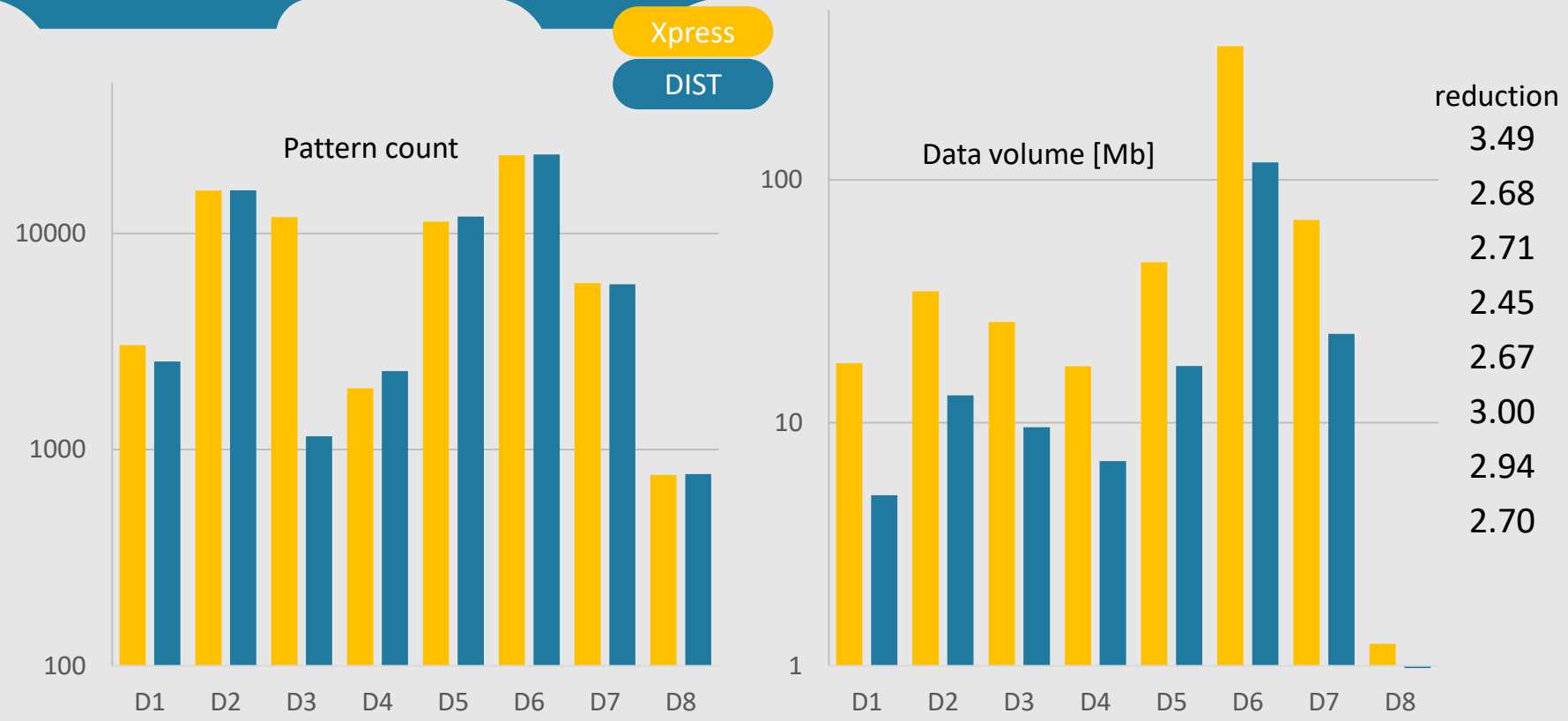
	Gates M	Scan cells K	Scan	Stuck-at faults	X-cells	X-chains	EDT inputs / size	Test coverage w/Xs %
D1	1.02	36.5	1,200 × 65	2,721,968	2,213	56	8 / 32	97.89
D2	2.47	149.4	1,200 × 66	5,933,388	837	36	2 / 46	99.71
D3	2.43	185	528 × 169	6,354,467	223	16	2 / 60	99.84
D4	1.21	72.3	729 × 175	3,812,564	7,185	148	16 / 64	96.40
D5	2.09	145.1	817 × 242	5,610,954	6,906	101	4 / 46	98.54
D6	1.18	97.8	1,236 × 242	4,251,354	472	22	2 / 37	97.65
D7	7.86	428.7	900 × 237	8,357,022	1,981	10	8 / 32	92.65
D8	0.22	12.6	3,163 × 291	188,486	375	9	4 / 32	98.97

Xpress

Experimental results

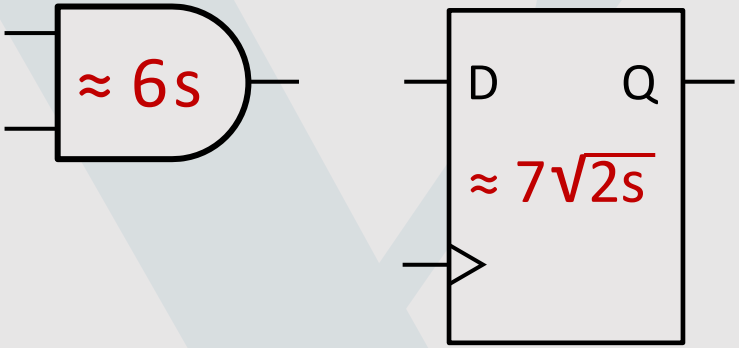
	Static control data [Mb]	Dynamic control data per pattern [% of EDT seed variables]			E0 [%]	Test coverage [%]	Test coverage Xpress
		min	max	average			
D1	0.1755	0.64	12	8.04	4.03	97.89	97.89
D2	1.6885	0.26	15	0.53	3.80	99.71	99.71
D3	1.4282	0.26	15	0.20	0.26	99.84	99.84
D4	0.2813	0.06	5	4.79	32.22	96.40	96.40
D5	1.3244	0.14	20	5.63	13.75	98.54	98.54
D6	2.4746	0.29	15	0.50	1.36	97.65	97.65
D7	0.9331	5.00	5	3.75	4.72	92.65	92.65
D8	0.0499	0.17	10	2.50	2.40	98.97	98.97

Experimental results



Group size: $\sqrt{2s}$

Silicon real-estate



s – the number of scan chains

- Design D5
  - 2.09M gates
  - 420 scan chains, each of 346 flip-flops
  - 29 groups, each of 15 chains
  - extra area: 208 flip-flops, 2,469 gates, 0.18% overhead

Conclusion

- X-tolerant compactor for deterministic in-system test
- Generic, scalable, and modular scan selection logic
- X states blocked within groups of chains and scan shift cycles
- Very good observability of errors
- In-field and in-system tests comply with test quality standards
- Minimal amount of control data