ITC 2024 PO 24

Flexible Scan Test Architecture with Scalable Bus in 2.5D/3D Packaged Chips

Chandrakant(Chandra) Nalage
BROADCOM

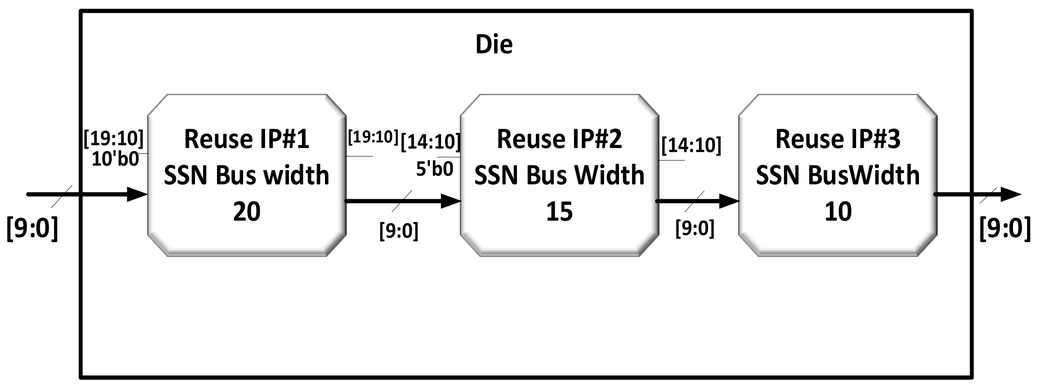
Vidya Neerkundar
SIEMENS

Introduction

2.5D and 3D integration of monolithic chiplets from different semiconductor process nodes is the new norm. The key challenges of concurrent cores tested in a traditional pin-muxed scan-access design are discussed in [1]. This poster describes the suitability of Tessent Streaming Scan Network (SSN) for reuse of IPs and chiplets in current and future generations of multi-die devices.

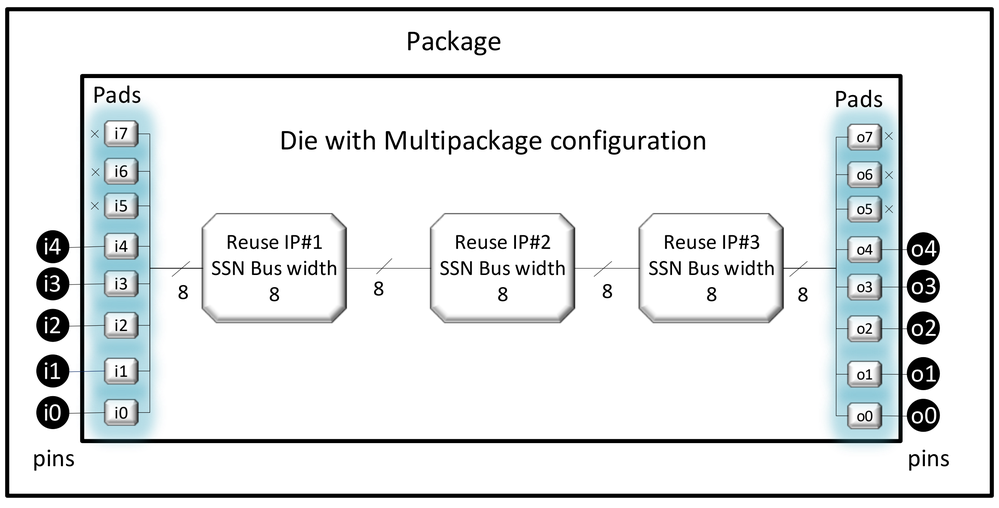
IP Core DFT Reuse

SSN allows scalable bus width down to 1-bit. The Digital IP cores designed with optimal bus width may be reused within the SOC/chiplet to be run with fewer bits. This is achieved by using the active LSB-bits of SSN bus during pattern retargeting. The same IP core can be re-used in different SOCs with varying SSN Bus width implementations.



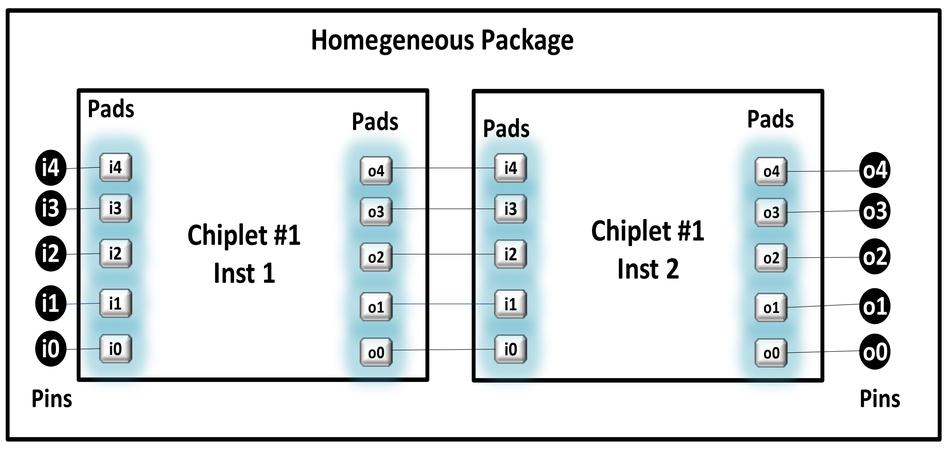
Die with Multi-Package Bonding Configuration

It is common for SOC/chiplet die with multi-package option to bond different sets of IOs depending upon market/performance need. Even though IOs are fixed at die-level, package level IOs can be less or equal to die IOs. This helps reduce test time by maximizing the SSN bus-width of the die depending on what the package can support.



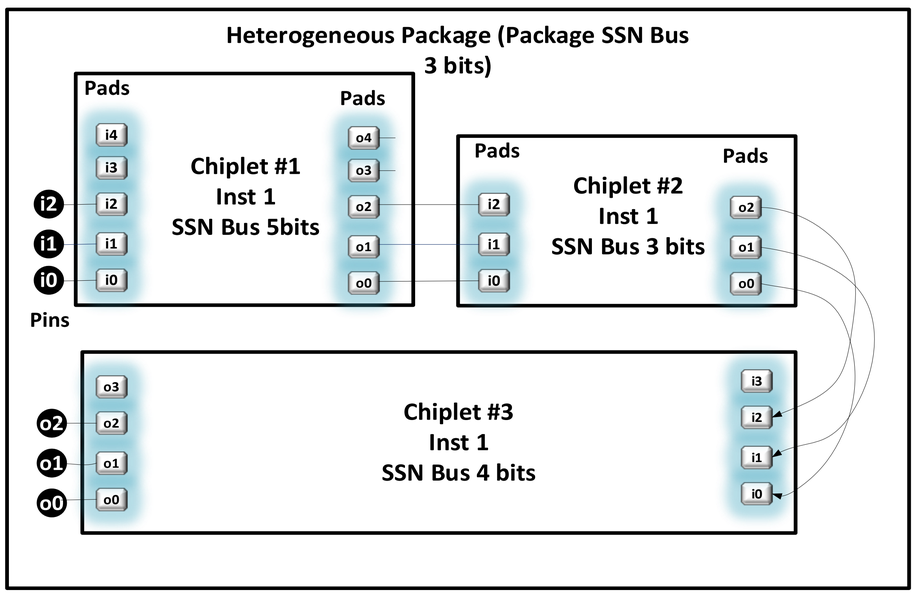
Chiplet in Homogenous Package Integration

In homogenous package integration, chiplets with the same or different modes or functionality are designed and integrated by a single chip supplier. Chiplets may not be designed from start, but rather reused from existing 2D monolithic dies. Depending on IO availability and routing resources at package-level, these chiplets can be integrated with full or reduced bus-width. Pattern retargeting is only needed if the package-level bus-width is smaller than the chiplet bus-width. Full test coverage is ensured without having to rearchitect the DFT for the chiplets.



Chiplet Reuse in Heterogeneous Package Integration

In heterogeneous packages, it is common to use chiplets from different vendors and different process nodes. The package can be pin-limited and not all chiplet test IOs can be brought out to package-level. If these chiplets have varying SSN bus-widths, they can be tested together on the same LSB-aligned SSN bus. Minor changes in the flow might be needed to achieve this. The combined test coverage at package-level will not be compromised.



Summary

With all the flexibilities of a scalable bus at IP core level, chiplet, and package, SSN is an ideal choice for scan testing complex chips with chiplets. Late design changes reduces the availability of package IOs pins. The topics discussed in this poster were used to avoid DFT implementation changes which would have impacted the chip schedule by up to a few months.