Wireless CPU® Quik Q2400 Series

Q2400
Product Specification

Revision: 005
Date: December 2006

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Q2400 Product Specification

Reference: WM_PRJ_Q24_PTS_003
Revision: 005
Date: December 27, 2006

Supports Open AT® embedded ANSI C applications

Document History

Revision	Date	List of revisions	
001	January 27, 2004	Creation	
002	December 17, 2004	Update according to the product upgrade Update document legal mentions.	
003	February 7, 2005	Update according to the product upgrade	
004	September 14, 2005	Update according to the product upgrade	
005	December 27, 2006	Modification of document format & naming Modification of the ON/ ~OFF paragraph Modification of the Battery charging paragraph Several other minor corrections (Microphone input impedance corrected)	

Caution

Information furnished herein by Wavecom is accurate and reliable. However, no responsibility is assumed for its use. Please read carefully the safety precautions for a terminal based on the Wireless CPU® Quik Q2400 Series.

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Open AT® Introduction:	www.wavecom.com/OpenAT
Developer support for software and hardware:	www.wavecom.com/forum

Overview

This document defines and specifies the Wireless CPU® QUIK Q2400, available under two GSM dual-band versions:

- **Q2400A**: E-GSM **900/1800** MHz with **16** Mbits of Flash memory and **2** Mbits of SRAM (16/2),
- **Q2400B**: E-GSM **900/1800** MHz with **32** Mbits of Flash memory and **4** Mbits of SRAM (32/4).

The Q2400 Wireless CPU® supports a powerful open software platform (Open AT®). Open AT® is the world's most comprehensive cellular development environment, which allows embedded standard ANSI C applications to be natively executed directly on the Wireless CPU®.

This Product Specification document covers the Wireless CPU® alone and does not include the programmable capabilities provided via the use of Open AT® Software Suites.

For detailed software programming guides, refer to the documents shown in the "References" section.

Contents

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1 References

1.1 Open AT® Software Documentation

[1] Getting Started with Open AT® (Ref. WM_ASW_OAT_CTI_00005)

[2] Open AT® Tutorial (Ref. WM_ASW_OAT_UGD_00050)

[3] Tools Manual (Ref. WM_ASW_OAT_UGD_00051)

[4] Open AT® Basic Development Guide (Ref. WM_ASW_OAT_UGD_00052)

[5] Open AT® ADL Guide (Ref. WM_ASW_OAT_UGD_00053)

[6] Open AT® V3.04 Customer Release Note (Ref. WM_DEV_OAT_DVD_135)

1.2 AT Software Documentation

[7] AT Commands Interface Guide for X52a (Ref. WM_ASW_OAT_UGD_00016)

[8] Customer Release Note X52a (Ref. WM_DEV_OAT_DVD_133)

1.3 Hardware Documents

[9] Quik Q2400 Customer Design Guidelines
(Ref. WM_PRJ_Q24_PTS_004)

[10] Quik Q2400 Series Process Customer Guidelines
(Ref. WM_PRJ_Q2400_PTS_006)

1.4 Other Documents

[11] Wavecom Acceptance and Verification Plan (Ref. WAVE Plan, Release 1.4)

[12] Power Consumption Modes Application Note
(Ref. WM_ASW_OAT_APN_012)

Note: All above documents are related to V3.04 Open AT® Software and 6.52a Open AT® Firmware. Wavecom recommends that the developer should check the web site for the latest documentation.

2 General Description

2.1 General Information

2.1.1 Features

The Quik Q2400 series are a self-contained E-GSM 900/1800 dual-band Wireless CPU®s including the following features:

2.1.1.1 Overall Dimensions

- 58.4 x 32.2 x 3.9 mm.

2.1.1.2 Power Consumption

- 2-Watt E-GSM 900 radio section running under 3.6 volts
- 1-Watt GSM1800 radio section running under 3.6 volts

2.1.1.3 Power Supply Voltage

- Digital section running under 2.8 volts
- 3V only SIM interface (for both 1.8 V and 5 V SIM interface with external adaptation, refer to document [9])

2.1.1.4 Capability

- Real Time Clock (RTC) with calendar
- Battery charge management
- Echo cancellation + noise reduction
- Full GSM software stack
- Complete shielding
- Complete interfacing through a 60-pin connector:
  - Power supply,
  - Serial link,
  - Audio,
  - SIM card interface,
  - Keyboard,
  - LCD.

2.1.2 External Connection

The Wireless CPU® Quik Q2400 has two external connections:

- RF connection pads (to the antenna),
- 60-pin General Purpose Connector (GPC) to Digital, Keyboard, Audio and Supply.

2.1.3 Additional Customizing Functions

The Wireless CPU® Quik Q2400 is designed to fit in very small terminals and only some custom functions must be added to make a complete dual-band solution:

- Keypad and LCD module,
- Earpiece and Microphone,
- Base connector,
- Battery,
- Antenna,
- SIM connector.

2.1.4 RoHS Compliance

The Wireless CPU® Q2400 is now compliant with RoHS (Restriction of Hazardous Substances in Electrical and Electronic Equipment) Directive 2002/95/EC which sets limits for the use of certain restricted hazardous substances. This directive states that "from 1st July 2006, new electrical and electronic equipment put on the market does not contain lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB), and polybrominated diphenyl ethers (PBDE)".

The Wireless CPUs which are compliant with this directive are identified by the RoHS logo on their label.

2.2 Functional Architecture

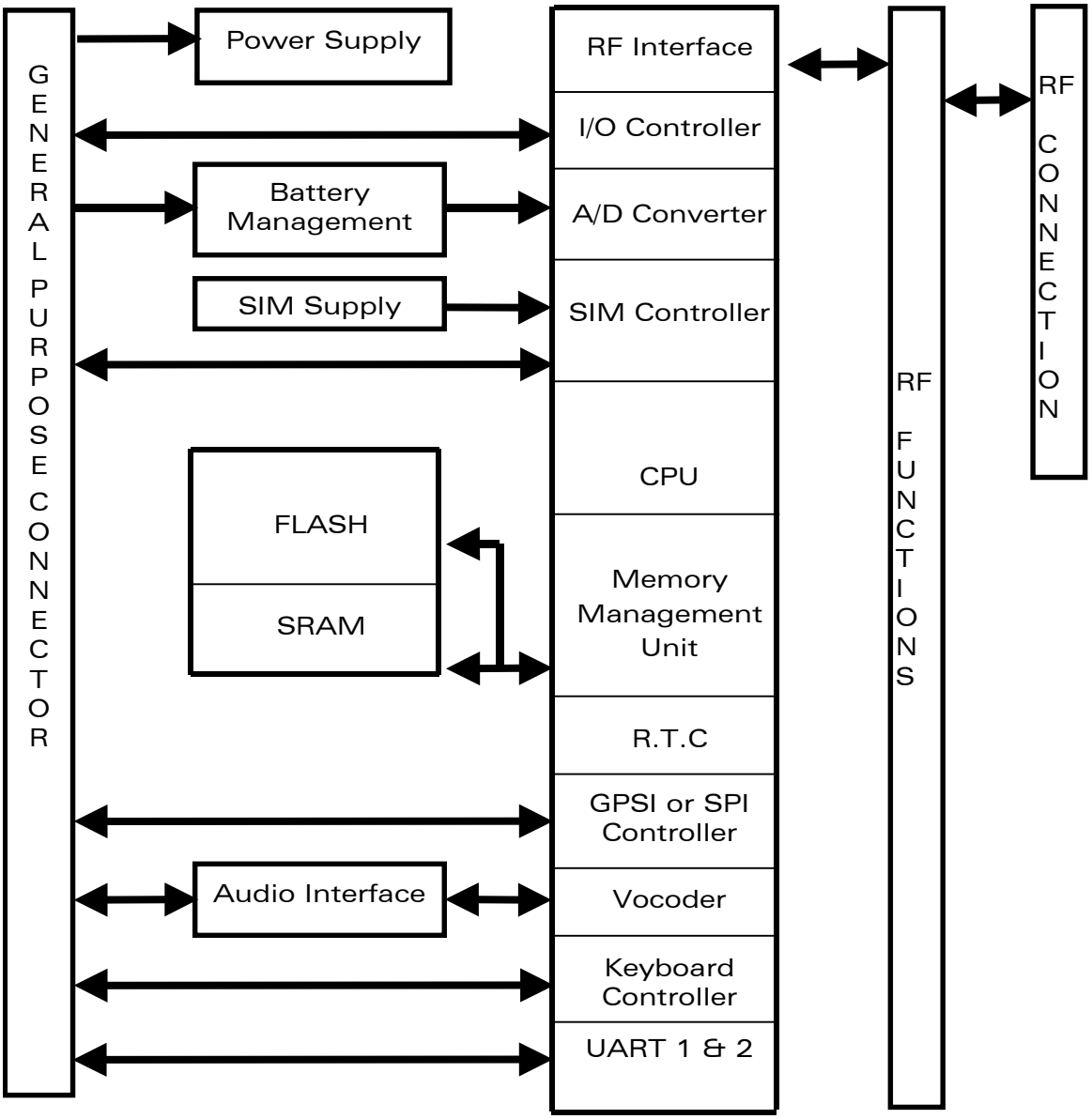


Figure 1: Functional architecture

2.2.1 RF Functionalities

The Radio Frequency (RF) functionalities comply with the Phase II E-GSM 900/DCS 1800 recommendations.

The Wireless CPU® Quik Q2400 frequencies are:

- Rx (E-GSM 900): 925 to 960 MHz
- Rx (DCS 1800): 1805 to 1880 MHz
- Tx (E-GSM 900): 880 to 915 MHz
- Tx (DCS 1800): 1710 to 1785 MHz

The Radio Frequency (RF) part is based on a specific dual-band chip including:

- Low-IF Receiver,
- Dual RF (Radio Frequency) synthesizer,
- Digital IF to Baseband Converter,
- Offset PLL (Phase Lock Loop) transmitter,
- 1 (logarithmic) Power Amplifier (PA) controller,
- Dual band Power Amplifier (PA) module.

2.2.2 Baseband Functionalities

The digital parts of the Wireless CPU® Quik Q2400 are based on a PHILIPS-VLSI chip (ONE C GSM).

This chipset uses a 0.25 µm mixed technology CMOS, which allows massive integration as well as low current consumption.

2.3 Firmware

The Wireless CPU® Quik Q2400 is designed to be integrated into various types of applications such as handsets or vertical applications (telemetry, multimedia).

For vertical applications, the firmware offers a set of AT commands to control the Wireless CPU® (for more information, refer to document [7]).

3 Interfaces

Note:

Some of the Wireless CPU® interface signals are multiplexed in order to limit number of pins but this architecture implies some limitation.

For example, in case of using SPI bus, 2-wire bus cannot be used.

Warning:

All external signals must be inactive when the Wireless CPU® is OFF to avoid any damage when starting and allow the Wireless CPU® to start correctly.

3.1 General Purpose Connector (GPC)

A 60-pin connector, with 0.5 mm pitch, is provided to interface the Wireless CPU® Quik Q2400 with a board containing either a LCD module, or a keyboard, or a SIM connector, or a battery connection.

The interfaces available on the GPC are described in the next sections.

The GPC is made by KYOCERA / AVX group with the following reference:

14 5087 060 930 861

The matting connector has the following reference:

24 5087 060 X00 861

For further details, refer to section 5.4 General Purpose Connector Data Sheet.

3.2 Power Supply

3.2.1 General Description

The power supply is one of the key factors in the design of a GSM terminal. Due to the burst emission in GSM, the power supply must be able to deliver high current peaks in a short time. During these peaks, the ripple (U_{ripp}) on the supply voltage must not exceed the specified limits, see the table "Maximum voltage ripple (U_{ripp}) vs Frequency in GSM & DCS" given below.

In communication mode, a GSM terminal emits 577 µs radio bursts every 4.615 ms.

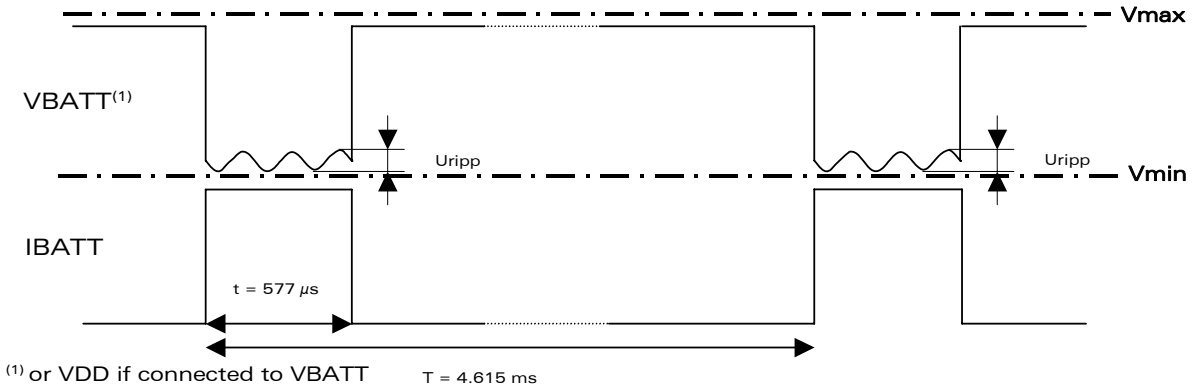


Figure 2: Typical power supply voltage in GSM mode

Two different inputs are provided for the power supply:

- VBATT is used to supply the RF part and
- VDD is used to supply the baseband part

Notes:

- It is possible to connect VBATT to VDD.
- In the event of separate power supply, they must be in the same state i.e either both active or inactive at the same time.

VBATT: Directly supplies the RF components with 3.6 V. It is essential to keep a minimum voltage ripple at this connection in order to avoid any phase error. The RF Power Amplifier current (2.0 A peak in GSM mode with a 50 Ω RF output) flows with a ratio of 1/8 of the time (around 577 µs every 4.615 ms for GSM).

The rising time is around 10 µs.

VDD: Supplies the +2.8 V ballast regulators of the Wireless CPU®. It is essential to keep the voltage over 3.1 volts at any time.

The Wireless CPU® shielding case is the grounding. The ground must be connected on the motherboard through a complete layer on the PCB.

Table 1: Power supply voltage

	V_{MIN}	V_{NOM}	V_{MAX}
VBATT	3.3 V (*)	3.6 V	4.5 V (**)
VDD	3.1 V		4.5 V

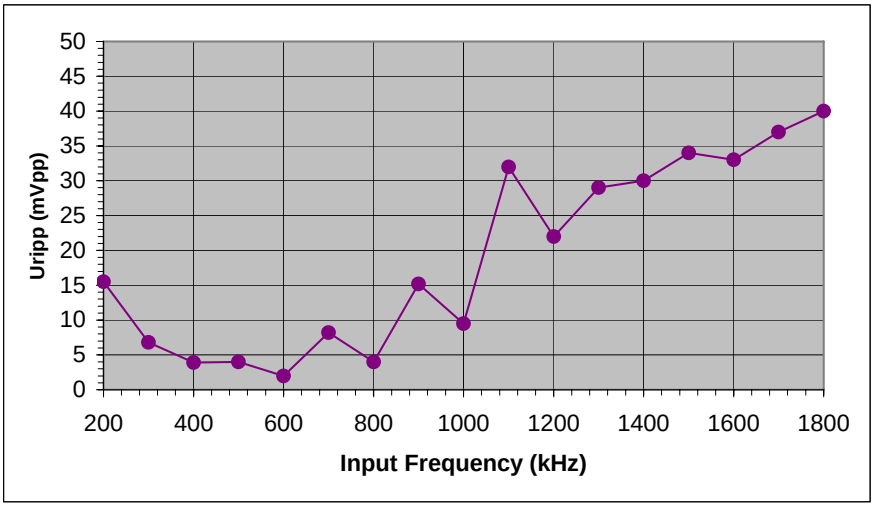
(*): This value must be guaranteed during the burst (with 2.0 A Peak in GSM mode).
(**): Max operating Voltage Stationary Wave Ratio (VSWR) 2:1.

When the Wireless CPU® is supplied with a battery, the total impedance (battery +contacts +protections +PCB) should be < 150 mΩ to limit voltage drop-out within emission burst.

As the radio power amplifier is directly connected to VBATT, the Wireless CPU® is sensitive to any Alternative Current on lines. When a DC/DC converter is used, Wavecom recommends setting the converter frequency in such a way that the resulting voltage does not exceed the values in following table and Figure 3.

Table 2: Maximum voltage ripple (Uripp) vs Frequency in GSM & DCS

Freq. (kHz)	U_{ripp} Max (mVpp)	Freq. (kHz)	U_{ripp} Max (mVpp)	Freq. (kHz)	U_{ripp} Max (mVpp)
<100	50	800	4	1500	34
200	15.5	900	15.2	1600	33
300	6.8	1000	9.5	1700	37
400	3.9	1100	32	1800	40
500	4	1200	22	>1900	40
600	2	1300	29		
700	8.2	1400	30		



for f<100kHz U_{ripp} Max = 50mVpp
for f> 1800kHz U_{ripp} Max = 40 mVpp

Figure 3: Maximum voltage ripple (Uripp) vs Frequency in GSM & DCS

For more information, refer to document [9] on Power Supply Design.

3.2.2 Power Consumption

The following information is given assuming a 50 Ω RF output.

Table 3: Power consumption in OFF mode (Wireless CPU® supplied, OFF state, no software running)

	Conditions	I_{NOM}	I_{MAX}
Overall consumption VBATT + VDD	Off	5 µA	10 µA

Table 4: Power consumption in E-GSM 900 MHz mode

	Conditions	I_{NOM}	I_{MAX}
VBATT+VDD	During TX bursts @Pcl5	1.60 A peak	1.8 A peak
	During RX bursts	110 mA peak	115 mA peak
	Average 1Rx/1Tx @Pcl5	250 mA	300 mA
	Average 1Rx/1Tx @Pcl8	190 mA	200 mA
	Average Idle mode	3 mA	7 mA

Power Control Level: Pcl5=2 W typ.; Pcl8=0.5 W typ.

Table 5: Power consumption in DCS 1800 MHz

	Conditions	I_{NOM}	I_{MAX}
VBATT+VDD	During TX bursts @Pcl0	1 A peak	1.5 A peak
	During RX bursts	130 mA peak	140 mA peak
	Average 1Rx/1Tx @Pcl0	190 mA	235 mA
	Average 1Rx/1Tx @Pcl3	150 mA	180 mA
	Average Idle mode	2 mA	6.5 mA

Power Control Level: Pcl0=1 W typ.; Pcl3=0.25 W typ.

Table 6: Power supply pin out

Signal	Pin number
+VBATT	55, 57, 58, 59, 60
VDD	11
GND	Shielding

The ground connection is made through the shielding ⇨ the four legs must be soldered to the ground plane.

3.3 Electrical Information for Digital I/O

All digital I/O comply with a 3 volts CMOS.

Table 7: Operating conditions

Parameter	I/O type	Min	Max	Condition
V_{IL}	CMOS	-0.5 V	0.8 V	
V_{IH}	CMOS	2.1 V	3.0 V	
V_{OL}	1X	0	0.2 V	I_{OL} = -1 mA
	2X	0	0.2 V	I_{OL} = -2 mA
	3X	0	0.2 V	I_{OL} = -3 mA
V_{OH}	1X	2.6 V	VCC	I_{OH} = 1 mA
	2X	2.6 V	VCC	I_{OH} = 2 mA
	3X	2.6 V	VCC	I_{OH} = 3 mA
I clamp	CMOS		40µA	Vf max = 0.33V

3.4 LCD Interface

The Wireless CPU® Quik Q2400 can be connected to a LCD module driver through either a SPI bus or a two-wire interface.

3.4.1 SPI Bus

The SPI bus includes a CLK signal (SPI_CLK), an I/O signal (SPI_IO) and an EN signal (SPI_EN) complying with SPI bus standard.

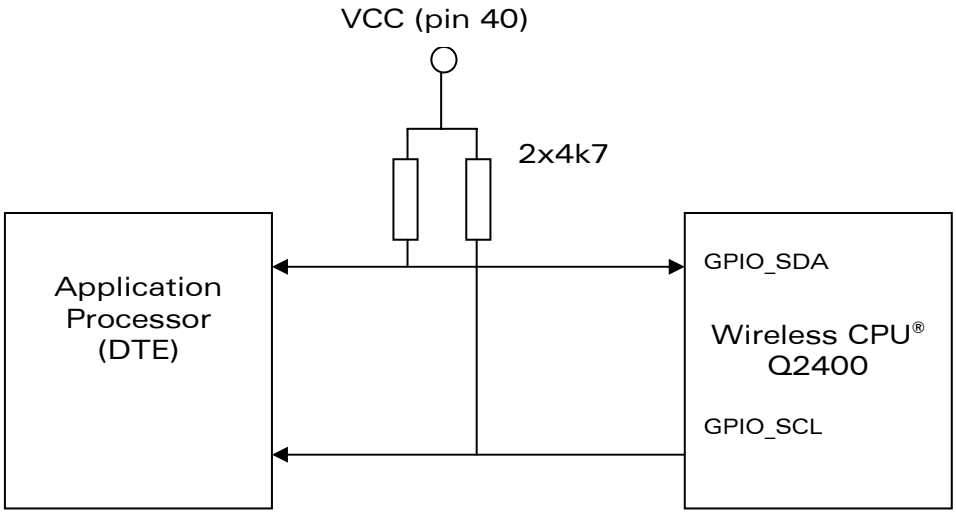
Table 8: SPI bus pin description

Signal	Pin number	I/O	I/O type	Reset State	Description	Multiplexed with
SPI_CLK	10	O	CMOS / 3X	Pull up	SPI Serial Clock	
SPI_IO	8	I/O	CMOS / 3X	Pull up	SPI Data	
SPI_EN *	28	O	CMOS / 3X	Output high	SPI Enable	GPO3

* Multiplexed with GPO3.

3.4.2 Two-wire Interface

A software emulated version of this interface using GPIOs is available. For more information, see "AT Command Interface Guide" [7].



3.5 SPI Auxiliary Bus

A second SPI Chip Enable (called SPI_AUX) must be used to add a SPI peripheral to the Wireless CPU® Quik Q2400.

Table 9: SPI auxiliary bus pin description

Signal	Pin number	I/O	I/O type	Reset State	Description	Multiplexed with
SPI_CLK	10	O	CMOS / 3X	Pull up	SPI Serial Clock	
SPI_IO	8	I/O	CMOS / 3X	Pull up	SPI Data	
SPI_AUX *	26	O	CMOS / 3X	Output high	SPI Aux. Enable	GPO0

* Multiplexed with GPO0.

3.6 Keyboard Interface

Warning:

This interface is not fully available with AT commands.

An AT command allows to get the input key code (see AT+CMER command description). This code is then to be processed by the application.

This interface provides 10 connections:

- 5 rows (ROW0 to ROW4) and
- 5 columns (COL0 to COL4).

The scanning is a digital one, and the debouncing is performed in the Wireless CPU®. No discrete components such as R, C (Resistor, Capacitor) are needed.

Table 10: Keyboard interface pin description

Signal	Pin number	I/O	I/O type	Description
ROW0	13	I/O	CMOS / 1X	Row scan
ROW1	15	I/O	CMOS / 1X	Row scan
ROW2	17	I/O	CMOS / 1X	Row scan
ROW3	19	I/O	CMOS / 1X	Row scan
ROW4	21	I/O	CMOS / 1X	Row scan
COL0	23	I/O	CMOS / 1X	Column scan
COL1	25	I/O	CMOS / 1X	Column scan
COL2	27	I/O	CMOS / 1X	Column scan
COL3	29	I/O	CMOS / 1X	Column scan
COL4	31	I/O	CMOS / 1X	Column scan

3.7 Main Serial Link (UART1)

A flexible 6-wire serial interface is available complying with V24 protocol signaling, but not with V28 (electrical interface) due to a 2.8 volts interface.

The signals are:

- TX data (CT103/TX),
- RX data (CT104/RX),
- Request To Send (CT105/RTS),
- Clear To Send (CT106/CTS),
- Data Terminal Ready (CT108-2/DTR),
- Data Set Ready (CT107/DSR).

The set of serial link signals are required for GSM DATA services application and is generated by the General Purpose I/O provided by the Wireless CPU®.

The 2 additional signals are Data Carrier Detect (CT109/DCD) and Ring Indicator (CT125/RI).

Table 11: UART1 pin description

Signal	Pin number	I/O	I/O type	Reset State	Description
CT103/TXD1	39	I	CMOS	High Z	Transmit serial data
CT104/RXD1	32	O	CMOS / 3X	Output high	Receive serial data
CT105/RTS1	30	I	CMOS	High Z	Request To Send
CT106/CTS1	37	O	CMOS / 3X	Output high	Clear To Send
CT107/DSR1	36	O	CMOS / 3X	Output high	Data Set Ready
CT108-2/DTR1	34	I	CMOS	High Z	Data Terminal Ready
CT109/DCD1	51	O	CMOS / 2X	High Z	Data Carrier Detect
CT125/RI1	54	O	CMOS / 2X	High Z	Ring Indicator
CT102/GND	Shielding legs	--	--	--	Ground

.

The rising and falling time of the reception signals (mainly CT103) must be less than 200 ns.

The Wireless CPU® Quik Q2400 is designed to operate using all the serial interface signals. In particular, it is necessary to use RTS and CTS signals for hardware flow control in order to avoid data corruption during transmission.

3.8 Auxiliary Serial Link (UART2)

For specific applications (e.g. Bluetooth connectivity) an auxiliary serial interface (UART2) will be available on the Wireless CPU® Q2400.

Table 12: UART2 pin description

Signal	Pin number	I/O	I/O type	Reset State	Description	Multiplexed with
CT103 / TXD2	18	I	CMOS	High Z	Transmit serial data	GPI
CT104 / RXD2	20	O	CMOS/3X	Output high	Receive serial data	GPO2
CT105 / RTS2	35	I	CMOS/3X	High Z	Request To Send	GPIO5
CT106 / CTS2	24	O	CMOS/3X	High Z	Clear To Send	GPIO0

3.9 SIM Interface

3.9.1 General Description

5 signals available are:

- SIM_VCC: SIM power supply
- SIM_RST: Reset
- SIM_CLK: Clock
- SIM_DATA: I/O port
- SIM_PRES: SIM card detect

The SIM interface controls a 3 V SIM card

Moreover, it is possible to manage either 1.8V/3V or 3V/5V SIM cards using an external voltage level shifter controlled by the GPO0 output signal (refer to document [9] on Customer Design Guidelines).

To be fully compliant with GSM 11.11 recommendations concerning SIM functions, please add shielding for each SIM signals on the PCB.

Table 13: SIM interface pin description

Signal	Pin number	I/O	I/O type	Description
SIM_CLK	3	O	2X	SIM Clock
SIM_RST	5	O	2X	SIM Reset
SIM_DATA	7	I/O	CMOS / 3X	SIM Data
SIM_VCC	9	O		SIM Power Supply
SIM_PRES	50	I	CMOS	SIM Card Detect

Table 14: SIM interface electrical characteristics

Parameter	Conditions	Min	Typ	Max	Unit
SIM_DATA V_{IH}	I_{IH} = ± 20 µA	0.7xSIM_VCC			V
SIM_DATA V_{IL}	I_{IL} = 1 mA			0.3xSIM_VCC	V
SIM_RST, SIM_DATA SIM_CLK V_{OH}	Source current = 20 µA	SIM_VCC – 0.1V			V
SIM_RST, SIM_DATA SIM_CLK V_{OL}	Sink current = -200 µA			0.1	V
SIM_VCC* Output Voltage	I_{SIMVCC} <= 6 mA	2.70	2.80	2.85	V
SIM_CLK Rise/Fall Time	Loaded with 30 pF			50	ns
SIM_RST, SIM_DATA Rise/Fall Time	Loaded with 30 pF			1	µs
SIM_CLK Frequency	Loaded with 30 pF			3.25	MHz

(*): Given for a 3 V interface. An external SIM driver is needed to handle 5 V SIMs.

Notes for SIM_PRES connection:

- When not used, **SIM_PRES** must be tied to VCC
- When used a **low** to **high** transition means that the SIM card is inserted and a **high** to **low** transition means that the SIM card is removed

3.10 General Purpose Input/Output

The Wireless CPU® Quik Q2400 provides:

- 3 General Purpose I/O,
- 4 General Purpose Outputs,
- 1 General Purpose Input.

They are used to control any external device such as a LCD or a Keyboard backlight.

Signal	Pin number	I/O	I/O type	Reset State	Description	Multiplexed with
GPIO0	24	I/O	CMOS / 3X	High Z	General Purpose I/O	CT106/CTS2
GPIO4	53	I/O	CMOS / 2X	Pull down	General Purpose I/O	
GPIO5	35	I/O	CMOS / 3X	High Z	General Purpose I/O	CT105/RTS2
GPO0	26	O	CMOS / 3X	Output high	General Purpose O	SPI_AUX
GPO1	22	O	CMOS / 3X	Output low	General Purpose O	
GPO2	20	O	CMOS / 3X	Output high	General Purpose O	CT104/RXD2
GPO3	28	O	CMOS / 3X	Output high	General Purpose O	SPI_EN
GPI	18	I	CMOS	Pull down	General Purpose I	CT103/TXD2

3.11 Activity Status Indication

The activity status indication signal is used to drive a LED through an open-collector transistor according to the Wireless CPU® activity status.

LED status	Wireless CPU® Quik Q2400 status	
OFF	Wireless CPU® in download mode or Wireless CPU® OFF	
ON	Permanent	Wireless CPU® switched ON, not registered on the network
	Slow flash LED ON for 200 ms, OFF for 2 s	Wireless CPU® switched ON, registered on the network
	Quick flash LED ON for 200 ms, OFF for 600 ms	Wireless CPU® switched ON, registered on the network, communication in progress

Table 15: Activity status indication

Signal	Pin number	I/O	I/O type	Reset State	Description
FLASH LED	52	I/O	CMOS / 2X	High Z	General Purpose I/O

3.12 Analog to Digital Converter (ADC)

An Analog to Digital Converter is provided by the Wireless CPU®. This converter is a 10-bit resolution, ranging from 0 to 2.8 V.

Table 16: ADC pin description

Signal	Pin number	I/O	I/O type	Description
AUXV0	33	I	Analog	A/D converter

Table 17: ADC electrical characteristics

Parameter	Min	Max	Unit
Resolution	10		bits
Sampling period	10		s
Input signal range	0	2.8V	V
ADC reference accuracy	0.75	2	%
Integral accuracy	+/- 1		LSB
Differential accuracy	+/- 1		LSB
Input impedance (R)	10		MΩ
Input impedance (C)		100	nF

3.13 Audio Interface

Two different microphone inputs and two different speaker outputs are supported.

The Wireless CPU® Quik Q2400 also includes an echo cancellation feature, which allows hands-free function.

In some cases, ESD protection must be added on the audio interface lines.

3.13.1 Microphone Inputs

The MIC2 inputs already include the biasing for an electret microphone allowing an easy connection to a handset.

The MIC1 inputs do not include an internal bias. MIC1/SPK1 is then appropriate for a hands-free system or a handset with biasing external to the Wireless CPU®.

3.13.1.1 Common Microphone Input Characteristics

The connection can be either differential or single-ended but using a differential connection in order to reject common mode noise and TDMA noise is strongly recommended. When using a single-ended connection, ensure a good ground plane, a good filtering as well as shielding, in order to avoid any disturbance on the audio path.

The gain in MIC inputs is internally adjusted and can be tuned from 30 dB to 51 dB by using an AT command (refer to AT commands documentation [7]).

The two microphone inputs are composed of a 1st order high pass filter with a cut-off frequency of 330 Hz.

Table 18: Microphone gain vs Max input voltage at 1kHz (using controller 1*)

Transmit Gain (dB)	Max Vin (mVrms)
+30	43.80
+33	31.01
+36	21.95
+39	15.54
+42	11
+45	7.79
+48	5.51
+51	3.9

(*) For more details, refer to AT commands documentation [7]

Table 19: Microphone gain vs Max input voltage at 1kHz (using controller 2*)

Transmit Gain (dB)	Max Vin (mVrms)	Transmit Gain (dB)	Max Vin (mVrms)
-6.5 to -4	2274	18.8 to 21.3	123.4
-3.5 to -2	1806	21.8 to 24.3	87.39
-1.5 to 0	1434	24.8 to 27.3	61.87
0.5 to 2	1139	27.8 to 30.3	43.8
2.5 to 4	905	30.8 to 33.3	31.01
4.5 to 6	719	33.8 to 36.3	21.95
6.5 to 8	571	36.8 to 39.3	15.54
8.5 to 10	454	39.8 to 42.3	11
10.8 to 12.3	348	42.8 to 45.3	7.79
12.8 to 15.3	246.3	45.8 to 48.3	5.51
15.8 to 18.3	174.4	48.8 to 51.3	3.9

(*) For more details, refer to AT commands documentation [7]

Table 20: Internal audio filter characteristics

Frequency	Gain
0-150 Hz	< -22 dB
150-180 Hz	< -11 dB
180-200 Hz	< -3 dB
200-3700 Hz	0 dB
>4000 Hz	< -60 dB

The Table 20 gives internal audio filter characteristics. This filter is located after controller 1 and 2 and is a digital filter. This filter meets all CCITT recommendations in terms of frequency response. There is an additional selective filter, which allows rejecting the 216.7 Hz generated by the GSM frame period (TDMA).

3.13.1.2 Main Microphone Inputs (MIC2)

The MIC2 inputs are differential ones. They already include the convenient biasing for an electret microphone (1 mA and 2 V). This electret microphone can be directly connected on these inputs.

The impedance of the microphone 2 must be around 2 kΩ. These inputs are the standard ones for a handset design. The input impedance is around 1.4kΩ +/- 20% between 400Hz and 4000Hz.

AC coupling is already embedded in the Wireless CPU®.

Table 21: MIC 2 pin description

Signal	Pin #	I/O	I/O type	Description
MIC2P	46	I	Analog	Microphone 2 positive input
MIC2N	48	I	Analog	Microphone 2 negative input

3.13.1.3 Auxiliary Microphone Inputs (MIC1)

The MIC1 inputs are differential and do not include internal bias. To use these inputs with an electret microphone, bias must be generated outside the Wireless CPU® Quik Q2400 according to the characteristic of this electret microphone. These inputs are the standard ones used either for an external headset or a hands-free kit.

These inputs are provided either for an external headset or a hands-free kit. The input impedance is around 10kΩ +/- 30% between 400Hz and 4000Hz

AC coupling is already embedded in the Wireless CPU®.

Table 22: MIC 1 pin description

Signal	Pin #	I/O	I/O type	Description
MIC1P	42	I	Analog	Microphone 1 positive input
MIC1N	44	I	Analog	Microphone 1 negative input

3.13.2 Speaker Outputs

3.13.2.1 Common Speaker Output Characteristics

The connection can be differential or single-ended but using a differential connection to reject common mode noise and TDMA noise is strongly recommended. Moreover, in single-ended mode, ½ of the power is lost. When using a single-ended connection, ensure a good ground plane, a good filtering as well as shielding, in order to avoid any disturbance on the audio path.

Speaker outputs SPK1 and SPK2 are push-pull amplifiers and can be loaded down to 150 Ω and up to 1 nF (see details in table *Speaker gain vs Max output voltage).*

Impedance of the speaker amplifier output in differential mode is:
R ≤ 1Ω +/-10 %.

These outputs are differential and the output power can be adjusted by step of 2 dB. The output can be directly connected to a speaker.

Using a single-ended connection also includes losing half of the output power compared to a differential connection.

The speaker output gain is internally adjusted and can be tuned by using an AT command.

Table 23: Speaker gain vs Max output voltage

Receive Gain (dB) (*)	Max output level (Vrms)	Max.speaker load (Ω)
+2	1.74	150
0	1.38	50
-2	1.099	32
-4	0.873	32
-6	0.693	32
-8	0.551	32
-10	0.437	32
-12	0.347	32
-14	0.276	32
-16	0.219	32
-18	0.174	32
-20	0.138	32
-22	0.110	32
-24	0.087	32
-26	0.069	32

(*) Analog gain: May not be significant

3.13.2.2 Speaker 2 Output

Table 24: Speaker 2 pin description

Signal	Pin #	I/O	I/O type	Description
SPK2P	45	O	Analog	Speaker 2 positive output
SPK2N	47	O	Analog	Speaker 2 negative output

3.13.2.3 Speaker 1 Output

Table 25: Speaker 1 pin description

Signal	Pin #	I/O	I/O type	Description
SPK1P	41	O	Analog	Speaker 1 positive output
SPK1N	43	O	Analog	Speaker 1 negative output

3.13.3 Buzzer Output

The buzzer output (BUZ) is a digital one. A buzzer can be directly connected between this output and VBATT. The maximum current is 80 mA (PEAK).

Table 26: Buzzer pin description

Signal	Pin #	I/O	I/O type	Description
BUZ	49	O	Analog (open collector)	Buzzer output

Table 27: Buzzer operating conditions

Parameter	Condition	Min	Max	Unit
V_{OL}	$I_{AVERAGE}$ = 40 mA		0.6	V
I_{PEAK}	VBATT = VBATTmax		80	mA
$I_{AVERAGE}$	VBATT = VBATTmax		40	mA

3.14 Battery Charging Interface

The Wireless CPU® Quik Q2400 supports one battery charging circuit and 2 algorithms for 3 batteries technologies:

- Ni-Cd (Nickel-Cadmium) with algorithm 0
- Ni-Mh (Nickel-Metal Hydrure) with algorithm 0
- Li-Ion (Lithium-Ion) with algorithm 1

The two algorithms control a switch, which connects the CHG-IN signal to the VBATT signal. The algorithm controls the frequency and the connected time of the switching. During the charging procedure the battery charging level is controlled and when Li-Ion algorithm is used, the battery temperature is monitoring thorough the BAT_TEMP ADC input.

Notes:

- Software before X55 version supports algorithm 0 only. (Ni-Cd / Ni-Mh charging algorithm).
- Due to memory size, Wireless CPU® Quik Q2400A supports only X4x software version. Li-Ion charging algorithm is not yet supported

Table 28: Pin description of battery charging interface

Signal	Pin number	I/O	I/O type	Description
CHG-IN	1,2,4	I	Supply	Current source input
BAT_TEMP	38	I	Analog	A/D converter

Table 29: Electrical characteristics of battery charging interface

Parameter		Minimum	Typ	Maximum	Unit
BAT_TEMP (pin 38)	Resolution		10		bits
	Input Impedance (R)	4.7			kΩ
	Input Impedance (C)			100	nF
	Sampling period		10		s
	Input signal range	0		2.8	V
CHG-IN (pin 1,2,4)	Voltage (for I=Imax)	5.1*		5.5	V
	Current Imax			800	mA

* To be parameterized as per battery manufacturer

3.14.1 Ni-Cd / Ni-Mh Charging Algorithm

To charge the battery, the algorithm measures the battery level when the switch is opened T2 and charges the battery by closing the switch T3. When the battery is charged (battery voltage reached BattLevelMax) the switch is opened during the time T3.

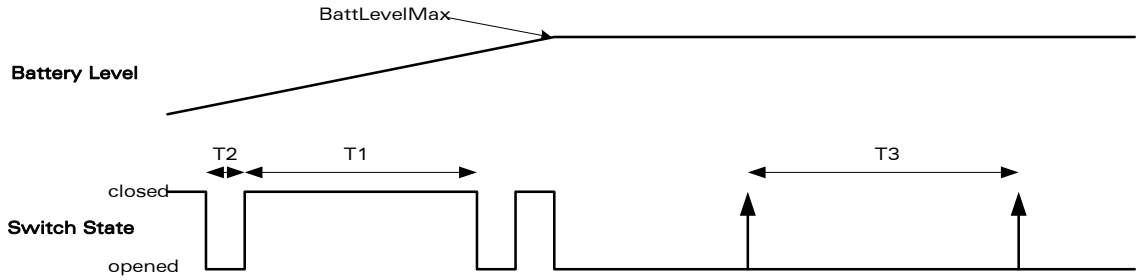


Figure 4: Ni-Cd / Ni-Mh charging waveform

Table 30: Electrical characteristics of Ni-Cd / Ni-Mh battery timing charge

Parameter	Min	Typ	Max	Unit
T1		1		s
T2		0.1		s
T3		5		s

Note: T1,T2,T3 and BattLevelMax can be configured by AT command.

The battery level is monitoring by the software, but not the temperature.

3.14.2 Li-Ion Charging Algorithm (only with software higher X55 version)

The Li-Ion algorithm, provides the temperature monitoring of the battery, which is highly recommended to prevent the damage of battery during the charging phase.

The Li-Ion charger algorithm can be decomposed in 3 phases:

1. Constant charge
2. Beginning of pulse charge
3. End of pulse charge

The three phases can be seen on the following waveform of a complete charge:

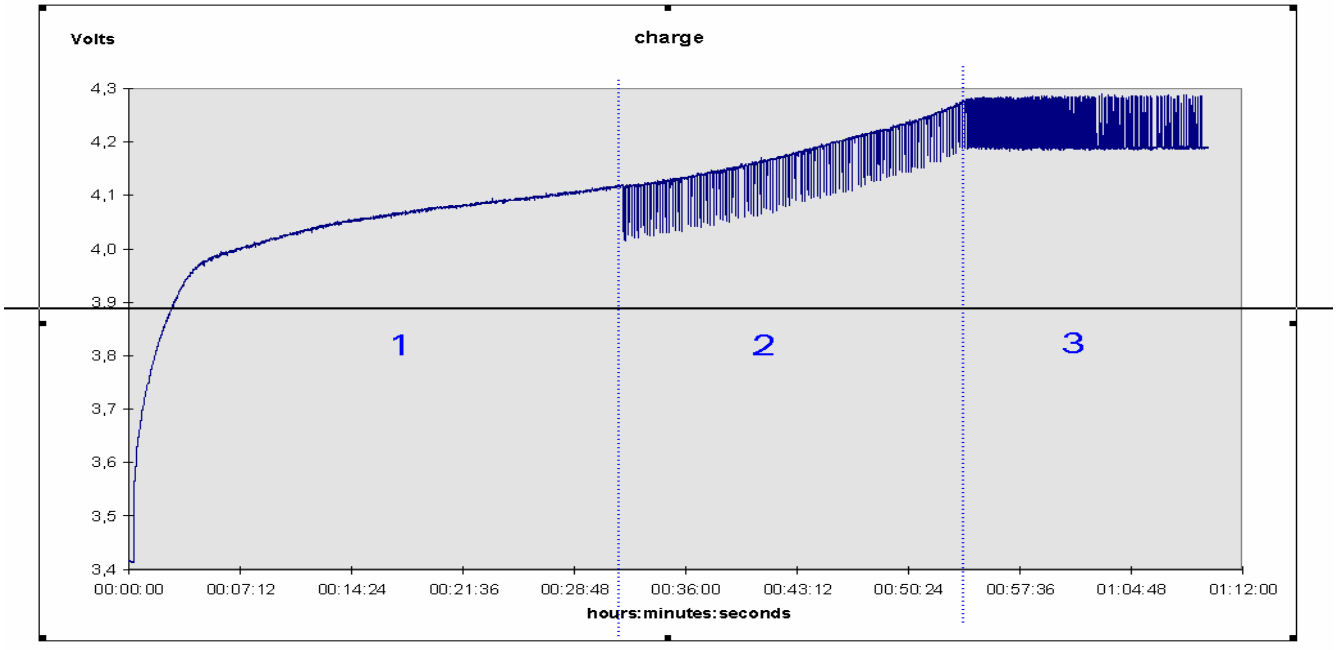


Figure 5: Li-Ion full charging waveform

Table 31: Electrical characteristics of Li-Ion battery timing charge

Step	Switch	Min	Typ	Max	Unit
1	Closed		always		s
2	Opened		0.1		s
	Closed		1		s
3	Opened	0.1		10	s
	Closed		1		s

3.14.3 Temperature Monitoring

The temperature monitoring is available only for the Li-Ion battery with the algorithm number 1. The BAT_TEMP (pin 38) ADC input must be used to sample the temperature analog signal provided by a NTC temperature sensor. The minimum and maximum temperature range can be set by using an AT command.

3.15 ON / ~OFF

3.15.1 General Description

This input is used to switch ON or OFF the Wireless CPU®.

A high level signal must be provided on the ON/~OFF pin to switch ON the Wireless CPU®.

To switch OFF, the ON/~OFF signal must be reset and an AT+CPOF command must be sent to the Wireless CPU®.

Table 32: ON/~OFF pin description

Signal	Pin number	I/O	I/O type	Description
ON/~OFF	6	I	CMOS	Wireless CPU® Power ON/OFF

Table 33: ON/~OFF electrical characteristics

Parameter	Min	Max	Unit
Input Impedance (R)	10		kΩ
Input Impedance (C)		50	pF

Table 34: ON/~OFF operating conditions

Parameter	I/O type	Min	Max	Unit
V_{IL}		0 V	0.6 V	V
V_{IH}		2.4 V	VDD+0.5 V	V

Warning:

All external signals must be inactive when the Wireless CPU® is OFF to avoid any damage when starting and allow Wireless CPU® to start and stop correctly.

3.15.2 Operating Sequences

3.15.2.1 Power-ON

Once the Wireless CPU® is supplied, the ON/~OFF signal must be asserted high during a delay of $T_{on-hold}$ (Hold delay on the ON/~OFF signal) to power-ON.

After this delay, once the firmware has completed its power-up sequence, an internal logic maintains the Wireless CPU® in power-ON condition.

You must not de-assert this ON/~OFF signal before this internal logic is internally asserted by the firmware; the Wireless CPU® would not start-up otherwise.

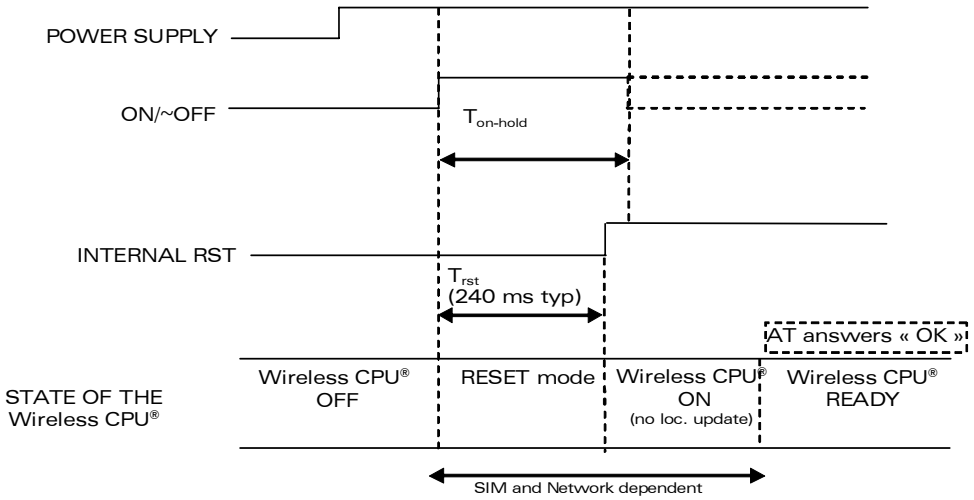


Figure 6: Power-ON sequence diagram (no PIN code activated)

The duration of the firmware power-up sequence depends on several factors:

- firmware version used by the Wireless CPU®,
- need to perform a recovery sequence if the power has been lost during a flash memory modification.

Other factors have a minor influence on

- number of parameters stored in EEPROM by the AT commands received so far
- ageing of the hardware components, especially the flash memory
- temperature conditions

The *recommended* way to de-assert the ON/~OFF signal is to use either an AT command or WIND indicators: the application must detect the end of the power-up initialization and de-assert ON/~OFF afterwards.

- Send an "AT" command and wait for the "OK" answer: once the initialization is complete the AT interface answers « OK » to "AT" message[1].
- Wait for the "+WIND: 3" message: after initialization, the Wireless CPU®, if configured to do so, will return an unsolicited "+WIND: 3" message. The generation of this message is enabled or disabled via an AT command.

Note:
For more information on these commands, see also "AT Commands Interface Guide" [7].

Proceeding thus – by software detection - will always prevent the application from de-asserting the ON/~OFF signal too early.

If WIND indicators are disabled or AT commands unavailable or not used, it is still possible to de-assert ON/~OFF after a delay long enough ($T_{on\text{-}hold}$) to ensure that the firmware has already completed its power-up initialization.

The table below gives the minimum values of $T_{on\text{-}hold}$ for all firmware versions:

Table 35: $T_{on\text{-}hold}$ minimum values

Open AT® Firmware	$T_{on\text{-}hold}$ Safe evaluations of the firmware power-up time
X.4x	8 s
X.5x (excepted 6.57)	24 s if Open AT® is used
	8 s otherwise
6.57 & above	8 s

The above figures take the worst cases into account: power-loss recovery operations, slow flash memory operations in high temperature conditions, and so on. But they are safe because they are large enough to ensure that ON/~OFF is not de-asserted too early.

Additional Notes:

1. Typical power-up initialization time figures for best cases conditions (no power-loss recovery, fast and new flash memory...) approximate 3.5 seconds in every firmware version. But releasing ON/~OFF after this delay does not guarantee that the application will actually start-up if for example the power plug has been pulled off during a flash memory operation, like a phone book entry update or an AT&W command
2. The ON/~OFF signal can be left at a high level until switch OFF. But this is not recommended as it will prevent the AT+CPOF command from performing a clean power-off. (see also Note in section 3.15.2.2 Power-OFF for an alternate usage)

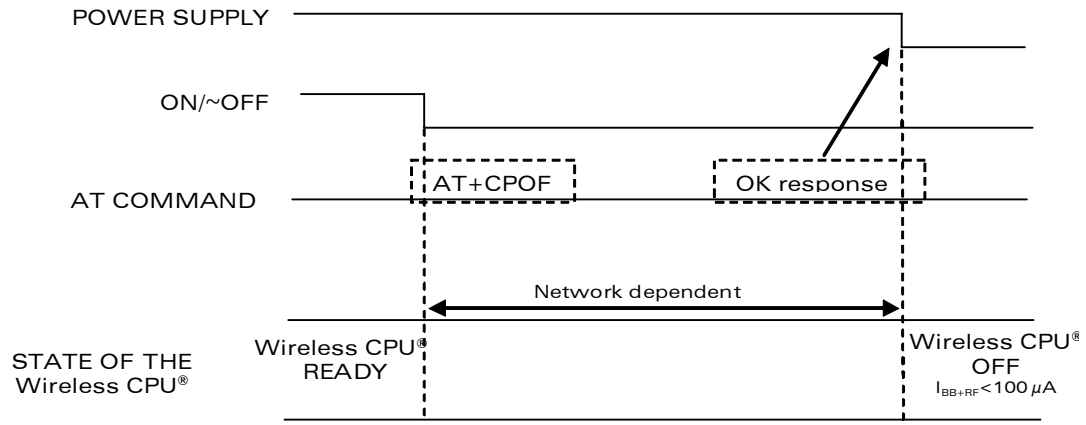
[1] If the application manages hardware flow control, the AT command can be sent during the initialisation phase.

3. When using a battery as power source, it is not recommended to let this signal high:
   If the battery voltage is too low and the ON/~OFF signal at low level, an internal mechanism switches OFF the Wireless CPU®. This automatic process prevents the battery to be over discharged and optimize its life span.
4. During the power-ON sequence, an internal reset is automatically performed by the Wireless CPU® for 240 ms (typical). Any external reset should be avoided during this phase.
5. Connecting a charger on the Wireless CPU® as exactly the same effect than setting the ON/~OFF signal. In particular the Wireless CPU® will not power-OFF after the AT+CPOF command, unless the Charger is disconnected.

3.15.2.2 Power-OFF

To properly power-OFF the Wireless CPU®, the application must reset the ON/~OFF signal to low and then send the AT+CPOF command to de-register from the network and switch off the Wireless CPU®.

Once the « OK » response is issued by the Wireless CPU®, the external power supply can be switched OFF.



I_{BB+RF} = overall current consumption (Base Band + RF part)

Figure 7: Power-OFF sequence diagram

Note:

- If the ON/~OFF pin is maintained to ON (High Level) then the Wireless CPU® cannot be switched OFF and after using AT+CPOF command through the firmware the Wireless CPU® enters in a Open AT® Max power consumption Mode (please refer to the Power Consumption Modes Application Note [12]).

3.16 BOOT (optional)

This input can be used to download software in the Flash memory of the Wireless CPU®.

For the applications based on AT commands, this is a backup download procedure only (refer to document [9] on Customer Design Guidelines).

The internal BOOT procedure is started when this pin is low during the reset of the Wireless CPU®.

In normal mode, this pin must be left open. In Internal BOOT mode, low level must be set through a 1kΩ resistor. If used, this input must be driven either by an open collector or an open drain output:

- BOOT pin 12 = 0, for download mode,
- BOOT pin 12 = 1, for normal mode.

Table 36: BOOT pin description

Signal	Pin number	I/O	I/O type	Description
BOOT	12	I	CMOS	Flash Downloading

Note: The nominal firmware download procedure is using the X-modem.

3.17 Reset Signal (~RST)

3.17.1 General Description

This signal is used to force a reset procedure by providing low level for at least 500 µs.

This signal must be considered as an emergency reset only. A reset procedure is automatically driven by an internal hardware during the power-up sequence.

This signal can also be used to provide a reset to an external device. It then behaves as an output. If no external reset is necessary this input can be left open. If used (emergency reset), it must be driven either by an open collector or an open drain output:

- ~RST pin 14 = 0, for Wireless CPU® Reset,
- ~RST pin 14 = 1, for normal mode.

Table 37: Reset pin description

Signal	Pin number	I/O	I/O type	Description
~RST	14	I/O	SCHMITT	Wireless CPU® Reset

Table 38: Reset electrical characteristics

Parameter	Min	Max	Unit
Input impedance (R)	4.7		kΩ
Input impedance (C)		10	nF

Table 39: Reset operating conditions

Parameter	Min	Max	Condition
$*V_{T-}$	1.1 V	1.2 V	
$*V_{T+}$	1.7 V	1.9 V	
V_{OL}		0.4 V	I_{OL} = -50 µA
V_{OH}	2.0 V		I_{OH} = 50 µA

* V_{T-}, V_{T+} : Hysteresis thresholds

Additional comments on Reset:

The Reset process is activated either by the external ~RST signal or by an internal signal (coming from a Reset generator). This automatic reset is activated at Power-up.

The Wireless CPU® remains in Reset mode as long as the ~RST signal is held low.

This signal should be used only for "emergency" resets.

A software reset is always preferred to a hardware reset.

3.17.2 Reset Sequence

To activate the « emergency » reset sequence, the ~RST signal must be set to low for 500 µs minimum.

As soon as the reset is completed, the AT interface answers « OK » to the application. For this, the application must send AT↵. If the application manages hardware flow control, the AT command can be sent during the initialization phase. Another solution is to use the AT+WIND command to get an unsolicited status from the Wireless CPU®.

For further details, refer to AT commands documentation [7].

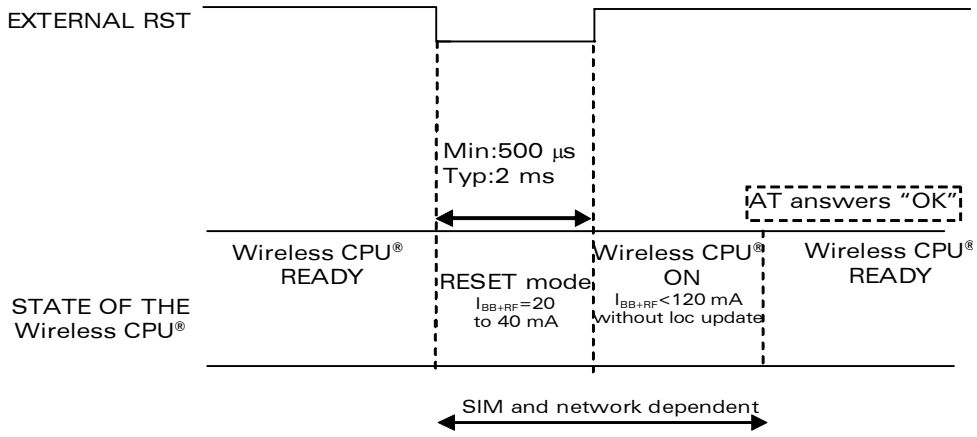


Figure 8: Reset sequence diagram

3.18 External Interrupt (~INTR)

The Wireless CPU® provides an external interrupt input ~INTR. This input is very sensitive and an interrupt is activated on high to low edge. If this signal is not used, it can be left open. If used, this input must be driven either by an open collector or an open drain output.

This input is used, for instance, to power-OFF automatically the Wireless CPU®.

Table 40: External interrupt pin description

Signal	Pin number	I/O	I/O type	Description
~INTR	16	I	CMOS	External Interrupt

Table 41: External interrupt electrical characteristics

Parameter	Min	Max	Unit
V_{IL}	-0.5	0.7	volt
V_{IH}	2.2	3.0	volt

3.19 VCC Output

This output can be used to power some external functions. VCC must be used as a digital power supply. This power supply is available when the Wireless CPU® is ON.

Table 42: VCC output pin description

Signal	Pin number	I/O	I/O type	Description
VCC	40	O	Supply	Digital supply

Table 43: VCC output operating conditions

Parameter	Condition	Min	Max	Unit
Output voltage	I = 10 mA	2.74	2.86	V
Output current			10	mA

3.20 Real Time Clock Supply (VCC_RTC)

The VCC_RTC input is used to provide a back-up power supply for the internal Real Time Clock (RTC). The RTC is supported by the Wireless CPU® when powered on but a back-up power supply is necessary to save date and time information when the Wireless CPU® is switched OFF.

If the RTC is not used, this pin can be left open.

Table 44: VCC_RTC pin description

Signal	Pin number	I/O	I/O type	Description
VCC_RTC	56	I/O	Supply	RTC Back-up supply

Table 45: VCC_RTC operating conditions

Parameter	Condition	Min	Max	Unit
Input voltage		2	2.75	V
Input current	VCC=0 V; t° = +25 °C VCC_RTC=2.5 V		3	µA
Input current	VCC=0 V; t°:-20 °C / +55 °C VCC_RTC=2.5 V		10	µA
Output voltage		2.4	2.75	V
Output current			2	mA

3.21 RF Interface

The impedance is 50 Ω nominal and the DC impedance is 0 Ω.

3.21.1 RF Connections

The antenna is connected to the Wireless CPU® through a coaxial cable. This cable is connected to both the "Antenna pad" (or Round pad) and the "Ground pad" (see Figure 9). It is recommended to use a **RG178 coaxial cable**.

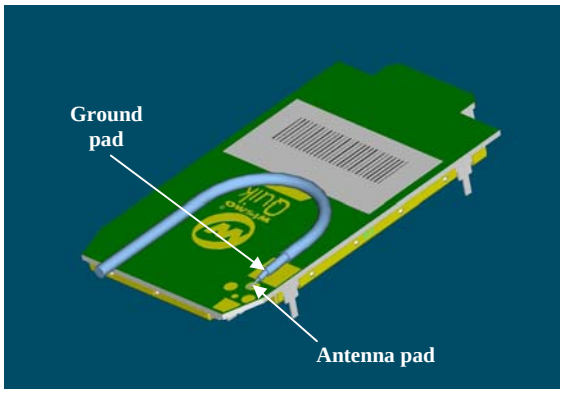


Figure 9: Antenna connection

Notes:

- The Wireless CPU® Quik Q2400 sub-series does not include any antenna switch for a car kit, but this function can be implemented externally and it can be driven by using a GPIO
- The antenna cable and connector must be selected in order to minimize losses in the frequency bands used for GSM 850/E-GSM 900MHz and DCS 1800/PCS 1900MHz
- 0.5 dB can be considered as a maximum value for loss between the Wireless CPU® and an external connector
- In order to maintain the RoHS status of the Wireless CPU®, Wavecom recommends that *lead-free solder-wire* and flux be used for Wireless CPU® assembly on the motherboard and RF cable assembly on the Wireless CPU®

For example:

- Solder-Wire: Kester 245 Cored 58 (Sn96.5Ag3Cu0.5)
- Flux: Kester 952-D6

3.21.2 RF Performances

RF performance is compliant with the ETSI recommendation GSM 05.05.

The main parameters for a **Receiver** are:

- E-GSM900 Reference Sensitivity = -104 dBm Static & TUHigh,
- DCS1800 Reference Sensitivity = -102 dBm Static & TUHigh,
- Selectivity @ 200 kHz: > +9 dBc,
- Selectivity @ 400 kHz: > +41 dBc,

- Linear dynamic range: 63 dB,
- Co-channel rejection: >= 9 dBc,

and for a **Transmitter**:

- Maximum output power (E-GSM 900): 33 dBm +/- 2 dB at ambient temperature,
- Maximum output power (DCS1800): 30 dBm +/- 2 dB at ambient temperature,
- Minimum output power (E-GSM 900): 5 dBm +/- 5 dB at ambient temperature,
- Minimum output power (DCS1800): 0 dBm +/- 5 dB at ambient temperature.

3.21.3 Antenna Characteristics

WAVECOM recommends using an antenna with the following characteristics:

Table 46: Antenna specifications

Characteristic		E-GSM 900	DCS 1800
Frequency TX		880 to 915 MHz	1710 to 1785 MHz
Frequency RX		925 to 960 MHz	1805 to 1880 MHz
Impedance		50 Ω	
VSWR	Rx max	1.5 :1	
	Tx max	1.5 :1	
Typical radiated gain		0 dBi in one direction at least	

Frequency depends on the application. A dual-band antenna may work in all these frequency bands.

4 Technical Specifications

4.1 General Purpose Connector Pin Out Description

Table 47: General Purpose Connector pin out description

Pin #	Signal	I/O	I/O type	Reset State	Description	Comment
1	CHG_IN	I	Supply	--	Supply for battery charging	High current Not connected if not used
2	CHG_IN	I	Supply	--	Supply for battery charging	High current Not connected if not used
3	SIM_CLK	O	CMOS/2X	Output low	Clock for SIM interface	
4	CHG_IN	I	Supply	--	Supply for battery charging	High current Not connected if not used
5	SIM_RST	O	CMOS/2X	Output low	Reset for SIM interface	
6	ON/~OFF	I	CMOS		Power ON/OFF control	
7	SIM_DATA	I/O	CMOS/3X	Output low	I/O for SIM interface	
8	SPI_IO	I/O	CMOS/3X	Pull up	Wire interface or SPI Serial Data	100 kΩ Pull-up inside
9	SIM_VCC	O	Supply	--	SIM card supply	6 mA max
10	SPI_CLK	O	CMOS/3X	Pull up	Wire interface or SPI Serial clock	100 kΩ Pull-up inside
11	VDD	I	Supply	--	Low power supply	3.1 V minimum or connected to VBATT
12	BOOT	I	CMOS/2X	Pull up	BOOT	Pull down through 1 kΩ for Flash downloading
13	ROW0	I/O	CMOS/1X	Output	Keyboard Row	
14	~RST	I/O	SCHMITT	--	Wireless CPU® Reset	Active low
15	ROW1	I/O	CMOS/1X	Output	Keyboard Row	

Pin #	Signal	I/O	I/O type	Reset State	Description	Comment
16	~INTR	I	CMOS	Pull up	External interrupt	Active low. 100 kΩ Pull-up inside
17	ROW2	I/O	CMOS/1X	Output	Keyboard Row	
18	GPI or CT103/TXD2	I	CMOS	Pull down	General purpose input or Aux serial Link (UART2)	100kΩ Pull down inside – Multiplexed
19	ROW3	I/O	CMOS/1X	Output	Keyboard Row	
20	GPO2 or CT104/RXD2	O	CMOS/3X	Output high	General purpose output or Aux serial Link (UART2)	Multiplexed
21	ROW4	I/O	CMOS/1X	Output	Keyboard Row	
22	GPO1	O	CMOX/3X	Output low	General purpose output	
23	COL0	I/O	CMOS/1X	Pull up	Keyboard Column	
24	GPIO0 or CT106/CTS2	I/O	CMOS/3X	High Z	General purpose I/O or Aux serial Link (UART2)	Multiplexed Pull up to VCC with 100 kΩ when not used
25	COL1	I/O	CMOS/1X	Pull up	Keyboard Column	
26	GPO0 or SPI_AUX	O	CMOS/3X	Output high	General purpose output or SPi Aux enable or SIM 3V/5V	Multiplexed
27	COL2	I/O	CMOS/1X	Pull up	Keyboard Column	
28	SPI_EN or GPO3	O	CMOS/3X	Output high	SPI main enable or General Purpose Output	Multiplexed
29	COL3	I/O	CMOS/1X	Pull up	Keyboard Column	
30	CT105/RTS1	I	CMOS/3X	High Z	Serial link interface Request To Send (UART1)	Pull up to VCC with 100 kΩ when not used
31	COL4	I/O	CMOS/1X	Pull up	Keyboard Column	
32	CT104/RXD1	O	CMOS/3X	Output high	Serial Link interface Receive (UART1)	
33	AUXV0	I	Analog	Pull up	Auxiliary ADC input 0	Can be tied to GND if not used
34	CT108-2/DTR1	I	CMOS	High Z	Serial link interface Data Terminal Ready (UART1)	Pull up to VCC with 100 kΩ when not used

Pin #	Signal	I/O	I/O type	Reset State	Description	Comment
35	GPIO5 or CT105/RTS2	I/O	CMOS/3X	High Z	General purpose I/O or Aux serial Link (UART2)	Multiplexed
36	CT107/DSR1	O	CMOS/3X	Output high	Serial Link interface Data Set Ready (UART1)	
37	CT106/CTS1	O	CMOS/3X	Output high	Serial Link interface Clear To Send (UART1)	
38	BAT_TEMP	I	Analog	High Z	ADC input for battery temperature measurement	Can be tied to GND if not used
39	CT103/TXD1	I	CMOS	High Z	Serial link interface Transmit (UART1)	Pull up to VCC with 100 kΩ when not used
40	VCC	O	Supply	--	2.8 V digital supply output	10 mA max.
41	SPK1P	O	Analog	High Z	Speaker 1 positive output	
42	MIC1P	I	Analog	High Z	Microphone 1 positive input	Not connected if not used
43	SPK1N	O	Analog	High Z	Speaker 1 negative output	
44	MIC1N	I	Analog	High Z	Microphone 1 negative input	Not connected if not used
45	SPK2P	O	Analog	High Z	Speaker 2 positive output	
46	MIC2P	I	Analog	High Z	Microphone 2 positive input	Not connected if not used
47	SPK2N	O	Analog	High Z	Speaker 2 negative output	
48	MIC2N	I	Analog	High Z	Microphone 2 negative input	Not connected if not used
49	BUZ	O	Analog	Open	Buzzer output	80 mA max
50	SIM_PRES	I	CMOS	High Z	SIM Card Detect	Can be tied to VCC if not used
51	CT109/DCD1	O	CMOS/2X	High Z	Serial Link interface Data Carrier Detect (UART1)	
52	FLASH LED	O	CMOS/2X	High Z	Wireless CPU® State	

Pin #	Signal	I/O	I/O type	Reset State	Description	Comment
53	GPIO4	I/O	CMOS/3X	Pull down	General purpose I/O	
54	CT125/RI1	O	CMOS/2X	High Z	Serial interface Ring Indicator (UART1)	
55	+VBATT		Supply	--	Battery Input	High current
56	VCC_RTC	I/O	Supply	--	RTC back-up supply	Not connected if not used
57	+VBATT		Supply	--	Battery Input	High current
58	+VBATT		Supply	--	Battery Input	High current
59	+VBATT		Supply	--	Battery Input	High current
60	+VBATT		Supply	--	Battery Input	High current

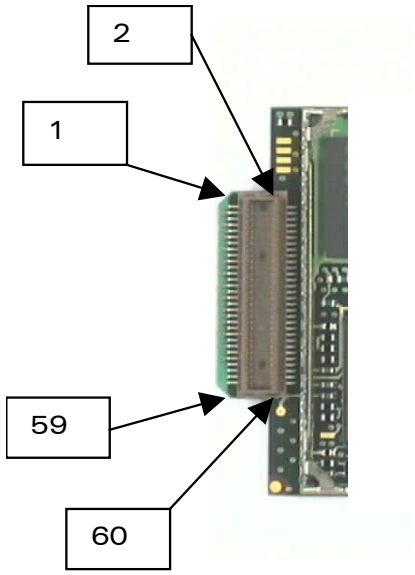


Figure 10: Wireless CPU® Quik Q2400 pin position (bottom view)

4.2 Environmental Specifications

Conditions	Temperature range
Operating / Full GSM specifications compliant	-20 °C to +55 °C
Storage	-30 °C to +85 °C

		ENVIRONMENTAL CLASSES		
TYPE OF TEST	STANDARDS	STORAGE Class 1.2	TRANSPORTATION Class 2.3	OPERATING (PORT USE) Class 7.3
Cold	IEC 68-2.1 Ab test	-25° C 72 h	-40° C 72 h	-20° C (GSM900) 16 h -10° C (GSM1800/1900) 16h
Dry heat	IEC 68-2.2 Bb test	+70° C 72 h	+70° C 72 h	+55° C 16 h
Change of temperature	IEC 68-2.14 Na/Nb test		-40° / +30° C 5 cycles t1 = 3 h	-20° / +30° C (GSM900) 3 cycles -10° / +30° C (GSM1800/1900): 3 cycles t1 = 3 h
Damp heat cyclic	IEC 68-2.30 Db test	+30° C 2 cycles 90% - 100% RH variant 1	+40° C 2 cycles 90% - 100% RH variant 1	+40° C 2 cycles 90% - 100% RH variant 1
Damp heat	IEC 68-2.56 Cb test	+30° C 4 days	+40° C 4 days	+40° C 4 days
Sinusoidal vibration	IEC 68-2.6 Fc test	5 - 62 Hz : 5 mm / s 62 - 200Hz : 2 m / s2 3 x 5 sweep cycles		
Random vibration wide band	IEC 68-3.36 Fdb test		5 - 20 Hz : 0.96 m2 / s3 20 - 500Hz : - 3 dB / oct 3 x 10 min	10 -12 Hz : 0.96 m2 / s3 12 - 150Hz : - 3 dB / oct 3 x 30 min

Electro-Static Discharge (ESD):

According to the norm **EN 61000-4-2**, the maximum ESD level supported by the Q2400 Wireless CPU® on contact discharges is ±1 kV on 60-pin connector and ±2 kV on the antenna connector.

Humidity:

According to **IPC/JEDEC J-STD-033**, the moisture class of the Q2400 Wireless CPU® series is **level 3**. The floor life from the opening of the sealed bag is 168 hours.

Reflow soldering:

The Wireless CPU® Quik Q2400 does not support any reflow soldering.

4.3 Mechanical Specifications

4.3.1 Physical Characteristics

The Wireless CPU® Quik Q2400 has a complete self-contained shield.

- Dimensions : 58.4 x 32.2 x 3.9 mm external dimensions (except shielding pins)
- Weight : <11 g

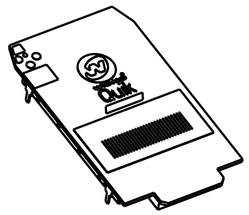
4.3.2 Mechanical Drawings

The following page gives the mechanical specifications of Wireless CPU® Quik Q2400.

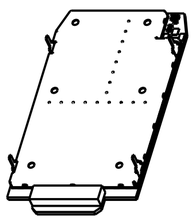
Figure 11: Mechanical drawing (see next page)

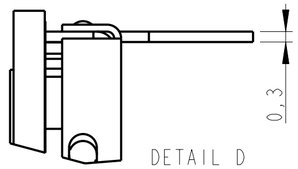
MAXIMUM BULK OCCUPIED ON THE MOTHER BOARD

SCALE 1,000

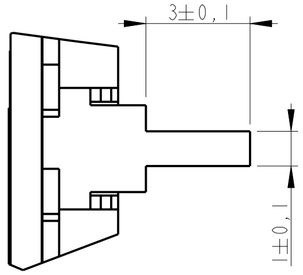


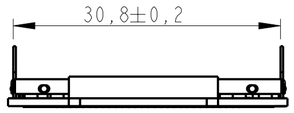
SCALE 1,000

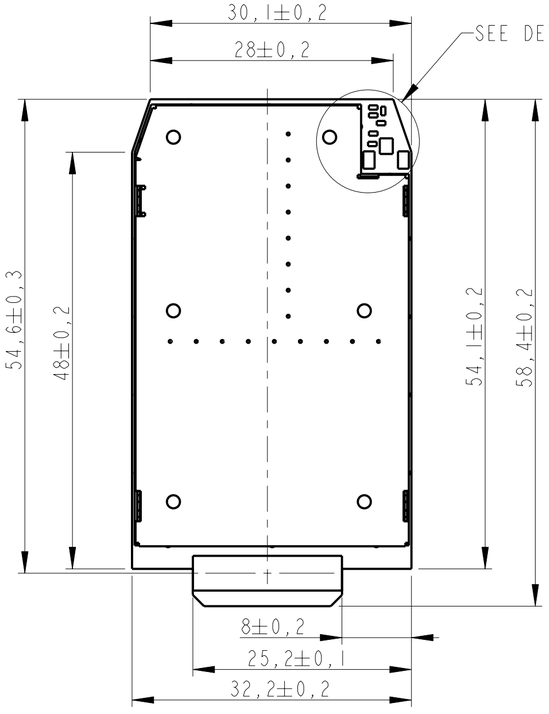


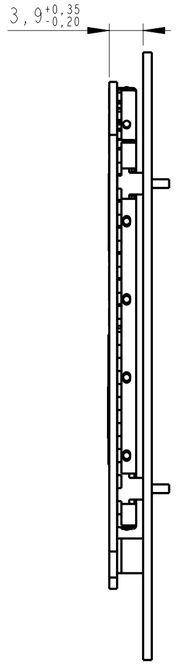


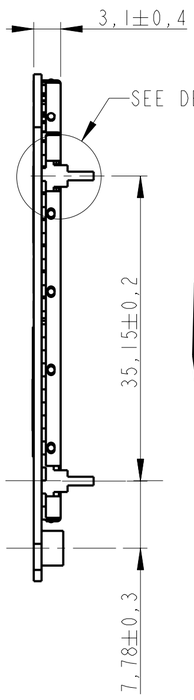
DETAIL D
SCALE 8,000

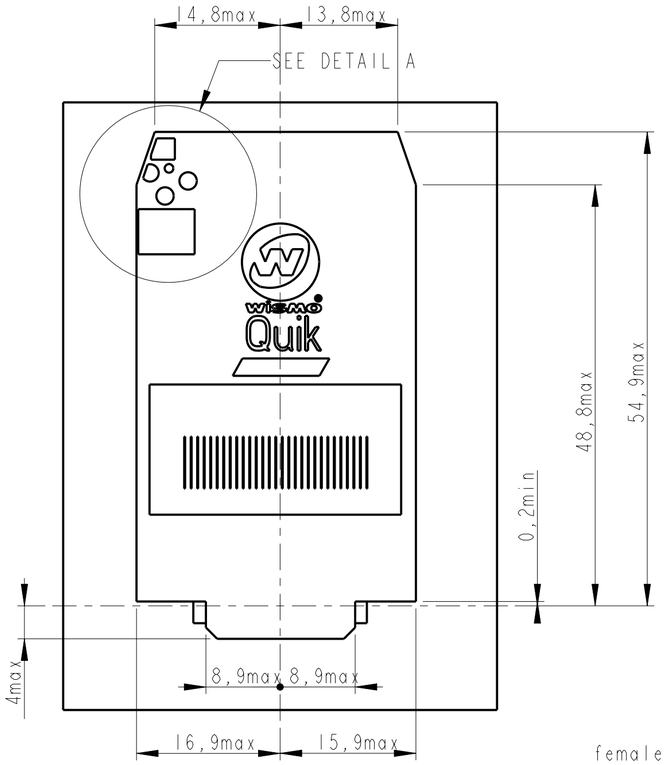


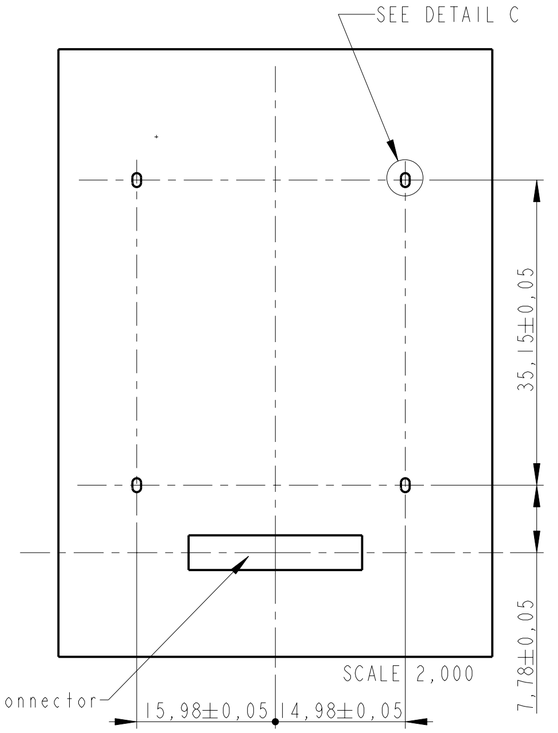


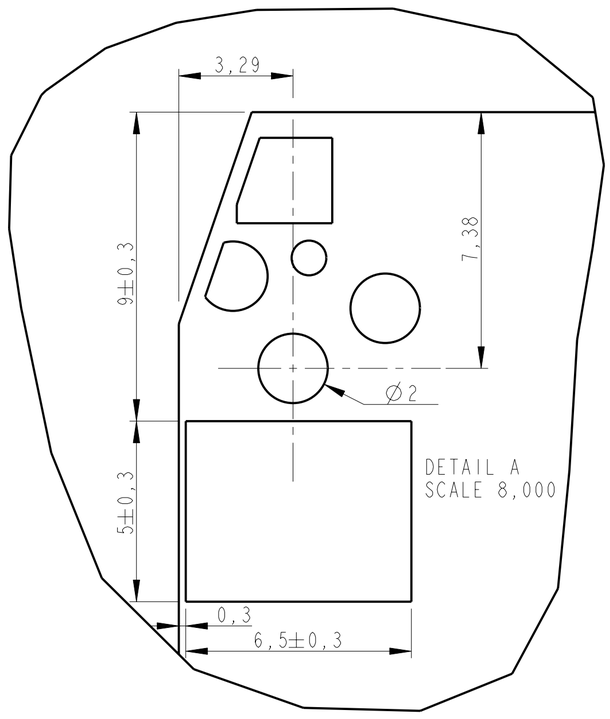




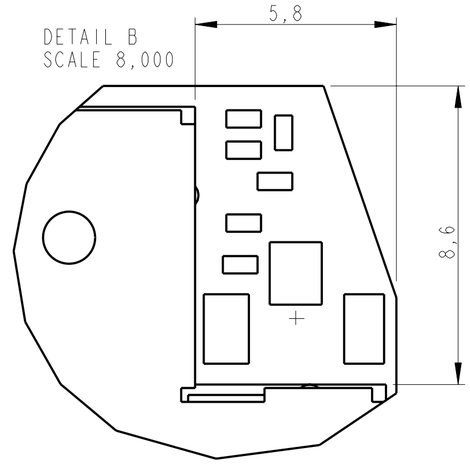


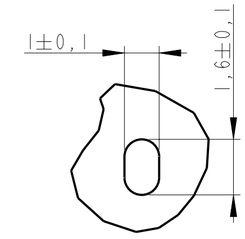






DETAIL B
SCALE 8,000





DETAIL C
SCALE 8,000

Dim modif.	04/02/05	JPM	MCH	Production	B
Creation	25/11/04	JPM	HER	Production	A
MODIFICATION	DATE	AUTHOR	RESP.	STATUS	IND

Wismo 2D10	GEN.TOL.: ±0,2	SCALE 2,000	
	FOLIO: 1/1	FORMAT : A2	
MODULE DIMENSIONS	WM-2-2171-V-001-A		
wavecom	AUTHOR : JPM		
	RESPONS. MCH		B
PRO/ENGINEER	WM2D10_DIMENSIONS		IND.

5 Appendix

5.1 Wavecom Acceptance Test

The Wireless CPU® Quik Q2400 complies with Wavecom standard acceptance test plan (Refer to document [11]).

5.2 GSM Standard and Recommendations

The Wireless CPU® Quik Q2400 is compliant with the following GSM ETSI, 3GPP and GCF and recommendations for Phase II.

Specification Reference	Title
3GPP TS 45.005 v5.5.0 (2002-08) Release 5	Technical Specification Group GSM/EDGE. Radio Access Network; Radio transmission and reception
GSM 02.07 V8.0.0 (1999-07)	Digital cellular telecommunications system (Phase 2+); Mobile Stations (MS) features (GSM 02.07 version 8.0.0 Release 1999)
3GPP TS 03.22 V8.7.0 (2002-08)	Technical Specification Group GSM/EDGE. Radio Access Network; Functions related to Mobile Station (MS) in idle mode and group receive mode; (Release 1999)
3GPP TS 03.40 V7.5.0 (2001-12)	Technical Specification Group Terminals; Technical realization of the Short Message Service (SMS) (Release 1998)
3GPP TS 03.41 V7.4.0 (2000-09)	Technical Specification Group Terminals; Technical realization of Cell Broadcast Service (CBS) (Release 1998)
ETSI EN 300 903 V8.1.1 (2000-11)	Digital cellular telecommunications system (Phase 2+); Transmission planning aspects of the speech service in the GSM Public Land Mobile Network (PLMN) system (GSM 03.50 version 8.1.1 Release 1999)

Specification Reference	Title
3GPP TS 04.06 V8.2.1 (2002-05)	Technical Specification Group GSM/EDGE Radio Access Network; Mobile Station - Base Station System (MS - BSS) interface; Data Link (DL) layer specification (Release 1999)
3GPP TS 04.08 V7.18.0 (2002-09)	Technical Specification Group Core Network; Digital cellular telecommunications system (Phase 2+); Mobile radio interface layer 3 specification (Release 1998)
3GPP TS 04.10 V7.1.0 (2001-12)	Technical Specification Group Core Networks; Mobile radio interface layer 3 Supplementary services specification; General aspects (Release 1998)
3GPP TS 04.11 V7.1.0 (2000-09)	Technical Specification Group Core Network; Digital cellular telecommunications system (Phase 2+); Point-to-Point (PP) Short Message Service (SMS) support on mobile radio interface (Release 1998)
3GPP TS 45.005 v5.5.0 (2002-08)	Technical Specification Group GSM/EDGE. Radio Access Network; Radio transmission and reception (Release 5)
3GPP TS 45.008 V5.8.0 (2002-08)	Technical Specification Group GSM/EDGE Radio Access Network; Radio subsystem link control (Release 5)
3GPP TS 45.010 V5.1.0 (2002-08)	Technical Specification Group GSM/EDGE Radio Access Network; Radio subsystem synchronization (Release 5)
3GPP TS 46.010 V5.0.0 (2002-06)	Technical Specification Group Services and System Aspects; Full rate speech; Transcoding (Release 5)
3GPP TS 46.011 V5.0.0 (2002-06)	Technical Specification Group Services and System Aspects; Full rate speech; Substitution and muting of lost frames for full rate speech channels (Release 5)
3GPP TS 46.012 V5.0.0 (2002-06)	Technical Specification Group Services and System Aspects; Full rate speech; Comfort noise aspect for full rate speech traffic channels (Release 5)
3GPP TS 46.031 V5.0.0 (2002-06)	Technical Specification Group Services and System Aspects; Full rate speech; Discontinuous Transmission (DTX) for full rate speech traffic channels (Release 5)

Specification Reference	Title
3GPP TS 46.032 V5.0.0 (2002-06)	Technical Specification Group Services and System Aspects; Full rate speech; Voice Activity Detector (VAD) for full rate speech traffic channels (Release 5)
TS 100 913V8.0.0 (1999-08)	Digital cellular telecommunications system (Phase 2+); General on Terminal Adaptation Functions (TAF) for Mobile Stations (MS) (GSM 07.01 version 8.0.0 Release 1999)
GSM 09.07 V8.0.0 (1999-08)	Digital cellular telecommunications system (Phase 2+); General requirements on interworking between the Public Land Mobile Network (PLMN) and the Integrated Services Digital Network (ISDN) or Public Switched Telephone Network (PSTN) (GSM 09.07 version 8.0.0 Release 1999)
3GPP TS 51.010-1 v5.0.0 (2002-09)	Technical Specification Group GSM/EDGE ; Radio Access Network ;Digital cellular telecommunications system (Phase 2+);Mobile Station (MS) conformance specification; Part 1: Conformance specification (Release 5)
3GPP TS 51.011 V5.0.0 (2001-12)	Technical Specification Group Terminals; Specification of the Subscriber Identity Module - Mobile Equipment (SIM - ME) interface (Release 5)
ETS 300 641 (1998-03)	Digital cellular telecommunications system (Phase 2); Specification of the 3 volt Subscriber Identity Module - Mobile Equipment (SIM-ME) interface (GSM 11.12 version 4.3.1)
GCF-CC V3.13 (2004-01)	Global Certification Forum – Certification criteria

5.3 Safety Recommendations (for information only)

IMPORTANT

FOR THE EFFICIENT AND SAFE OPERATION OF

YOUR GSM APPLICATION BASED ON Wireless CPU® Quik Q2400 Series

PLEASE READ THIS INFORMATION CAREFULLY

5.3.1 RF Safety

5.3.1.1 General

Your GSM terminal[2] is based on the GSM standard for cellular technology. The GSM standard is spread all over the world. It covers Europe, Asia and some parts of America and Africa. This is the most used telecommunication standard.

Your GSM terminal is actually a low power radio transmitter and receiver. It sends out as well as receives radio frequency energy. When you use your GSM application, the cellular system which handles your calls controls both the radio frequency and the power level of your cellular modem.

5.3.1.2 Exposure to RF Energy

There has been some public concern on possible health effects of using GSM terminals. Although research on health effects from RF energy has focused on the current RF technology for many years, scientists have begun research regarding newer radio technologies, such as GSM.

After existing research had been reviewed, and after compliance to all applicable safety standards had been tested, it has been concluded that the product was fitted for use.

If you are concerned about exposure to RF energy there are things you can do to minimize exposure. Obviously, limiting the duration of your calls will reduce your exposure to RF energy. In addition, you can reduce RF exposure by operating your cellular terminal efficiently by following the below guidelines.

5.3.1.3 Efficient Terminal Operation

For your GSM terminal to operate at the lowest power level, consistent with satisfactory call quality:

- If your terminal has an extendible antenna, extend it fully. Some models allow you to place a call with the antenna retracted. However your GSM terminal operates more efficiently with the antenna when it is fully extended
- Do not hold the antenna when the terminal is « IN USE ». Holding the antenna affects call quality and may cause the modem to operate at a higher power level than needed

[2] based on Q2400

5.3.1.4 Antenna Care and Replacement

Do not use the GSM terminal with a damaged antenna. If a damaged antenna comes into contact with the skin, a minor burn may result. Replace the damaged antenna immediately. You may repair antenna to yourself by following the instructions provided to you.. If so, use only a manufacturer-approved antenna. Otherwise, have your antenna repaired by a qualified technician.

Buy or replace the antenna only from the approved suppliers list. Using of unauthorized antennas, modifications or attachments could damage the terminal and may violate local RF emission regulations or invalidate type approval.

5.3.2 General Safety

5.3.2.1 Driving

Check with the laws and the regulations regarding the use of cellular devices in the area where you have to drive as you always have to comply with them. When using your GSM terminal while driving, please:

- give full attention to driving,
- pull-off from the road and park before making or answering a call if driving conditions so require.

5.3.2.2 Electronic Devices

Most electronic equipment, for example in hospitals and motor vehicles are shielded from RF energy. However, RF energy may affect some improperly shielded electronic equipment.

5.3.2.3 Vehicle Electronic Equipment

Check with your vehicle manufacturer/representative to determine if any on-board electronic equipment is adequately shielded from RF energy.

5.3.2.4 Medical Electronic Equipment

Consult the manufacturer of any personal medical devices (such as pacemakers, hearing aids, etc) to determine if they are adequately shielded from external RF energy.

Turn your terminal **OFF** in health care facilities when any regulations posted in the area instruct you to do so. Hospitals or health care facilities may be using RF monitoring equipment.

5.3.2.5 Aircraft

Turn your terminal OFF before boarding any aircraft.

Use it on the ground only with crew permission.

Do not use it in the air.

To prevent possible interference with aircraft systems, Federal Aviation Administration (FAA) regulations require you should have prior permission from a crew member to use your terminal while the aircraft is on the ground. In order to prevent interference with cellular systems, local RF regulations prohibit using your modem while airborne.

5.3.2.6 Children

Do not allow children to play with your GSM terminal. It is not a toy. Children could hurt themselves or others (by poking themselves or others in the eye with the antenna, for example). Children could damage the modem, or make calls that increase your modem bills.

5.3.2.7 Blasting Areas

To avoid interfering with blasting operations, turn your unit OFF when you are in a « blasting area » or in areas posted: « turn off two-way radio ». Construction crew often uses remote control RF devices to set off explosives.

5.3.2.8 Potentially Explosive Atmospheres

Turn your terminal **OFF** when in any area with a potentially explosive atmosphere. Though it is rare, but your modem or its accessories could generate sparks. Sparks in such areas could cause an explosion or fire resulting in bodily injuries or even death.

Areas with a potentially explosive atmosphere are often, but not always, clearly marked. They include fuelling areas such as petrol stations; below decks on boats; fuel or chemical transfer or storage facilities; and areas where the air contains chemicals or particles, such as grain, dust, or metal powders.

Do not transport or store flammable gas, liquid, or explosives, in the compartment of your vehicle which contains your terminal or accessories.

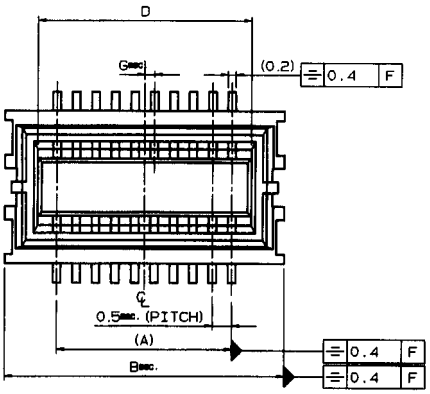
Before using your terminal in a vehicle powered by liquefied petroleum gas (such as propane or butane) ensure that the vehicle complies with the relevant fire and safety regulations of the country in which the vehicle is used.

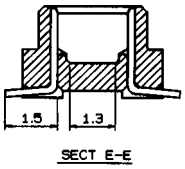
5.4 General Purpose Connector Data Sheet

The following 6 pages are the KYOCERA/ELCO data sheets for the GPC (also available from http://www.avxcorp.com .

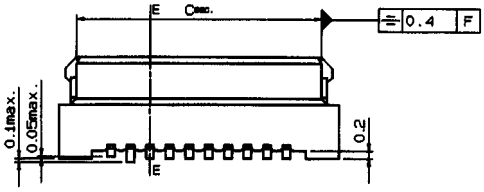
0,5 mm Spacing SERIES 5087

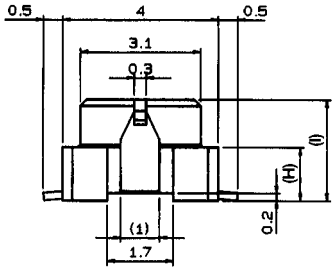
Surface Mount Vertical Plug

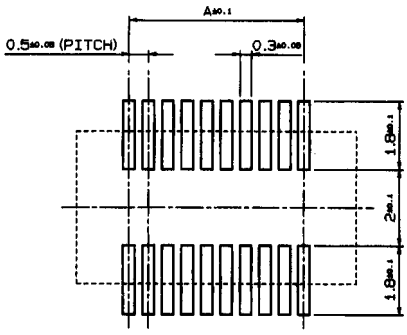




Specifications:
- 1000 per Tape and Reel
- Voltage - 50 V
- Current Rating - 0.4 A
- Dielectric Withstanding Voltage - 500 V
- Operating Temperature - (-25°C ~ +85°C)
- Contact Material - phosphor bronze
- Insulator Material - PPS (UL 94 V-0)







MOUNTING LAYOUT

No. of Pos.	P/N	A	B	C	D	G
20	10 5087 020 XX0 861	4.5/.177	7.2/.283	6.2/.244	5.5/.217	0.25/.0098
30	10 5087 030 XX0 861	7.0/.276	9.7/.382	8.7/.343	8.0/.315	0.50/.0196
36	10 5087 036 XX0 861	8.5/.335	11.2/.441	10.2/.402	9.5/.374	0.25/.0098
40	10 5087 040 XX0 861	9.5/.374	12.2/.480	11.2/.441	10.5/.414	0.25/.0098
50	10 5087 050 XX0 861	12.0/.472	14.7/.579	13.7/.539	13.0/.512	0.50/.0196
60	10 5087 060 XX0 861	14.5/.571	17.2/.677	16.2/.638	15.5/.610	0.25/.0098

Dimensions millimeters/inches

ORDERING CODE

Typical Example	14	5087	0XX	2XX	861

14: PLUG - Tape and Reel

NUMBER OF CONTACTS:

40, 60 : 3.0mm Stack
36, 40, 50 : 3.5mm Stack
20, 30, 36, 50, 60 : 4.0mm Stack

2: Without Adhesive Tape
9: Adhesive Cover Tape

VARIATION CODE:

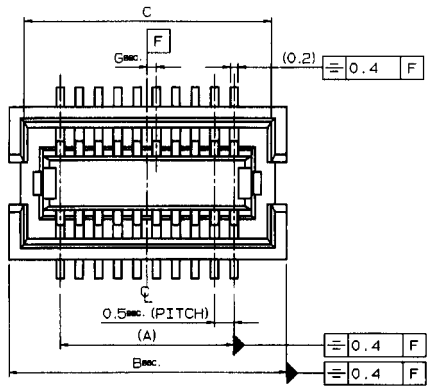
	H	I
30	.9	2.15
35	1.4	2.7
40	1.9	3.2

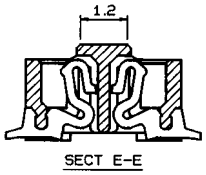
PLATING VARIATION:

861: 15 microinches of gold with gold flash tails

Consult factory for other sizes

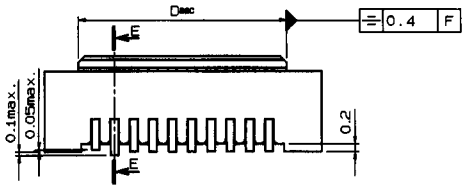
0,5 mm Spacing SERIES 5087

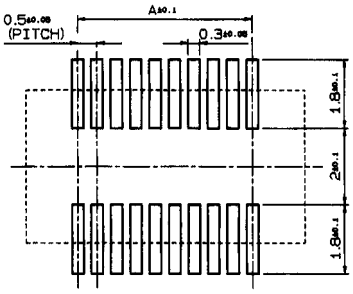




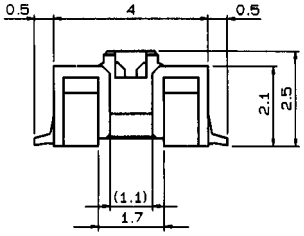
Surface Mount Vertical Receptacle

Specifications:
- 1000 per Tape and Reel
- Voltage - 50 V
- Current Rating - 0.4 A
- Dielectric Withstanding Voltage - 500 V
- Operating Temperature - (-25°C ~ +85°C)
- Contact Material - phosphor bronze
- Insulator Material - PPS (UL 94 V-0)





MOUNTING LAYOUT



No. of Pos.	P/N	A	B	C	D	G
20	20 5087 020 x00 861	4.5/.177	7.2/.283	6.4/.252	5.4/.213	0.25/.0098
30	20 5087 030 x00 861	7.0/.276	9.7/.382	8.9/.350	7.9/.311	0.50/.0196
36	20 5087 036 x00 861	8.5/.335	11.2/.441	10.4/.409	9.4/.370	0.25/.0098
40	20 5087 040 x00 861	9.5/.374	12.2/.480	11.4/.449	10.4/.409	0.25/.0098
50	20 5087 050 x00 861	12.0/.472	14.7/.579	13.9/.547	12.9/.508	0.50/.0196
60	20 5087 060 x00 861	14.5/.570	17.2/.677	16.4/.646	15.4/.606	0.25/.0098

Dimensions millimeters/inches

ORDERING CODE

Typical Example	24	5087	0XX	200	861

24: Receptacle - Tape and Reel

NUMBER OF CONTACTS:
20, 30, 36, 40, 50, 60

2: Without Adhesive Tape
9: Adhesive Cover Tape

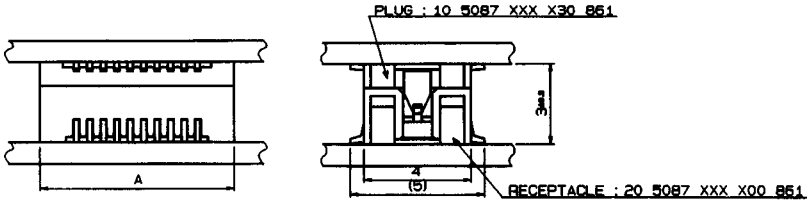
PLATING VARIATION:
861: 15 microinches of gold with gold flash tails

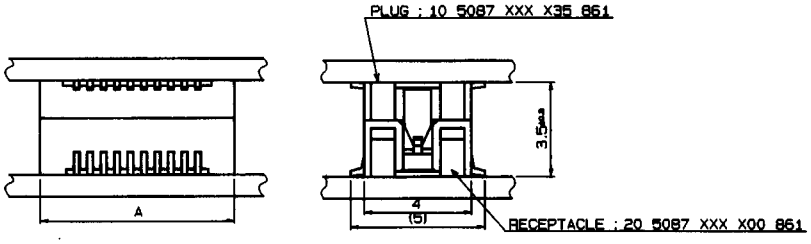
Consult factory for other sizes

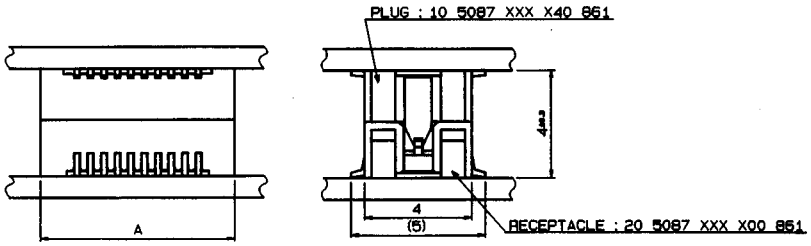
0,5 mm Spacing Applications

	P/N	Stacking Height
PLUG	10 5087 xxx x30 861	3.0
RECE.	20 5087 xxx x00 861	
PLUG	10 5087 xxx x35 861	3.5
RECE.	20 5087 xxx x00 861	
PLUG	10 5087 xxx x40 861	4.0
RECE.	20 5087 xxx x00 861	

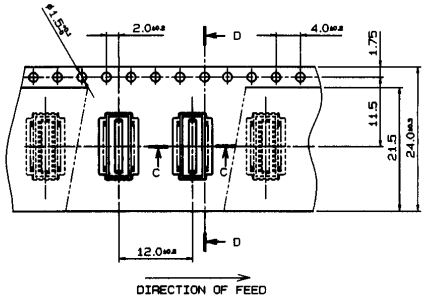
No. of Pos.	A
20	7.2/.283
30	9.7/.382
36	11.2/.441
40	12.2/.480
50	14.7/.579
60	17.2/.677

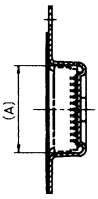


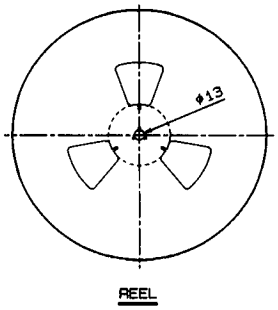


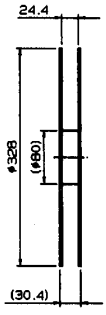


0,5 mm Spacing Tape and Reel



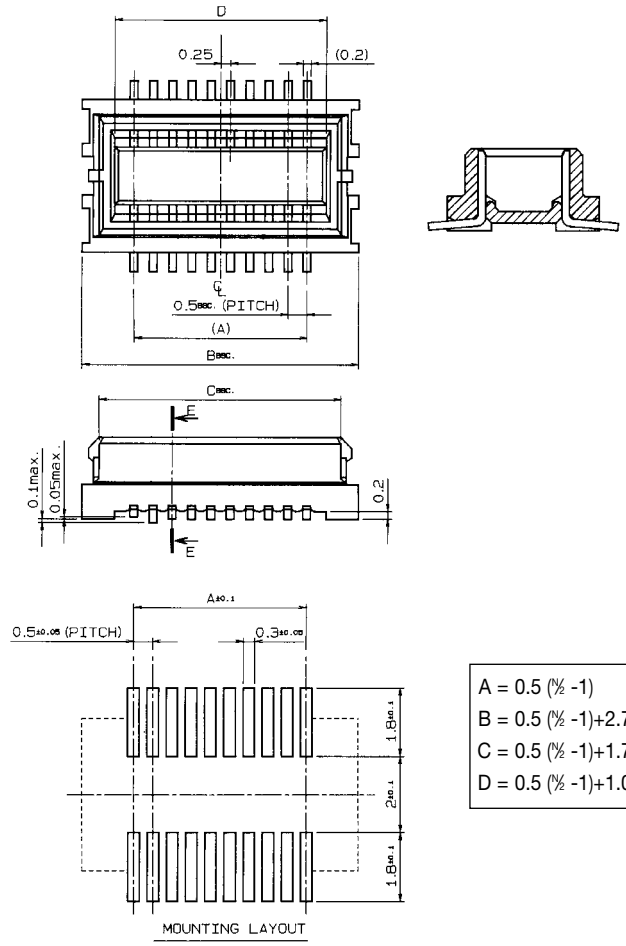






Super Micro Connectors 0.5mm Pitch

Series 5087 Plug



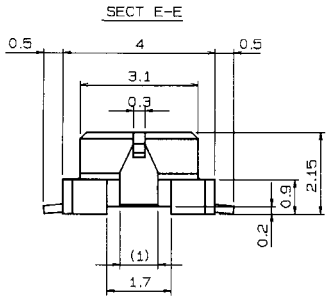
A = 0.5 (N -1)
B = 0.5 (N -1)+2.7
C = 0.5 (N -1)+1.7
D = 0.5 (N -1)+1.0

ORDERING CODE

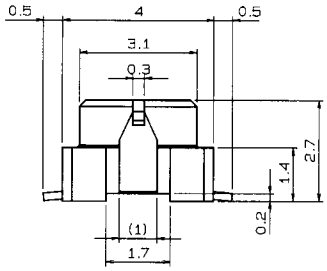
14 5087 0XX X XX 8XX

- FINISH
  - 861 = Ni Under Coated 1.25µm min. Gold-Mating Area Au 0.38µm min.
  - 829 = Ni Under Coated 1.25µm min. Gold-Mating Area Au 0.1µm min.
- VARIATION
  - 30 : H = 3.0mm
  - 35 : H = 3.5mm
  - 40 : H = 4.0mm
- TYPE 0 = without Boss with Retention Clip
  - 2 = without Boss, Retention Clip
  - 9 = without Boss, Retention Clip, with Adhesive Tape
- NUMBER OF POSITIONS (20, 30, 32, 36, 40, 50, 60)
- SERIES
- TAPE AND REEL
  - 14 = Plug

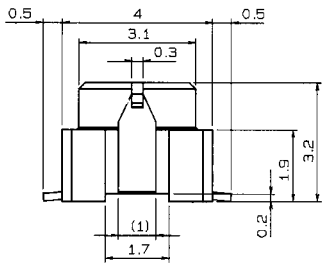
H = 3.0mm Type



H = 3.5mm Type

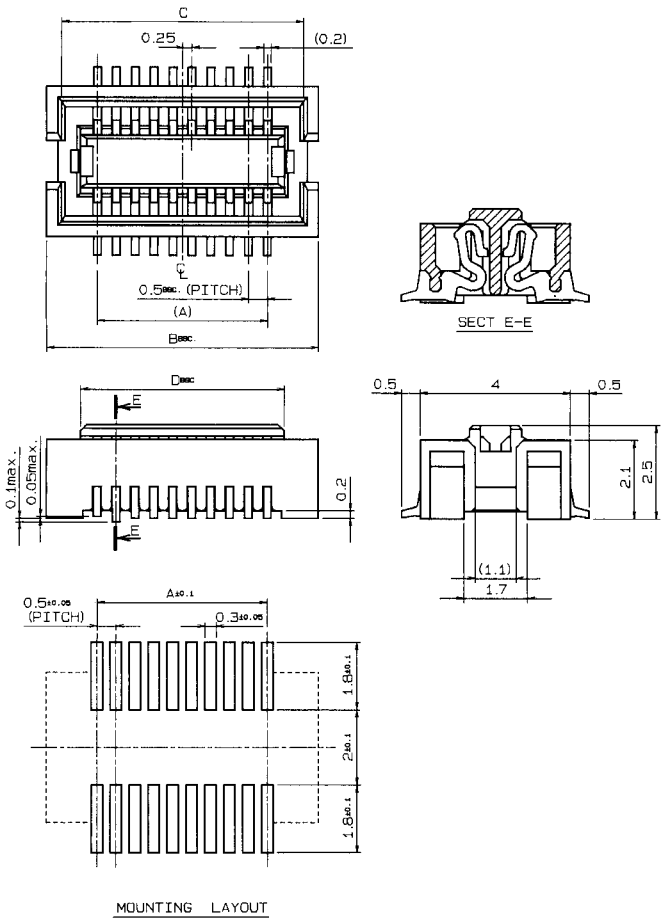


H = 4.0mm Type



Super Micro Connectors 0.5mm Pitch

Series 5087 Receptacle H = 3.0 ~ 4.0mm Type



ORDERING CODE

24 5087 0XX X 00 8XX

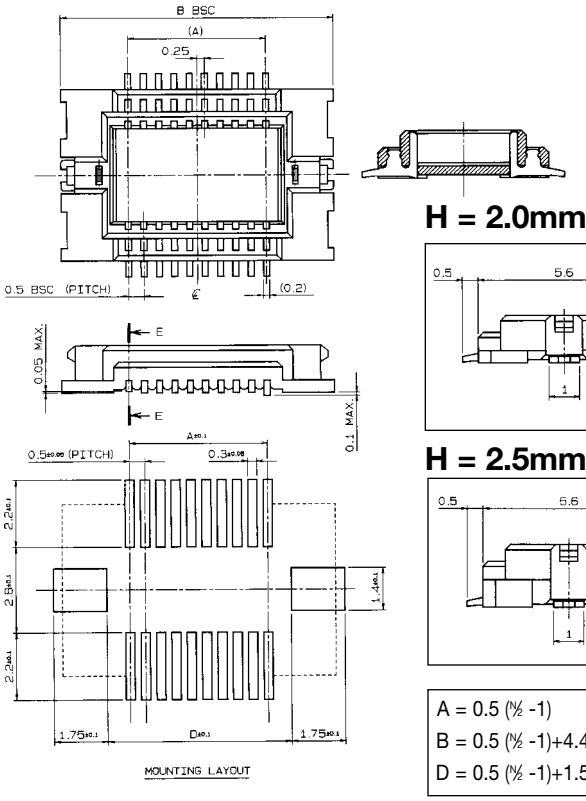
- **24** — TAPE AND REEL
  24 = Receptacle
- **5087** — SERIES
- **0XX** — NUMBER OF POSITIONS
  (20, 30, 32, 36, 40, 50, 60)
- **X** — TYPE
  0 = without Boss with Retention Clip
  2 = without Boss, Retention Clip
  9 = without Boss, Retention Clip, with Adhesive Tape
- **00** — VARIATION
  H = 3.0 ~ 4.0mm
- **8XX** — FINISH
  861 = Ni Under Coated 1.25µm min. Gold-Mating Area Au 0.38µm min.
  829 = Ni Under Coated 1.25µm min. Gold-Mating Area Au 0.1µm min.

A = 0.5 (½ -1)
B = A +2.7
C = A +1.9
D = A +0.9

Additional information on this product is available from AVX's catalog or AVX's FAX Service.
Call 1-800-879-1613 and request document **#270**. Visit our website http://www.avxcorp.com

Super Micro Connectors 0.5mm Pitch

Series 5087 Plug



H = 2.0mm Type

H = 2.5mm Type

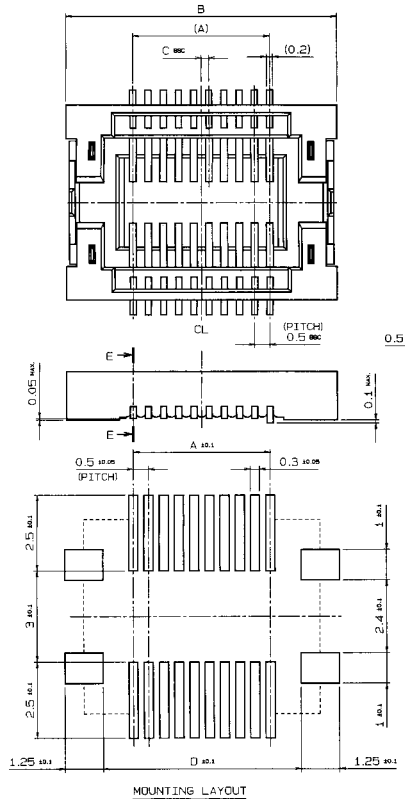
A = 0.5 (N -1)
B = 0.5 (N -1)+4.4
D = 0.5 (N -1)+1.5

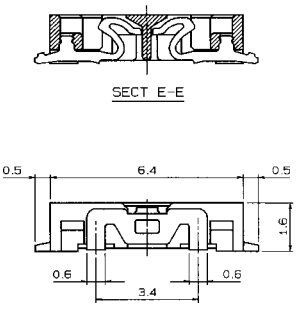
ORDERING CODE

14 5087 0XX X XX 8XX

- FINISH
  - 861 = Ni Under Coated 1.25µm min. Gold-Mating Area Au 0.38µm min.
  - 829 = Ni Under Coated 1.25µm min. Gold-Mating Area Au 0.1µm min.
- VARIATION
  - 20 : H = 2.0mm
  - 25 : H = 2.5mm
- TYPE 0 = without Boss with Retention Clip
  - 2 = without Boss, Retention Clip
  - 9 = without Boss, Retention Clip, with Adhesive Tape
- NUMBER OF POSITIONS (10*, 20, 30, 40, 50, 60) *2.0mm H only
- SERIES
- TAPE AND REEL
  - 14 = Plug

Series 5087 Receptacle H = 2.0 ~ 2.5mm Type



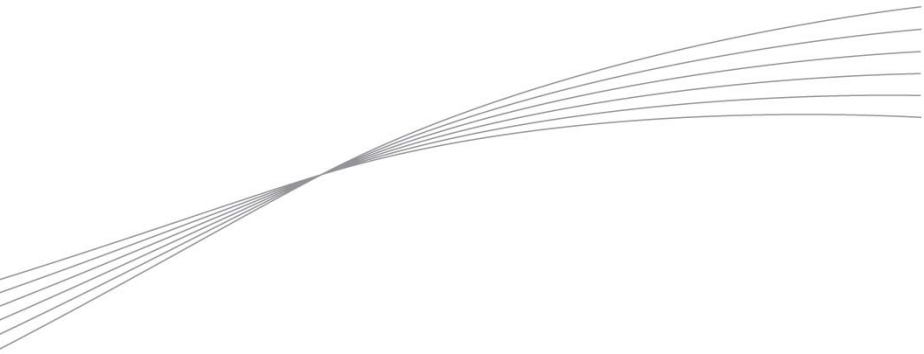


ORDERING CODE

24 5087 0XX X 01 8XX

- FINISH
  - 861 = Ni Under Coated 1.25µm min. Gold-Mating Area Au 0.38µm min.
  - 829 = Ni Under Coated 1.25µm min. Gold-Mating Area Au 0.1µm min.
- VARIATION
  - H = 2.0 ~ 2.5mm
- TYPE 0 = without Boss with Retention Clip
  - 2 = without Boss, Retention Clip
  - 9 = without Boss, Retention Clip, with Adhesive Tape
- NUMBER OF POSITIONS (10, 20, 30, 40, 50, 60)
- SERIES
- TAPE AND REEL
  - 24 = Receptacle

Additional information on this product is available from AVX's catalog or AVX's FAX Service. Call 1-800-879-1613 and request document **#271.** Visit our website http://www.avxcorp.com



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WAVECOM S.A. - 3 esplanade du Foncet - 92442 Issy-les-Moulineaux Cedex - France - Tel: +33(0)1 46 29 08 00 - Fax: +33(0)1 46 29 08 08
Wavecom, Inc. - 4810 Eastgate Mall - Second Floor - San Diego, CA 92121 - USA - Tel: +1 858 362 0101 - Fax: +1 858 558 5485
WAVECOM Asia Pacific Ltd. - Unit 201-207, 2nd Floor, Bio-Informatics Centre – No.2 Science Park West Avenue - Hong Kong Science Park, Shatin - New Territories, Hong Kong