



# MC5728V Important Signal Considerations

## Application Note



# Preface

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## Revision history

Version	Date	Summary of changes
1.0	Jan10	Initial release.
2	Aug12	New template. Changes to the patents section.

## About This Guide

This document describes important signal considerations regarding MDL\_RESET\_N and W\_DISABLE# signals of the MC5728V MiniCard module, and also USB enumeration and power-up timing.

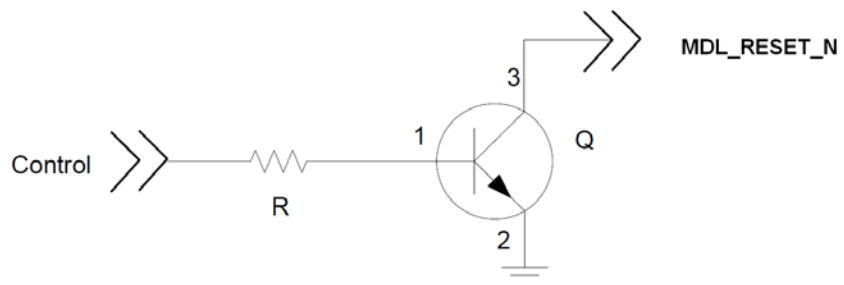
## MDL\_RESET\_N — Module reset input

The MDL\_RESET\_N signal (pin 33) is an input to the MC5728V module from the host device to initiate a reset of the module.

When integrating with your host device, keep the following in mind.

- This signal is an input to the module and should be driven LOW only for its active state (RESET); otherwise it should be floating or (High impedance). It should never be driven to a logic high level. At module power-up, the Baseband processor holds this signal LOW for a pre-determined time; the host must not interfere with this sequence (by attempting to drive the signal HIGH). If the host does not comply with this, unwanted behavior and an unknown state of the module may occur.
- If the host never needs to assert a reset to the MC5728V module, leave this signal unconnected from the host interface. Figure 1 shows good design practice for connecting the MDL\_RESET\_N signal. This allows for open collector output when not being asserted by the host device.

Figure 1: Recommended MDL\_RESET\_N connection



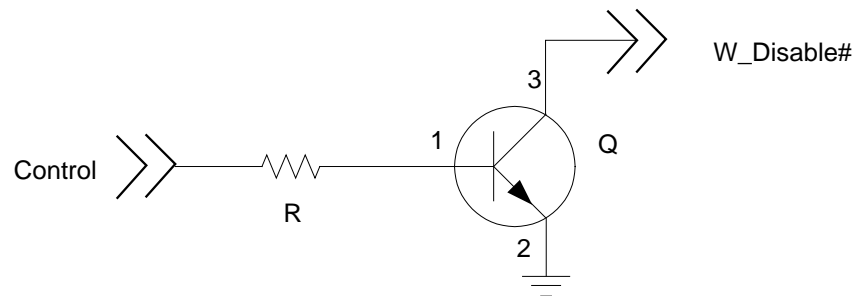
## W\_DISABLE# — Wireless disable

The W\_DISABLE# signal (pin 20) is an input to the module from the host device to control the Power state (power on and shutdown of the MC5728V module, depending on the state of the signal).

When integrating with your host device, keep the following in mind.

- This signal is an input to the module and should be driven LOW only for its active state (controlling the power state); otherwise it should be floating or (High impedance). It should never be driven to a logic high level. The MC5728V module has an internal pull-up resistor to Module Power (3.3V) in place, so if the signal is floating or (high impedance), the module will power on.
- If the host never needs to assert this power state control to the MC5728V module, leave this signal unconnected from the host interface. Figure 2 shows good design practice for connecting the W\_DISABLE# signal. This allows for open collector output when not being asserted by the host device.

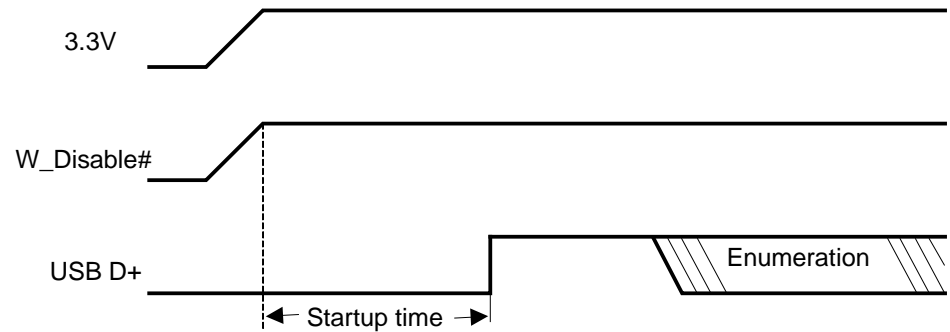
Figure 2: Recommended W\_DISABLE# connection



# USB enumeration and power-up timing

The unit is ready to enumerate with a USB host within a maximum of 5.1 seconds after power-up.

Figure 3: Power-up timing diagram



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*Note: Startup time is the time after power-up when the modem is ready to begin the enumeration sequence.*

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