Product Technical Specification & Customer Design Guidelines

AirPrime Q26 Extreme

SIERRA WIRELESS

WM_DEV_Q26EX_PTS_002
007
March 01, 2011

Important Notice

Due to the nature of wireless communications, transmission and reception of data can never be guaranteed. Data may be delayed, corrupted (i.e., have errors) or be totally lost. Although significant delays or losses of data are rare when wireless devices such as the Sierra Wireless modem are used in a normal manner with a well-constructed network, the Sierra Wireless modem should not be used in situations where failure to transmit or receive data could result in damage of any kind to the user or any other party, including but not limited to personal injury, death, or loss of property. Sierra Wireless accepts no responsibility for damages of any kind resulting from delays or errors in data transmitted or received using the Sierra Wireless modem, or for failure of the Sierra Wireless modem to transmit or receive such data.

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Consult our website for up-to-date product descriptions, documentation, application notes, firmware upgrades, troubleshooting tips, and press releases: www.sierrawireless.com

Document History

Version	Date	Updates
001	December 22, 2008	Creation
002	March 18, 2009	Update power consumption figures add thermal design rules
003	June 05, 2009	Update for Vbatt range, thermal foam and temperature behavior
004	August 4, 2009	Reformatted in Sierra Wireless style. Updated UART1 tolerance information as follows: The UART1 interface is 2.8 volts type. Moreover, it is 3.3 volts tolerant. Updated the Standards and Recommendations section.
005	September 16, 2009	Updated Antenna gain of 4.6dBi and additional information in this paragraph of the Standards Recommendations section. Updated CT104-RXD1 to be MUXed with GPIO37.
006	December 3, 2009	Standards and Recommendations section: • Updated FCC notice by adding to the last sentence of one paragraph regarding FCC multi-transmitter information, deleted the following one sentence regarding compliance, and fixed the values in the following sentence to 4.6dBi (850MHz) and 3.4 dBi (1900MHz). Interfaces section: • Updated 3V/1V8 UICC/SIM interface bullet • Updated USIM/SIM card bullet USIM/SIM Interface section • Added "Using the USIM is recommended over the SIM card" sentence
007	March 01, 2011	Reformatted in the rebranded SWI template.
		Updated section 3.21.2.1 Super Capacitor
		Added a note in section 3.10 General Purpose Input/Output, specifying which GPIO is associated with AT+WTBI.
		Deleted the last bullet point in section 3.16.1.2 Additional Notes based on Tracker 01626.
		Added note for entering Sleep Mode in section 3.2.2.1 Power Consumption without the Sierra Wireless Software SuiteOpen AT Processing.
		Removed the second bullet point from 3.8.1.2 For Use with 4-wire Serial Interface (UART2 does not have DTR2).
		Updated Figure 16 Example of Full Modem V24/CMOS Serial Link Implementation for UART1.
		Updated chip reference from ADM3307AECP to ADM3307EACP.

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1. Introduction

1.1. Overview

This document presents and defines the Q26 Extreme embedded module.

The Q26 Extreme embedded module is a multi-mode EDGE 2G / WCDMA 3G / HSxPA (High Speed Downlink & High Speed Uplink Packet Access) solution with dual antenna receive diversity and footprint compatible with other Q26 embedded module devices.

The Q26 Extreme embedded module supports the Sierra Wireless Software Suite, the world's most comprehensive cellular development environment which allows embedded standard ANSI C applications to be natively executed directly on the embedded module.

This product specification document covers the embedded module alone and does not include the programmable capabilities provided via the use of the Sierra Wireless Software Suite.

1.2. References

1.2.1. Reference Documents

For more details, several reference documents can be consulted. The Sierra Wireless documents referenced herein are provided in the Sierra Wireless documentation package; however, the general reference documents which are not Sierra Wireless owned are not provided in the documentation package.

Please check the web site for the latest documentation available.

The first software version available for the Q26 Extreme embedded module is Sierra Wireless Software Suite 2.30.

1.2.1.1. Sierra Wireless Software Documents

[1] Getting Started with SDK 2.33

Reference: WM_DEV_OAT_UGD_048

[2] Basic Development Guide for SDK 2.33 (if using IDE; obsolete if using Developer Studio)

Reference: WM_DEV_OAT_UGD_050

[3] ADL User Guide for SDK 2.33 (if using IDE; obsolete if using Developer Studio)

Reference: WM_DEV_OAT_UGD_051

[4] SDK 2.33 Official Release Note

Reference: WM_DEV_OAT_DVD_338

1.2.1.2. Firmware Documents

[5] Firmware 7.4 AT Commands Manual
Reference: WM_DEV_OAT_UGD_079

[6] Firmware 7.1 Official Release Note
Reference: WM_DEV_OAT_CRN_013

1.2.1.3. General Reference Documents

[7] "I^2C Bus Specification and user guide", Version 3.0, NXP 2007

[8] ISO 7816-3 Standard

1.2.2. List of Abbreviations

Table 1. Abbreviations

Abbreviation	Definition
AC	Alternating Current
ADC	Analog to Digital Converter
A/D	Analog to Digital conversion
AF	Audio-Frequency
AT	ATtention (prefix for modem commands)
AUX	AUXiliary
CAN	Controller Area Network
CB	Cell Broadcast
CEP	Circular Error Probable
CLK	CLocK
CMOS	Complementary Metal Oxide Semiconductor
CS	Coding Scheme
CTS	Clear To Send
DAC	Digital to Analog Converter
dB	Decibel
DC	Direct Current
DCD	Data Carrier Detect
DCE	Data Communication Equipment
DCS	Digital Cellular System
DR	Dynamic Range
DSR	Data Set Ready
DTE	Data Terminal Equipment
DTR	Data Terminal Ready
EDGE	Enhanced Data rates for GSM Evolution
EFR	Enhanced Full Rate
EGPRS	Enhanced General Packet Radio Service
E-GSM	Extended GSM

Abbreviation	Definition
EMC	ElectroMagnetic Compatibility
EMI	ElectroMagnetic Interference
EMS	Enhanced Message Service
EN	ENable
ESD	ElectroStatic Discharges
FIFO	First In First Out
FR	Full Rate
FTA	Full Type Approval
GND	GrouND
GPI	General Purpose Input
GPC	General Purpose Connector
GPIO	General Purpose Input Output
GPO	General Purpose Output
GPRS	General Packet Radio Service
GPS	Global Positioning System
GSM	Global System for Mobile communications
HR	Half Rate
HSDPA	High Speed Downlink Packet Access
HSUPA	High Speed Uplink Packet Access
HSxPA	High Speed x(downlink/uplink) Packet Access
I/O	Input / Output
LED	Light Emitting Diode
LNA	Low Noise Amplifier
MAX	MAXimum
MIC	MICrophone
MIN	MINimum
MMS	Multimedia Message Service
MO	Mobile Originated
MT	Mobile Terminated
na	Not Applicable
NF	Noise Factor
NMEA	National Marine Electronics Association
NOM	NOMinal
NTC	Negative Temperature Coefficient
PA	Power Amplifier
Pa	Pascal (for speaker sound pressure measurements)
PBCCH	Packet Broadcast Control CHannel
PC	Personal Computer
PCB	Printed Circuit Board
PCM	Pulse Code Modulation (audio) or Protection Circuit Module (battery)
PDA	Personal Digital Assistant
PFM	Power Frequency Modulation
PSM	Phase Shift Modulation

Abbreviation	Definition
PWM	Pulse Width Modulation
RAM	Random Access Memory
RF	Radio Frequency
RFI	Radio Frequency Interference
RHCP	Right Hand Circular Polarization
RI	Ring Indicator
RST	ReSeT
RTC	Real Time Clock
RTCM	Radio Technical Commission for Maritime services
RTS	Request To Send
RX	Receive
SCL	Serial CLock
SDA	Serial DAta
SMS	Short Message Service
SPI	Serial Peripheral Interface
SPL	Sound Pressure Level
SPK	SPeaKer
SRAM	Static Random Access Memory
TBC	To Be Confirmed
TDMA	Time Division Multiple Access
TP	Test Point
TVS	Transient Voltage Suppressor
TX	Transmit
TYP	TYPical
UART	Universal Asynchronous Receiver-Transmitter
UMTS	Universal Mobile Telecommunications System
USB	Universal Serial Bus
USIM	Universal Subscriber Identification Module
USSD	Unstructured Supplementary Services Data
VSWR	Voltage Standing Wave Ratio
WCDMA	Wideband Code Division Multiple Access

1.3. Web Site Support

Table 2. Web Site Support Links

Subject Matter	Web Site
General information about Sierra Wireless and its range of products:	http://www.sierrawireless.com/
Specific support about the Q26 Extreme embedded module:	http://www.sierrawireless.com/productsandservices/AirPrime/Embedded_Modules/Q_Series/Q26_Extreme.aspx
Carrier/Operator approvals:	http://www.sierrawireless.com/Support/Downloads/AirPrime/Q_Series/AirPrime_Q26_Extreme.aspx

Subject Matter	Web Site
Sierra Wireless Software Suite Introduction:	http://www.sierrawireless.com/en/productsandservices/AirPrime/Sierra_Wireless_Software_Suite.aspx
Developer support for software and hardware:	http://forum.sierrawireless.com/

2. General Description

2.1. General Information

The Q26 Extreme embedded module is a self-contained GSM/GPRS/EGDE quad-band and HSxPA tri band embedded module with the following characteristics:

2.1.1. Overall Dimensions

- Dimension:
  - Length: 40 mm
  - Width: 32.2 mm
  - Thickness: 6.3 mm
- X/Y form-factor compatible with the Q2686/87 embedded module range

2.1.2. Approvals & Quality

- EU Directive 2002/95/EC on RoHS
  - The Q26 Extreme embedded module is compliant with RoHS (Restriction of Hazardous Substances in Electrical and Electronic Equipment) Directive 2002/95/EC which sets limits for the use of certain restricted hazardous substances.
  - This directive states that "from 1st July 2006, new electrical and electronic equipment put on the market does not contain lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB), and polybrominated diphenyl ethers (PBDE)".
- Regulatory: R&TTE directive (CE marking), GCF-CC, PTCRB, FCC/IC.
- Manufacturing: ISO/TS 16949

2.1.3. Telecom Features

- 3GPP FDD Release 6 HSUPA Compliant.
- Tri-Band UMTS/HxDPA (WCDMA/FDD) 2100/1900/850 MHz (band I, II, V)
  - Downlink data rates up to HSDPA Category 8 (7.2 Mbps).
  - Uplink data rates up to HSUPA Category 5 (2 Mbps)
  - Advanced Type III receiver technology supporting simultaneous Receive Diversity and Equalization.
- Quad-Band GSM GPRS EDGE 850/900/1800/1900 MHz
  - GPRS class 12
  - EDGE (E-GPRS) multi-slot class 12
- Dual mode with fully automated handover between 2G and 3G networks
- Voice: HR, FR and EFR; Adaptive multi-rate AMR in GSM & UMTS.

2.1.4. Interfaces

- Digital section running under 2.8 volts and 1.8 volts
- 3V/1V8 UICC/SIM interface
- Complete interfacing:
  - Power supply
  - Serial link
  - Analog audio
  - Parallel bus 16bits
  - PCM digital audio
  - USIM/SIM card
  - Keyboard
  - USB 2.0 slave FS
  - Serial LCD (not available with AT commands)

2.1.5. Application Processor

The application processor embeds the Sierra Wireless Software Suite with an extensive set of Plug-Ins, supported by Developer Studio, enabling the creation of natively executed code in C and/or Lua script.

- Up to 88 MIPS for application execution
- Includes a low latency, multitasking pre-emptive Operating System

2.1.6. Connectivity

The Q26 Extreme embedded module has the following external connections:

- Two solutions for the main RF antenna connection
  - UFL connector
  - Soldered connection
- Diversity RF antenna connection
  - Soldered connection
- Analog and digital interfaces
  - 100 pin I/O connector

2.2. Functional Architecture

The global architecture of the Q26 Extreme embedded module is described below:

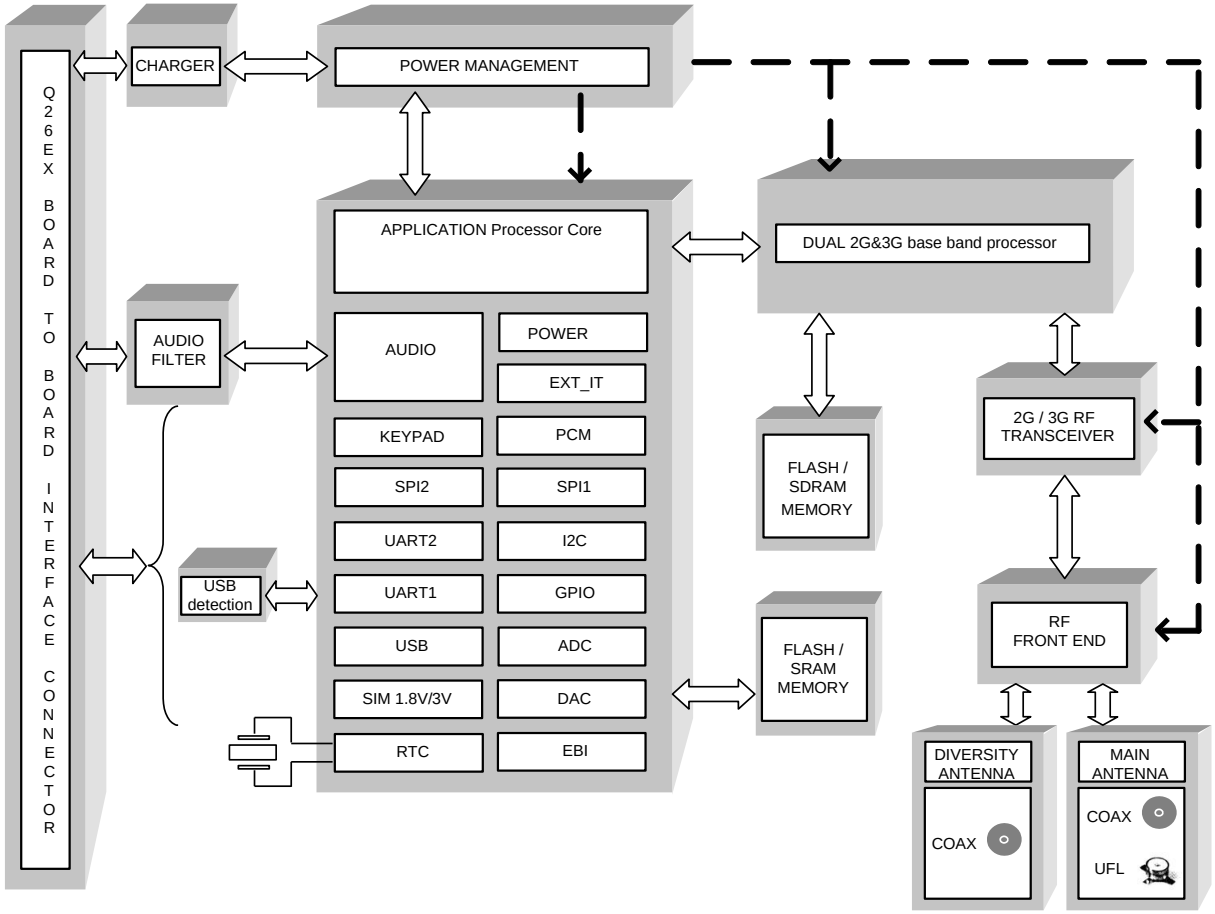


Figure 1. Functional Architecture

2.2.1. RF Functionalities

The Radio Frequency (RF) range complies with the Phase II EGSM 900/DCS 1800 and GSM 850/PCS 1900 recommendations. The frequencies are:

Table 3. RF Frequency Ranges

RF Bandwidth	Transmit Band (Tx)	Receive Band (Rx)
GSM 850	824 to 849 MHz	869 to 894 MHz
E-GSM 900	880 to 915 MHz	925 to 960 MHz
DCS 1800	1710 to 1785 MHz	1805 to 1880 MHz
PSC 1900	1850 to 1910 MHz	1930 to 1990 MHz
WCDMA Band I	1920 to 1980 MHz	2110 to 2170 MHz
WCDMA Band II	1850 to 1910 MHz	1930 to 1990 MHz
WCDMA Band V	824 to 849 MHz	869 to 894 MHz

The Radio Frequency (RF) part is based on a specific quad-band chip with a:

- Direct down conversion Rx architecture
- Linear direct up-conversion Tx architecture
- On chip Tx power control
- Analog I/Q base band interface for all modes
- Integrated Σ-Δ fractional N synthesizer for dual-mode operation
- On chip multi-band true Rx diversity

2.2.2. Application Processor

The Q26 Extreme supports the complete family of software Plug-Ins provided within the Sierra Wireless Software Suite (TCP-IP, Internet, GPS, Lua, Security, Bluetooth, aqLink™). It also supports VariPower & VariSpeed (26-104MHz) features allowing highly configurable power optimization:

- ARM946 32 bit processor
- Programmable to 104MHz operation
- Internal Memory (8kbyte Cache I$, 8kbyte D$)
- Latency time: < 1ms
- Memory access speed up to 52MHz
- 2 user Timers at 13MHz fine tuning (1 for customer)
- 3 External IT with debouncing

2.3. Operating System

The Q26 Extreme Embedded Module is Sierra Wireless Software Suite compliant. With the Sierra Wireless Software Suite, customers can embed their own applications with the Q26 Extreme embedded module and turn the Q26 Extreme embedded module into a solution for their specific market need.

The operating system allows for the Q26 Extreme Embedded Module to be controlled by AT commands. However, some interfaces in the Q26 Extreme module may still not be available even with AT command control as these interfaces are dependent on the peripheral devices connected to the Q26 Extreme embedded module.

3. Interfaces

3.1. General Purpose Connector

A 100-pin connector is provided to interface the Q26 Extreme embedded module with a board containing a serial LCD module, a keyboard, a USIM connector, or a battery connection.

The available interfaces on the GPC are described below.

Table 4. Available GPC Interfaces

Name	Driven by AT Commands	Driven by Open AT
Serial Interface		✓
Keyboard Interface	✓	✓
Main Serial Link	✓	✓
Auxiliary Serial Link	✓	✓
USIM Interface	✓	✓
General Purpose IO	✓	✓
Analog to Digital Converter	✓	✓
Analog Audio Interface	✓	✓
Buzzer Output	✓	✓
Battery Charging Interface	✓	✓
External Interruption	✓	✓
VCC_2V8 and VCC_1V8		
BAT-RTC (Backup Battery)		
LED0 signal	✓	✓
Digital Audio Interface (PCM)		✓
USB 2.0 Interface	✓	✓

3.2. Power Supply

3.2.1. Power Supply Description and Ground Plane

3.2.1.1. Electrical Constraints

Only the VBATT input is necessary to supply the Q26 Extreme embedded module.

1. Operational average current

   Recommended value for the operational average max current = 1.1A.

2. Peak max current

   Recommended value for peak max current = 2.1A.

   The rising time is around 10µs.

   See subsection 7 Details for worst case description.

3. Ground

   The Q26 Extreme embedded module shielding case is the grounding. The ground must be connected to the motherboard through a complete layer on the PCB.

Table 5. Input Power Supply Voltage

	V_{MIN}	V_{NOM}	V_{MAX}
VBATT[1,2]	3.4V	3.8V	4.2V

1 This value must be guaranteed during the burst (with 2.1A Peak in GSM or GPRS mode)

2 Max operating Voltage Stationary Wave Ratio (VSWR) 2:1

4. Impedance

   When the embedded module is supplied with a battery, the total impedance (battery + protections + PCB) should be < 150mΩ.

5. Recommendations when using DC/DC converter

   As the radio power amplifier is directly connected to VBATT, the embedded module is sensitive to any Alternative Current on lines. When a DC/DC converter is used, Sierra Wireless recommends setting the converter frequency in such a way that the resulting voltage does not exceed the values in following table.

Table 6. Maximum Voltage Ripple (U_{ripp}) vs. Frequency

Frequency (Hz)	U_{ripp} Max (mVpp)
f ≤ 300	80
300 < f ≤ 800	10
800 < f ≤ 1100	30
f > 1100	60

6. Constraints in Alarm/Off mode

   When the embedded module is in Alarm/Off mode, no voltage has to be applied on any pin of the 100-pin connector, except on Vbatt (pins 1 to 4), BAT-RTC (pin 7) for RTC operation or ON/~OFF (pin 19) to power-ON the embedded module.

7. Details

   Due to the burst emission mode used in GSM/GPRS/EGPRS, the power supply must be able to deliver high current peaks in a short time. During the peaks, the ripple (U_{ripp}) on the supply voltage must not exceed a certain limit).

   - In communication mode, a GSM/GPRS class 2 terminal emits 577µs radio bursts every 4.615ms.

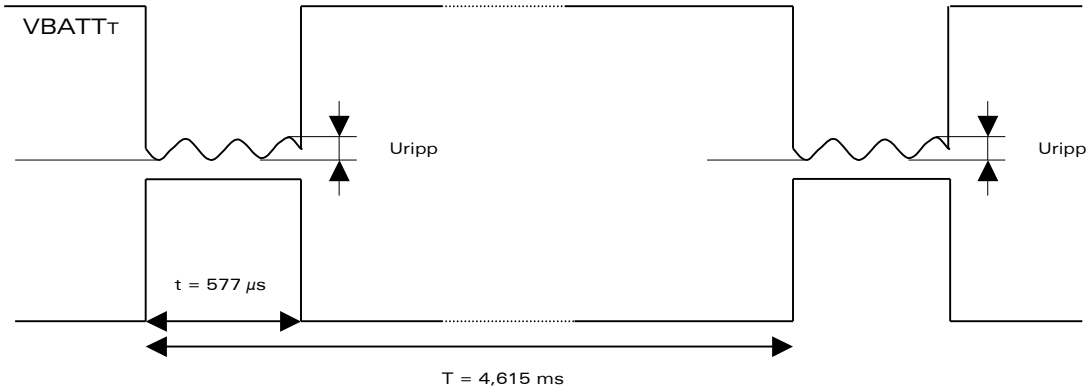


Figure 2. Power Supply During GSM Burst Emission

   - Directly supplies the RF components with 3.8V. It is essential to keep a minimum voltage ripple at this connection in order to avoid any phase error.

   The RF Power Amplifier current (**2.1A** max peak in GSM /GPRS mode) flows with a ratio of:

   - 1/8 of the time (577µs every 4.615ms for GSM /GPRS cl. 2)
   - 2/8 of the time (1154µs every 4.615ms for GSM /GPRS cl. 10)
   - 4/8 of the time (2302µs every 4.615ms for GSM /GPRS cl. 12)

   The rising time is around 10µs.

3.2.1.2. Design Requirements

Attention should be paid:

- to the quality of the power supply:
  - linear regulation (recommended) or PWM (Pulse Width Modulation) converter (usable) are preferred for low noise.
  - PFM (Power Frequency Modulation) or PSM (Phase Shift Modulation) system must be avoided.
- to the capacity to deliver high current peaks in a short time (burst radio emission).
- that the VBATT line supports peak currents with an acceptable voltage drop which guarantees a VBATT minimal value of 3.4V.

For PCB design constraints related to power supply tracks, ground planes and shielding, refer to section 6 Design Guidelines.

3.2.1.3. Decoupling of Power Supply Signals

Decoupling capacitors on VBATT lines are embedded in the Q26 Extreme embedded module. Hence, it should not be necessary to add decoupling capacitors close to the embedded module.

However, in case of EMI/RFI problems, the VBATT signal may require some EMI/RFI decoupling – parallel 33pF capacitor close to the embedded module or a serial ferrite bead (or both to get better results). Low frequency decoupling capacitors (22µF to 100µF) may be used to reduce TDMA noise (217Hz).

Caution: *When ferrite beads are used, the recommendation given for the power supply connection must be followed with care (as high current capacity and low impedance).*

3.2.2. Power Consumption

Power consumption is dependent on the configuration used. It is for this reason that the following consumption values are given for each mode, RF band and type of software used (AT or Open AT®).

All the following information are given assuming a 50Ω RF output.

The following consumption values were obtained by performing measurements on embedded module samples at a temperature of 25°C.

Three VBATT values are used to measure the consumption, VBATTmin (3.4V), VBATTmax (4.2V) and VBATTtyp (3.8V).

The average current is given for the three VBATT values and the peak current given is the maximum current peak measured with the three VBATT voltages.

For a more detailed description of the operating modes, see the appendix of document [5] Firmware v7.4 AT Commands Manual.

3.2.2.1. Power Consumption without the Sierra Wireless Software Suite

The following measurement results are relevant when there is no Sierra Wireless Software Suite application.

For an explanation of the power consumption modes, please refer to document [5] Firmware v7.4 AT Commands Manual.

Table 7. Power Consumption without the Sierra Wireless Software Suite

Operating Mode	Parameters	I_{NOM} Average; VBATT= 3.8V			Unit
		Min	Typ	Max	
ALARM Mode			16		µA
SLEEP Mode			1.4		mA
ACTIVE Mode			24.5		mA
SLEEP mode with telecom stack in Idle Mode [1]	Case 2G (Paging 9/Rx burst occurrence ~2s)		3.1		mA
	Case 2G (Paging 2/Rx burst occurrence ~0,5s)		6.4		mA
	Case WCDMA (Paging 9)		2		mA
ACTIVE mode with	Case 2G (Paging 9/Rx burst		28.6		mA

Operating Mode	Parameters	I_{NOM} Average; VBATT= 3.8V			Unit
		Min	Typ	Max	
telecom stack in Idle Mode [1]	occurrence ~2s)				
	Case 2G (Paging 2/Rx burst occurrence ~0,5s)		32.8		mA
	Case WCDMA (Paging 9)		27.6		mA
Peak current in GSM/GPRS Mode	850/900 MHz - PCL5/gam.3 (TX power 33dBm)			2.1	A
	1800/1900 MHz - PCL0/gam.3 (TX power 30dBm)			1.7	A
GSM Connected Mode (Voice)	850/900 MHz - PCL5 (TX power 33dBm)		470		mA
	850/900 MHz - PCL19 (TX power 5dBm)		300		mA
	1800/1900 MHz - PCL0 (TX power 30dBm)		420		mA
	1800/1900 MHz - PCL15 (TX power 0dBm)		290		mA
GPRS Transfer Mode class 8 (4Rx/1Tx)	850/900 MHz - gam. 3(TX power 33dBm)		455		mA
	1800/1900 MHz - gam.3(TX power 30dBm)		415		mA
GPRS Transfer Mode class 10 (3Rx/2Tx)	850/900 MHz - gam.3 (TX power 30dBm)		570		mA
	1800/1900 MHz - gam.3 (TX power 27dBm)		500		mA
GPRS Transfer Mode class 12 (1Rx/4Tx)	850/900 MHz - gam.3 (TX power 27dBm)		720		mA
	1800/1900 MHz - gam.3 (TX power 24dBm)		620		mA
EGPRS Transfer Mode class 8 (4Rx/1Tx)	850/900 MHz - gam.6 (TX power 27dBm)		385		mA
	1800/1900 MHz - gam.5 (TX power 26dBm)		380		mA
EGPRS Transfer Mode class 10 (3Rx/2Tx)	850/900 MHz - gam.6 (TX power 24dBm)		480		mA
	1800/1900 MHz - gam.5 (TX power 23dBm)		460		mA
EGPRS Transfer Mode class 12 (1Rx/4Tx)	850/900 MHz - gam.6 (TX power 21dBm)		640		mA
	1800/1900 MHz - gam.5 (TX power 20dBm)		600		mA
UMTS Connected Mode (Voice)	BAND I @ +22 dBm		780	810	mA
	BAND I @ +10 dBm		570		mA
	BAND II @ +22 dBm		821	920	mA
	BAND II @ +10 dBm		570		mA
	BAND V @ +22 dBm		780	825	mA
	BAND V @ +10 dBm		535		mA
UMTS Data Transfer2	BAND I @ +22 dBm		855	885	mA

Operating Mode	Parameters	I_{NOM} Average; VBATT= 3.8V			Unit
		Min	Typ	Max	
384kbits/s	BAND I @ +10 dBm		645		mA
	BAND II @ +22 dBm		860	930	mA
	BAND II @ +10 dBm		635		mA
	BAND V @ +22 dBm		825	870	mA
	BAND V @ +10 dBm		550		mA
HSDPA Data Transfer2 Cat. 8 7.2Mbits/s	BAND I @ +22 dBm		915	945	mA
	BAND I @ +10 dBm		720		mA
	BAND II @ +22 dBm		935	1050	mA
	BAND II @ +10 dBm		720		mA
	BAND V @ +22 dBm		875	920	mA
	BAND V @ +10 dBm		625		mA
HSUPA Data Transfer2 Cat. 5 2Mbist/s	BAND I @ +22 dBm		890	920	mA
	BAND I @ +10 dBm		705		mA
	BAND II @ +22 dBm		920	990	mA
	BAND II @ +10 dBm		710		mA
	BAND V @ +22 dBm		875	920	mA
	BAND V @ +10 dBm		625		mA

TX means that the current peak is the RF transmission burst (Tx burst)

RX means that the current peak is the RF reception burst (Rx burst)

1 This mode consumption is dependent on the USIM card used. Some USIM cards respond faster than others; the longer the response time, the higher the consumption. The measurements were performed with a large number of 3V USIM cards.

Note: The USB port must be deactivated to enter Sleep Mode.

3.2.2.2. Power Consumption with the Sierra Wireless Software Suite

The activation of the software could increase the power consumption up to 60mA in ACTIVE mode and CONNECTED when the full CPU load is used by the Sierra Wireless Software Suite application.

3.2.2.3. Power Supply Pin-Out

Table 8. Power Supply Pin-Out

Signal	Pin Number
VBATT	1, 2, 3, 4
GND	Shielding

Caution: *The grounding connection is made through the shielding ⇨ the four leads must be soldered to the ground plane.*

3.3. Electrical Information for Digital I/O

The three types of digital I/O on the Q26 Extreme embedded module are: 2.8Volt CMOS, 1.8Volt CMOS and Open drain.

The three types are described below:

Table 9. 2.8 Volts Type (2V8)

Parameter		I/O Type	Minimum	Typical	Maximum	Condition
Internal 2.8V power supply		VCC_2V8	2.74V	2.8V	2.86V	
Input / Output pin	V_{IL}	CMOS	-0.5V*		0.84V	
	V_{IH}	CMOS	1.96V		3.2V*	
	V_{OL}	CMOS			0.4V	I_{OL} = - 4 mA
	V_{OH}	CMOS	2.4V			I_{OH} = 4 mA
	I_{OH}				4mA	
	I_{OL}				- 4mA	

* Absolute maximum ratings

All 2.8V I/O pins do not accept input signal voltage above the maximum voltage specified above, except for the UART1 interface, which is 3.3V tolerant.

Table 10. 1.8 Volts Type (1V8)

Parameter		I/O Type	Minimum	Typical	Maximum	Condition
Internal 1V8 power supply		VCC_1V8	1.76V	1.8V	1.94V	
Input / Output pin	V_{IL}	CMOS	-0.5V*		0.54V	
	V_{IH}	CMOS	1.33V		2.2V*	
	V_{OL}	CMOS			0.4V	I_{OL} = - 4 mA
	V_{OH}	CMOS	1.4V			I_{OH} = 4 mA
	I_{OH}				4mA	
	I_{OL}				- 4mA	

* Absolute maximum ratings

Table 11. Open Drain Output Type

Signal Name	Parameter	I/O Type	Minimum	Typical	Maximum	Condition
LED0	V_{OL}	Open Drain			0.4V	
	I_{OL}	Open Drain			8mA	
BUZZER0	V_{OL}	Open Drain			0.4V	
	I_{OL}	Open Drain			100mA	
SDA1/ GPIO27 and SCL1/	V_{TOL}	Open Drain			3.3V	Tolerated voltage
	V_{IH}	Open Drain	2V			

Signal Name	Parameter	I/O Type	Minimum	Typical	Maximum	Condition
GPIO26	V_{IL}	Open Drain			0.8V	
	V_{OL}	Open Drain			0.4V	
	I_{OL}	Open Drain			3mA	

The reset states of the I/Os are given in each interface description chapter. Definitions of these states are given below:

Table 12. Reset State Definition

Parameter	Definition
0	Set to GND
1	Set to supply 1V8 or 2V8 depending on I/O type
Pull-down	Internal pull-down with ~60kΩ resistor.
Pull-up	Internal pull-up with ~60kΩ resistor to supply 1V8 or 2V8 depending on I/O type.
Z	High impedance
Undefined	**Caution:** *Undefined must not be used in your application if a special state is required at reset. These pins may be toggling a signal during reset.*

3.4. Serial Interface

The Q26 Extreme embedded module provides two SPI bus (i.e. for LCDs, memories, etc.) and an I^2C 2-wire interface.

3.4.1. SPI Bus

Both SPI bus interfaces include:

- A CLK signal
- An I/O signal
- An I signal
- A CS (Chip Select) signal complying with the standard SPI bus (any GPIO)
- An optional Load signal (only the SPIx-LOAD signal)

3.4.1.1. Characteristics

- Master mode operation
- The CS signal must be any GPIO
- The LOAD signal (optional) is used for the word handling mode (only the SPIx-LOAD signal)
- SPI speed is from 102 kbit/s to 13 Mbit/s in master mode operation
- 3 or 4-wire interface(5-wire possible with the optional SPIx-LOAD signal)
- SPI-mode configuration: 0 to 3
- 1 to 16 bits data length

3.4.1.2. SPI Configuration

Table 13. SPI Configuration

Operation	Maximum Speed	SPI-Mode	Duplex	3-wire Type	4-wire Type	5-wire Type
Master	13 Mb/s	0, 1, 2, 3	Half	SPIx-CLK; SPIx-IO; GPIOx as CS	SPIx-CLK; SPIx-IO; SPIx-I; GPIOx as CS	SPIx-CLK; SPIx-IO; SPIx-I; GPIOx as CS; SPIx-LOAD (not muxed in GPIO);

For the 3-wire configuration, SPIx-I/O is used as input and output.

For the 4-wire configuration, SPIx-I/O is used as output only, SPIx-I is used as input only.

For the 5-wire configuration, SPIx-I/O is used as output only, SPIx-I is used as input only. And the dedicated SPIx-LOAD signal is used. It is an additional signal in more than a Chip Select (any other GPIOx).

3.4.1.3. SPI Waveforms

Waveforms for SPI transfer with 4-wire configuration in master mode 0.

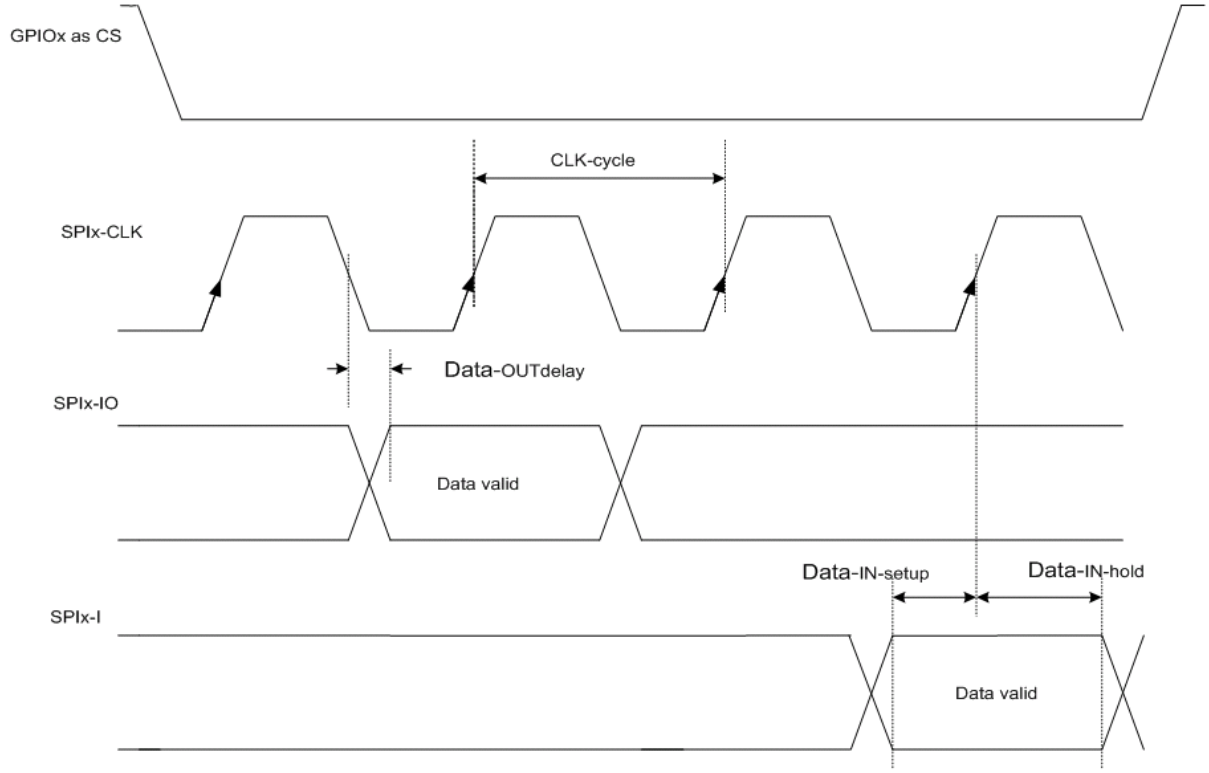


Figure 3. SPI Timing Diagrams; Mode 0, Master, 4 wires

Table 14. AC Characteristics of the SPI Bus

Signal	Description	Minimum	Typical	Minimum	Unit
CLK-cycle	SPI clock frequency	0.102		13	MHz
Data-OUT delay	Data out ready delay time			10	ns
Data-IN-setup	Data in setup time	2			ns
Data-OUT-hold	Data out hold time	2			ns

Waveforms for SPI transfer with the SPIx-LOAD signal configuration in master mode 0 (chip select is not represented).

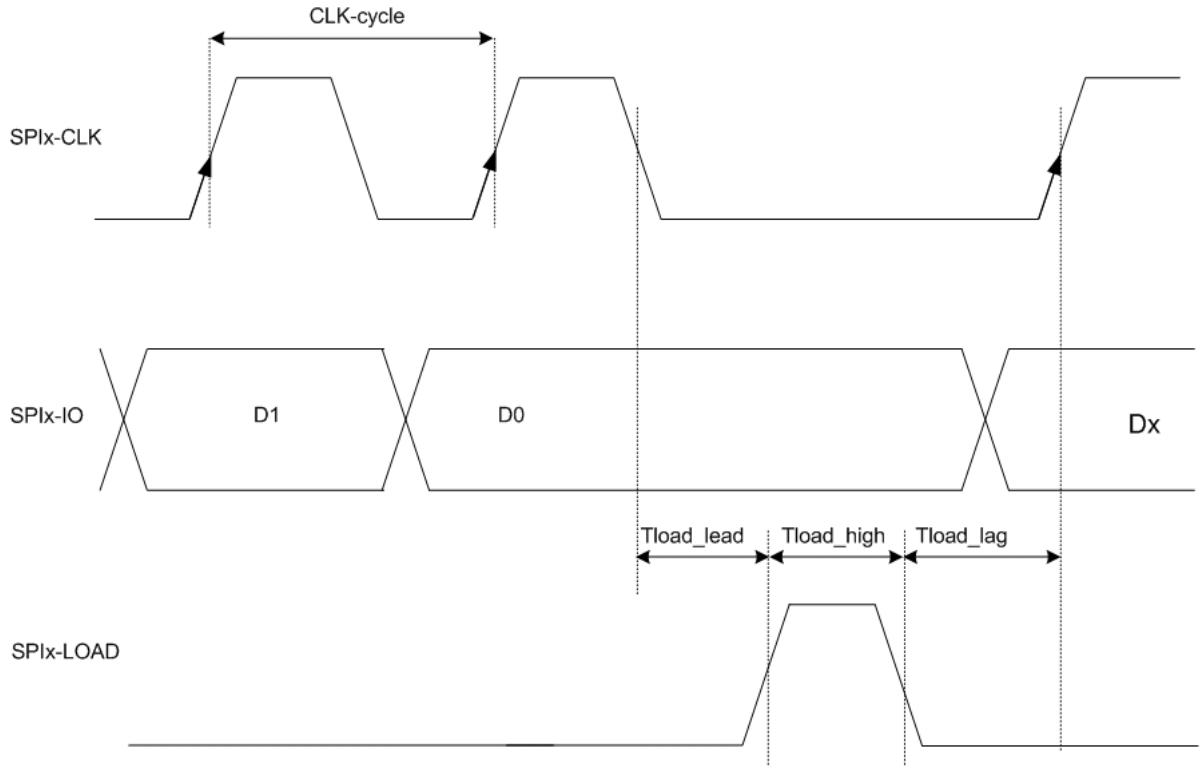


Figure 4. SPI Timing Diagrams with SPIx-LOAD Signal; Mode 0, Master, 4 wires

3.4.1.4. SPI1 Bus: Pins Description

Table 15. SPI1 Bus Pin Description

Signal	Pin #	I/O	I/O Type	Reset State	Description	Multiplexed with
SPI1-CLK	23	O	2V8	Z	SPI Serial Clock	GPIO28
SPI1-IO	25	I/O	2V8	Z	SPI Serial input/output	GPIO29
SPI1-I	24	I	2V8	Z	SPI Serial input	GPIO30
SPI1-LOAD	22	O	2V8	Z	SPI load	GPIO31

Refer to section 3.3 Electrical Information for Digital I/O for open drain, 2V8 and 1V8 voltage characteristics, and reset state definitions.

3.4.1.5. SPI2 Bus: Pins Description

Table 16. SPI2 Pin Description

Signal	Pin #	I/O	I/O Type	Reset State	Description	Multiplexed with
SPI2-CLK	26	O	2V8	Z	SPI Serial Clock	GPIO32
SPI2-IO	27	I/O	2V8	Z	SPI Serial input/output	GPIO33

Signal	Pin #	I/O	I/O Type	Reset State	Description	Multiplexed with
SPI2-I	29	I	2V8	Z	SPI Serial input	GPIO34
SPI2-LOAD	28	O	2V8	Z	SPI Load	GPIO35

Refer to section 3.3 Electrical Information for Digital I/O for open drain, 2V8 and 1V8 voltage characteristics, and reset state definitions.

3.4.1.6. Application Example for 4-wire SPI Bus

The specific feature of a 4-wire serial interface (SPI bus) is that the input and output data lines are disassociated. The SPIx-IO signal is used only for output data whereas the SPIx-I signal is used only for input data.

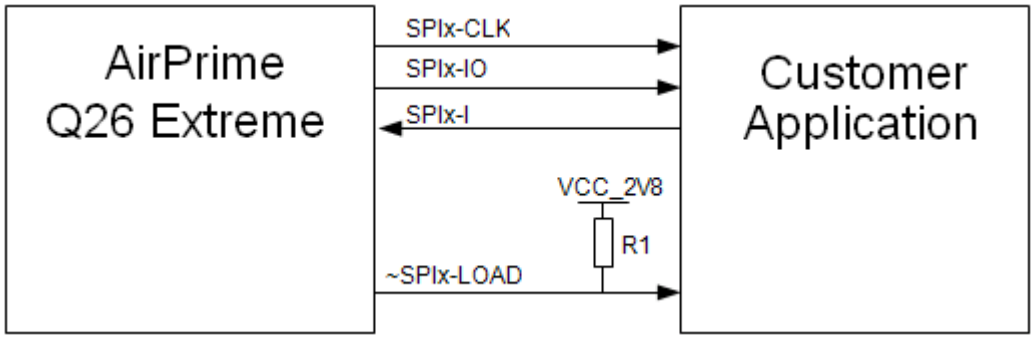


Figure 5. Example of 4-wire SPI Bus Application

One pull-up resistor R1 is needed to set the SPIx-CS level for the reset state. R1 recommended value: 100kΩ.

Except for R1, no external components are needed if the electrical specification of the customer application complies with the Q26 Extreme embedded module SPIx interface electrical specification.

3.4.1.7. Application Example for 3-wire SPI Bus

The specific feature of a 3-wire serial interface (SPI bus) is that the input and output data lines are disassociated. The SPIx-IO signal is used for both output and input data.

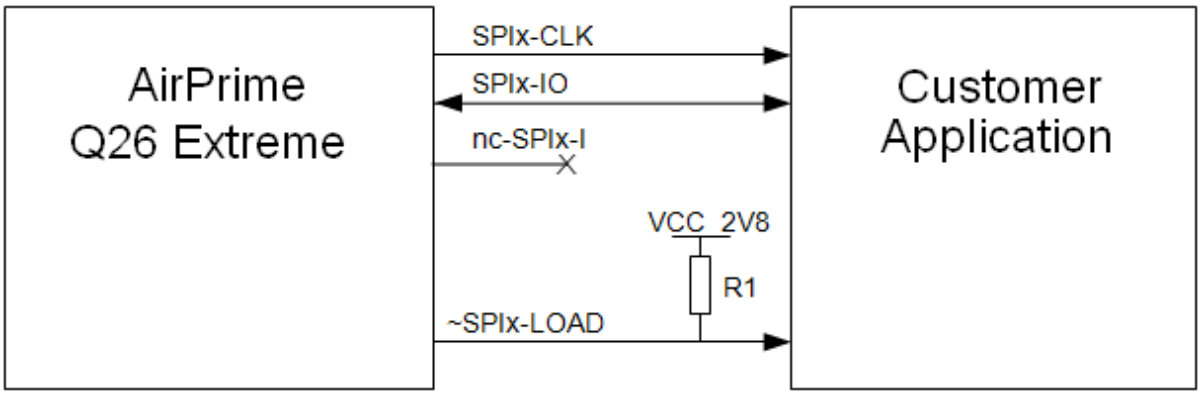


Figure 6. Example of 3-wire SPI Bus Application

One pull-up resistor R1 is needed to set the SPIx-CS level for the reset state. The R1 value depends on the peripheral plugged on the SPIx interface. R1 recommended value: 100kΩ.

Except for R1, no external components are needed if the electrical specification of the customer application complies with the Q26 Extreme embedded module SPIx interface electrical specification.

The SPIx-I line is not used in a 4-wire configuration. This line can be left open or used as GPIO for other application's functionality.

The SPIx interface voltage range is 2.8V. It can be powered either by VCC_2V8 (pin 10) of the Q26 Extreme embedded module or by any other power supply.

3.4.2. I²C Bus

The I²C interface includes a clock signal (SCL1) and data signal (SDA1) complying with a 100kbit/s-standard interface (standard mode: s-mode).

The I²C bus is always master.

The maximum speed transfer range is 400kbit/s (fast mode: f-mode).

3.4.2.1. I²C Waveforms

I²C bus waveform in master mode configuration:

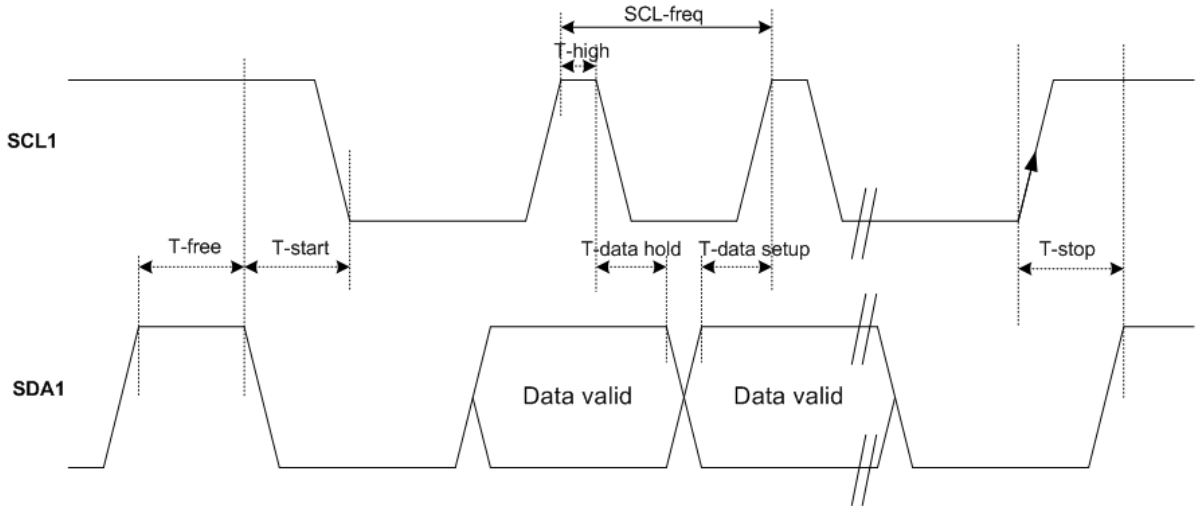


Figure 7. I²C Timing Diagrams, Master

Table 17. AC Characteristics of the I²C Bus

Signal	Description	Minimum	Typical	Maximum	Unit
SCL1-freq	I²C clock frequency	100		400	kHz
T-start	Hold time START condition	0.6			µs
T-stop	Setup time STOP condition	0.6			µs
T-free	Bus free time, STOP to START	1.3			µs
T-high	High period for clock	0.6			µs
T-data-hold	Data hold time	0		0.9	µs
T-data-setup	Data setup time	100			ns

3.4.2.2. I²C Bus Pin-Out

Table 18. I²C Bus Pin Description

Signal	Pin #	I/O	I/O Type	Reset State	Description	Multiplexed with
SCL1	44	O	Open drain	Z	Serial Clock	GPIO26
SDA1	46	I/O	Open drain	Z	Serial Data	GPIO27

Refer to section 3.3 Electrical Information for Digital I/O for open drain, 2V8 and 1V8 voltage characteristics, and reset state definitions.

3.4.2.3. Application Example

The two lines need to be pulled-up to the V_I²C voltage. The V_I²C voltage is dependent on the customer application component connected on the I²C bus. Nevertheless, the VI²C must comply with the Q26 Extreme embedded module electrical specification.

The VCC_2V8 (pin 10) of the Q26 Extreme embedded module may be used to connect the pull-up resistors, if the I²C bus voltage is 2.8 V.

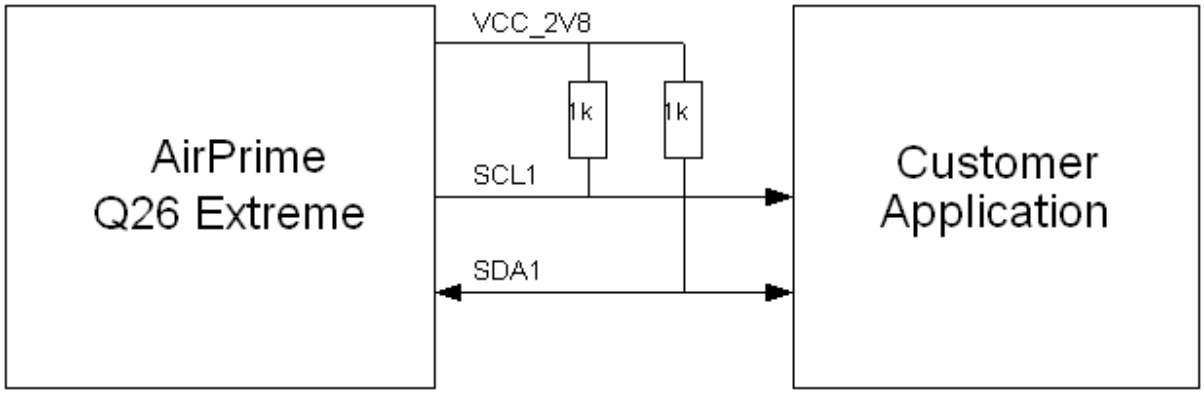


Figure 8. Example of I²C Bus Application

The pull-up resistor values are selected depending on the mode used. For Fast mode, it is recommended to use 1kΩ resistors in order to ensure the compliance with the I²C specification. For the Standard mode, higher values of resistors may be used to save power consumption.

3.5. Parallel Interface

3.5.1. General Description

The Q26 Extreme embedded module offers a 16-bit parallel and 1V8 bus interface. Its characteristics are described below:

- Up to 128 Mega Byte address range per chip select (CS2 and CS3)
- Support for 8, 16, and 32 bit (multiplexed synchronous mode) devices
- Byte enable signals for 16 bit and 32 bits operation
- Fully programmable timings based on AHB (a division of the ARM clock at 26 MHz) cycles (except for synchronous mode which is based on CLKBURST cycles at 26 MHz only)
  - individually selectable timings for read and write
  - 0 to 7 clock cycles for setup
  - 1 to 32 clock cycles for access cycle
  - 1 to 8 clock cycles for page access cycle
  - 0 to 7 clock cycles for hold
  - 1 to 15 clock cycles for turnaround
- Page mode Flash memory support
  - page size of 4, 8, 16 or 32
- Burst mode Flash memory support up to AHB (26 MHz) clock frequency (for devices sensitive to rising edge of the clock only)
  - AHB, AHB/2, AHB/4 or AHB/8 burst clock output
  - burst size of 4, 8, 16, 32
  - automatic CLKBURST power-down between accesses
- Intel mode (WE and OE) and Motorola mode (E and R/W) control signals
- Synchronous write mode
- Synchronous multiplexed data/address mode (x32 mode)
- Adaptation to word, halfword, and byte accesses to the external devices

3.5.2. Pin Description

Table 19. Parallel Bus Pin Description

Signal	Pin #	I/O	I/O Type	Reset State	Description	Multiplexed with
D0	85	I/O	1V8	Pull down	Bidirectional data and address line	Not mux
D1	87	I/O	1V8	Pull down	Bidirectional data and address line	Not mux
D2	89	I/O	1V8	Pull down	Bidirectional data and address line	Not mux
D3	91	I/O	1V8	Pull down	Bidirectional data and address line	Not mux
D4	93	I/O	1V8	Pull down	Bidirectional data and address line	Not mux
D5	95	I/O	1V8	Pull down	Bidirectional data and address line	Not mux

Signal	Pin #	I/O	I/O Type	Reset State	Description	Multiplexed with
D6	97	I/O	1V8	Pull down	Bidirectional data and address line	Not mux
D7	99	I/O	1V8	Pull down	Bidirectional data and address line	Not mux
D8	100	I/O	1V8	Pull down	Bidirectional data and address line	Not mux
D9	98	I/O	1V8	Pull down	Bidirectional data and address line	Not mux
D10	96	I/O	1V8	Pull down	Bidirectional data and address line	Not mux
D11	94	I/O	1V8	Pull down	Bidirectional data and address line	Not mux
D12	92	I/O	1V8	Pull down	Bidirectional data and address line	Not mux
D13	90	I/O	1V8	Pull down	Bidirectional data and address line	Not mux
D14	88	I/O	1V8	Pull down	Bidirectional data and address line	Not mux
D15	86	I/O	1V8	Pull down	Bidirectional data and address line	Not mux
~OE-R/W	81	O	1V8	1	Output enable signal (Intel mode); read not write signal (Motorola mode)	Not mux
~WE-E	84	O	1V8	1	Write enable Signal (Intel mode) Enable signal (Motorola mode)	Not mux
~CS3	83	I/O	1V8	Pull up	User Chip select 3	GPIO44
~CS2	51	I/O	1V8	Pull up	User Chip Select 2	GPIO1/INT2
A1	42	O	1V8	1	This signal has 2 functions: external Address or byte enable 2 for 16 or 32 bits devices. Another name is used: A1_BE2	Not mux
A24	53	I/O	1V8	Z	Address line for external device / Command selection	GPIO2

3.5.3. Asynchronous Access Bus and Timing

For all timing diagrams in the following section the notations hereafter are used:

- ADR is used for address bus A [24,1] or D [15:0].when used as address lines
- DATA is used for D[15:0] when used as DATA lines
- ~CS is used for ~CS2 or~CS3
- ~BE is used for A1_~BE2 (Double function on A1 pin)

- ~OE and R/W are used for ~OE_R/W
- ~WE and E are used for ~WE_E
- ~ADV signal (Not available on the 100-pin connector) is the address valid signal

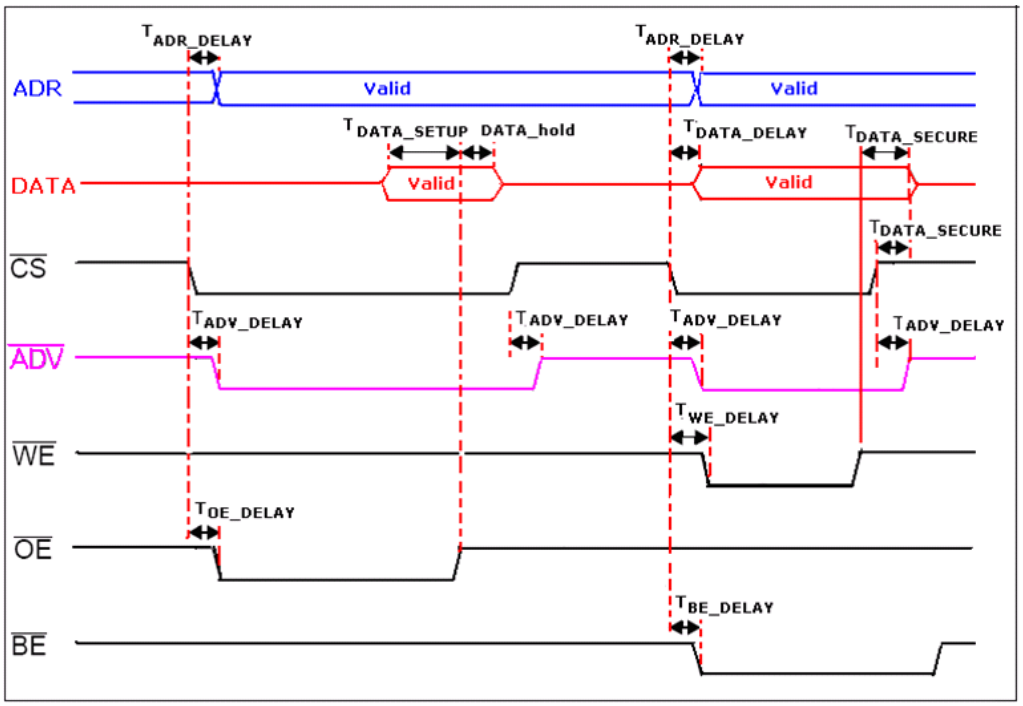


Figure 9. Asynchronous Access

The ~ADV signal is mentioned here because synchronous mode devices may require the signal to be asserted when an asynchronous access is performed.

3.5.4. AC Characteristics of Asynchronous Accesses

Table 20. AC Characteristic of Asynchronous Accesses

Signal	Description	Minimum	Typical	Maximum	Unit
T_{ADR_DELAY}	ADR delay time from ~CS active			3	ns
T_{DATA_SETUP}	DATA to ~OE setup time	18			ns
T_{DATA_HOLD}	DATA hold time after ~OE inactive	3		4	ns
T_{DATA_DELAY}	DATA delay time from ~CS active			5	ns
T_{DATA_SECURE}	DATA hold time after ~WE inactive or ~CS inactive	-5*			ns
T_{ADV_DELAY}	ADV delay time from ~CS active and inactive			3	ns
T_{WE_DELAY}	~WE delay time from ~CS active			3**	ns
T_{OE_DELAY}	~OE delay time from ~CS active			3**	ns
T_{BE_DELAY}	~BE delay time from ~CS active			3	ns

* This timing forces to program at least one cycle for asynchronous.

** These maximum delays also depend on the setting of registers.

3.5.5. Synchronous Access Bus and Timing

For all timing diagrams in the following section the notations hereafter are used:

- ADR is used for address bus as A24, A1 or D [15:0] when used as address lines
- DATA is used for D [15:0] when used as data lines
- ~CS is used for ~CS2 or ~CS3
- ~BE is used for A1_~BE2 (Double function on A1 pin)
- ~OE and R/W are used for ~OE_R/W
- ~WE and E are used for ~WE_E
- CLKBURST is the internal clock at 26 MHz (Not available on connector pinout)
- ~ADV signal (Not available on the 100-pin connector) is the address valid signal
- ~BAA signal (Not available on the 100-pin connector) is the burst address advance for synchronous operations
- ~WAIT signal (Not available on the 100-pin connector) is the wait signal for synchronous operation

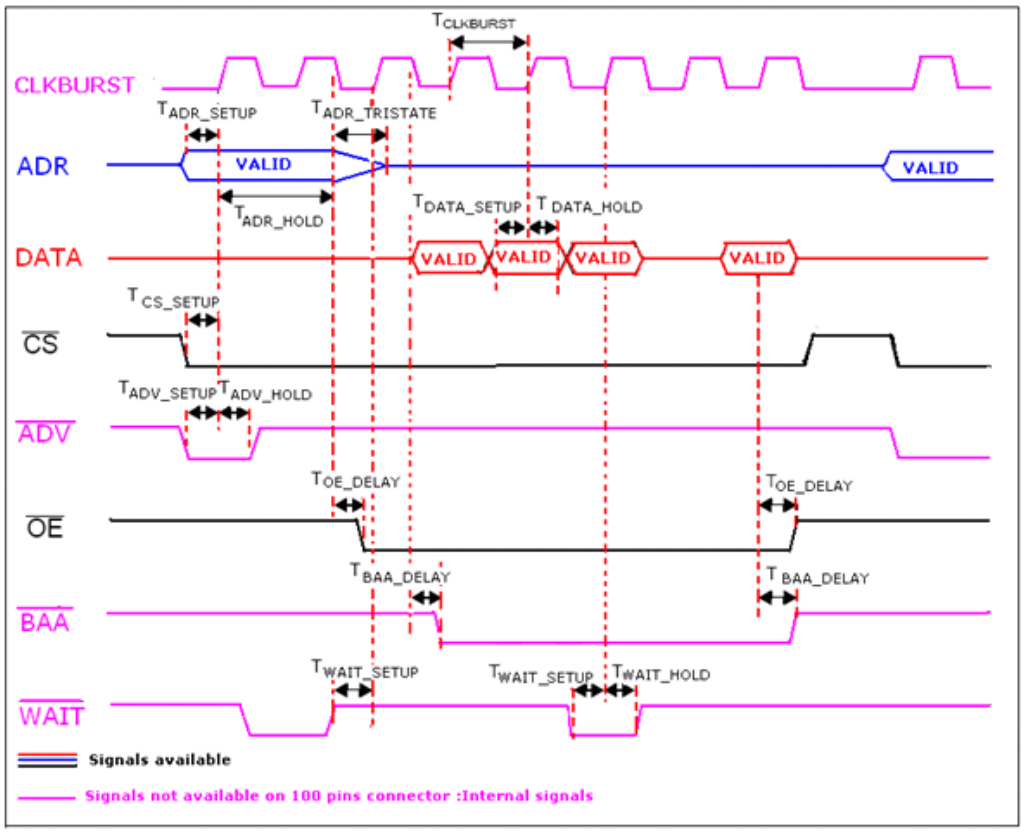


Figure 10. Read Synchronous Timing

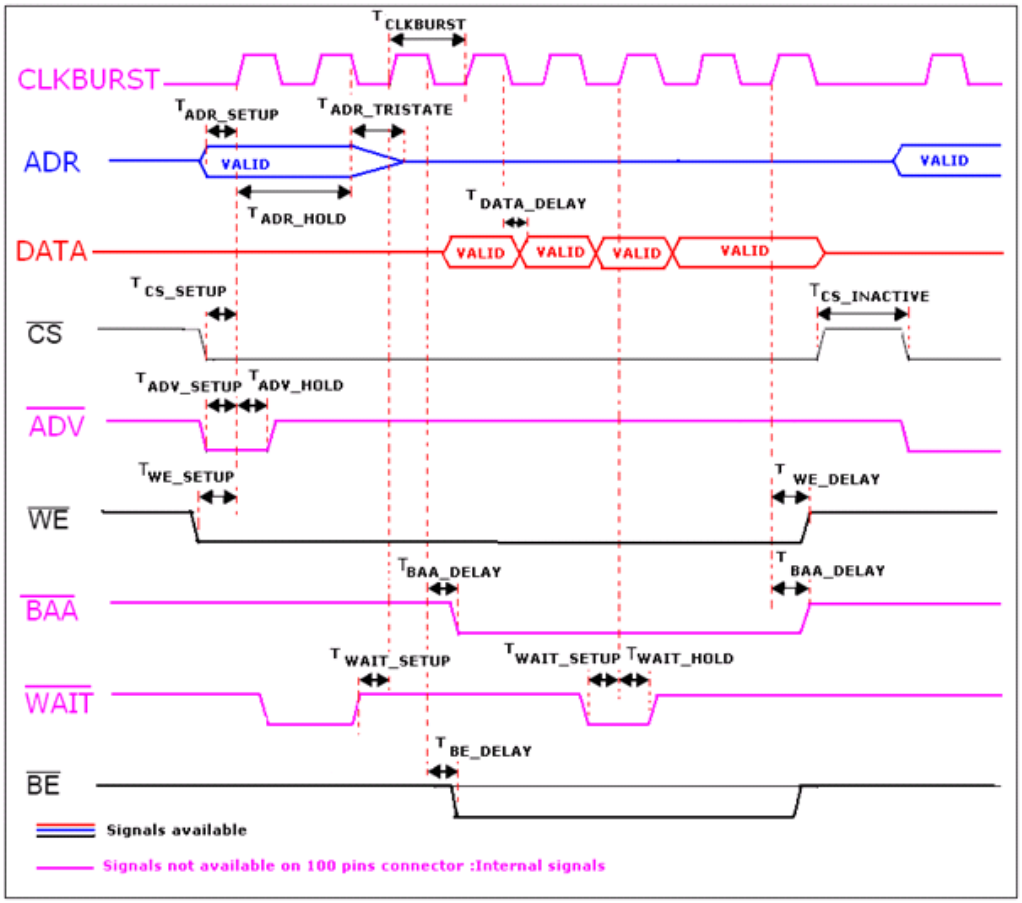


Figure 11. Write Synchronous Timing

3.5.6. AC Characteristic of Synchronous Accesses

Table 21. AC Characteristic of Synchronous Accesses

Signal	Description	Minimum	Typical	Maximum	Unit
T_{DATA_DELAY}	CLKBURTS falling edge to DATA valid delay			4	ns
T_{WE_SETUP}	WE to CLKBURST setup time	7			ns
T_{BE_DELAY}	CLKBURST falling edge to BE delay			4	ns
$T_{CLKBURST}$	CLKBURST clock : period time		38.4		ns
T_{ADR_SETUP}	Address bus setup time	7			ns
T_{ADR_HOLD}	Address bus hold time	19			ns
$T_{ADR\_TRISTATE}$	Address bus tristate time			10	ns
T_{DATA_SETUP}	Data bus setup time	5			ns
T_{DATA_HOLD}	Data bus hold time	3			ns
T_{CS_SETUP}	Chip select setup time	7			ns
T_{ADV_SETUP}	ADV setup time	7			ns
T_{ADV_HOLD}	ADV hold time	7			ns
T_{OE_DELAY}	Output Enable delay time			13	ns
T_{BAA_DELAY}	BAA delay time			13	ns
T_{WAIT_SETUP}	Wait setup time	5			ns

Signal	Description	Minimum	Typical	Maximum	Unit
T_{WAIT_HOLD}	Wait hold time	5			ns

3.5.7. Example of Typical Application Using Parallel Bus

For example, it is possible to interface a NAND memory.

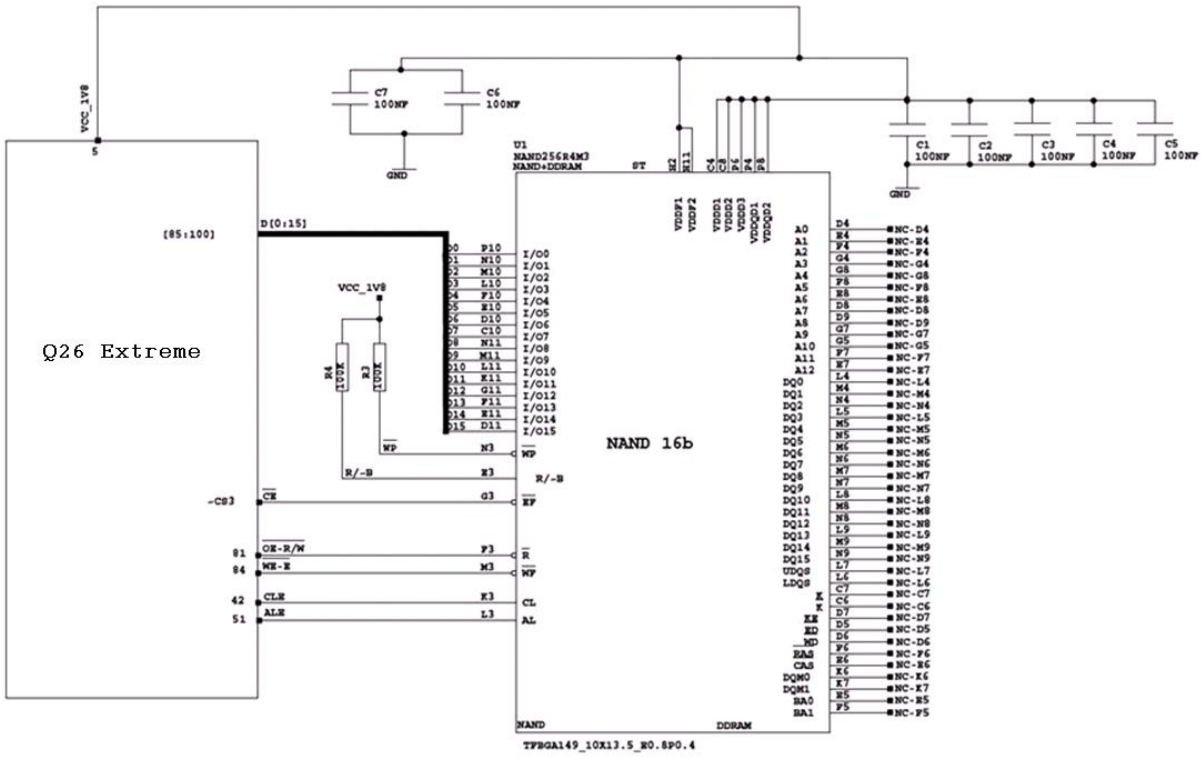


Figure 12. Example of Parallel Bus Application (NAND)

3.5.8. Additional Information on Address Size Bus

The following table lists the possible configurations depending on address bus size requested on parallel interface.

Table 22. Address Bus Size Details

Address Bus Size	Address Lines	Chip Select Available
1	A1	/CS2, /CS3
2	A1, A24	/CS2, /CS3

Few signals are multiplexed. It is thus possible to have these configurations.

- ~CS3*, A1, GPIO2
- ~CS3*, A1, A24,
- ~CS3*, ~CS2*, A1, GPIO2
- ~CS3*, ~CS2*, A1, A24

3.6. Keyboard Interface

This interface provides 10 connections:

- 5 rows (ROW0 to ROW4) and
- 5 columns (COL0 to COL4)

Scanning is digital and debouncing is performed in the Q26 Extreme embedded module.

No discrete components such as resistors or capacitors are needed.

Table 23. Keyboard Interface Pin Description

Signal	Pin #	I/O	I/O Type	Reset State	Description	Multiplexed with
ROW0	68	I/O	1V8	0	Row scan	GPIO9
ROW1	67	I/O	1V8	0	Row scan	GPIO10
ROW2	66	I/O	1V8	0	Row scan	GPIO11
ROW3	65	I/O	1V8	0	Row scan	GPIO12
ROW4	64	I/O	1V8	0	Row scan	GPIO13
COL0	59	I/O	1V8	Pull-up	Column scan	GPIO4
COL1	60	I/O	1V8	Pull-up	Column scan	GPIO5
COL2	61	I/O	1V8	Pull-up	Column scan	GPIO6
COL3	62	I/O	1V8	Pull-up	Column scan	GPIO7
COL4	63	I/O	1V8	Pull-up	Column scan	GPIO8

Refer to section 3.3 Electrical Information for Digital I/O for open drain, 2V8 and 1V8 voltage characteristics, and reset state definitions.

With the Sierra Wireless Software Suite, when the keyboard service is used, the whole multiplexed signals become unavailable for other purposes. In the same way, if one or more GPIOs (from the table above) are allocated, the keyboard service is unavailable.

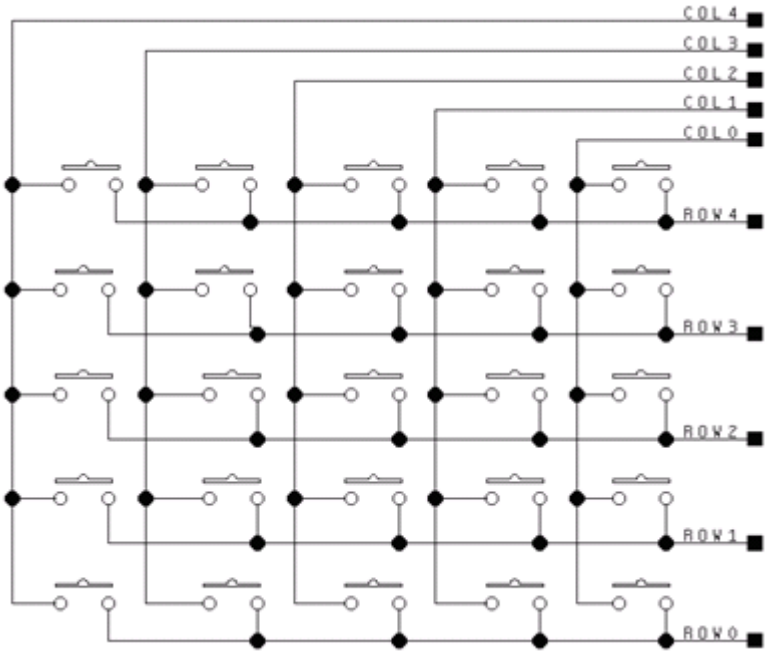


Figure 13. Example of Keyboard Implementation

3.7. Main Serial Link (UART1)

A flexible 8-wire serial interface is available that complies with V24 protocol signaling, but not with V28 (electrical interface) due to a 2.8 volts interface.

The signals are:

- TX data (CT103-TX)
- RX data (CT104-RX)
- Request To Send (~CT105-RTS)
- Clear To Send (~CT106-CTS)
- Data Terminal Ready (~CT108-2-DTR)
- Data Set Ready (~CT107-DSR)
- Data Carrier Detect (~CT109-DCD)
- Ring Indicator (CT125-RI)

Table 24. UART1 Interface Pin Description

Signal*	Pin #	I/O	I/O Type	Reset State	Description	Multiplexed with
CT103-TXD1	71	I	2V8	Z	Transmit serial data	GPIO36
CT104-ZXD1	73	O	2V8	Z	Transmit serial data	GPIO37
~CT105-RTS1	72	I	2V8	Z	Request To Send	GPIO38
~CT106-CTS1	75	O	2V8	Z	Clear To Send	GPIO39
~CT107-DSR1	74	O	2V8	Z	Data Set Ready	GPIO40
~CT108-2-DTR1	76	I	2V8	Z	Data Terminal Ready	GPIO41
~CT109-DCD1	70	O	2V8	Undefined	Data Carrier Detect	GPIO43
~CT125-RI1	69	O	2V8	Undefined	Ring Indicator	GPIO42
CT102-GND	Shielding leads		GND		Ground	

* According to PC view

Refer to section 3.3 Electrical Information for Digital I/O for open drain, 2V8 and 1V8 voltage characteristics, and reset state definitions.

With the Sierra Wireless Software Suite, when the UART1 service is used, the whole multiplexed signals become unavailable for other purposes. In the same way, if one or more GPIOs (from the table above) are allocated, the UART1 service is unavailable.

The **rise** and **fall time** of the reception signals (mainly CT103) must be less than 300ns.

The maximum baud rate of UART1 is 921kbit/s for the Sierra Wireless Software Suite firmware.

Caution: *The Q26 Extreme embedded module is designed to operate using all the serial interface signals. In particular, it is mandatory to use RTS and CTS for hardware flow control in order to avoid data loss/corruption during transmission.*

3.7.1. Typical Implementation

The level shifter must be 2.8V with V28 electrical signal compliance.

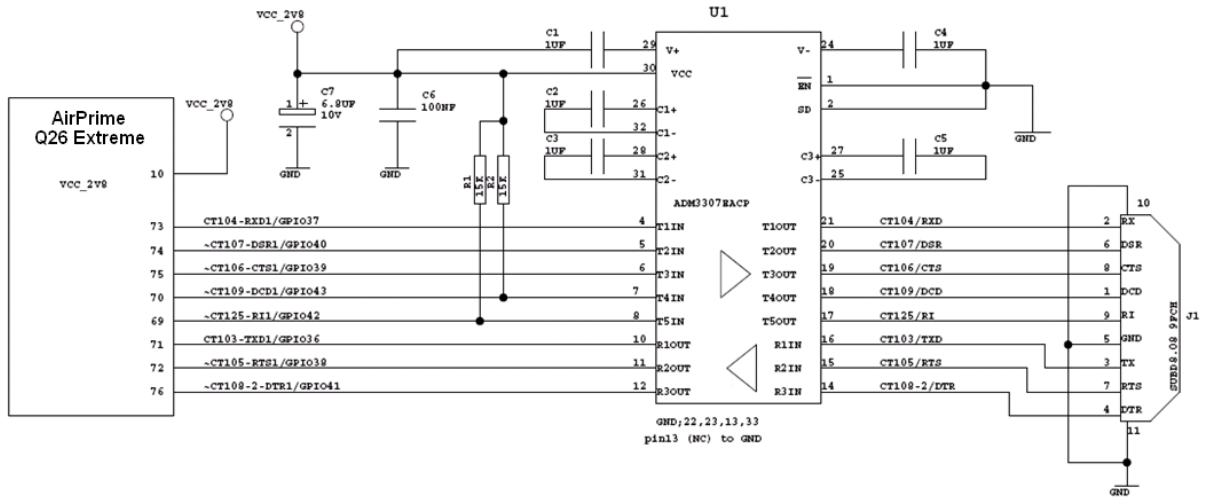


Figure 14. Example of RS-232 Level Shifter Implementation for UART1

U1 chip also protects the embedded module against ESD at 15kV (Air Discharge).

Recommended Components:

- R1, R2: 15kΩ
- C1, C2, C3, C4, C5: 1µF
- C6: 100nF
- C7: 6.8µF TANTAL 10V CP32136 AVX
- U1: ADM3307AECP Analog devices
- J1: SUB-D9 female

R1 and R2 are necessary only during the Reset state, to force the ~CT1125-RI1 and ~CT109-DCD1 signals to high levels.

The ADM3307EACP chip has a maximum speed of 921kbits/s. If other level shifters are used, ensure that their speeds are compliant with the UART1 useful speed.

The ADM3307EACP can be powered either by VCC_2V8 (pin 10) of the Q26 Extreme embedded module or by an external regulator at 2.8 volts.

If the UART1 interface is connected directly to a host processor, it is not necessary to use level shifters. The interface can be connected as shown in Figure 15 Example of V24/CMOS Serial Link Implementation for UART1.

3.7.1.1. V24/CMOS Possible Design

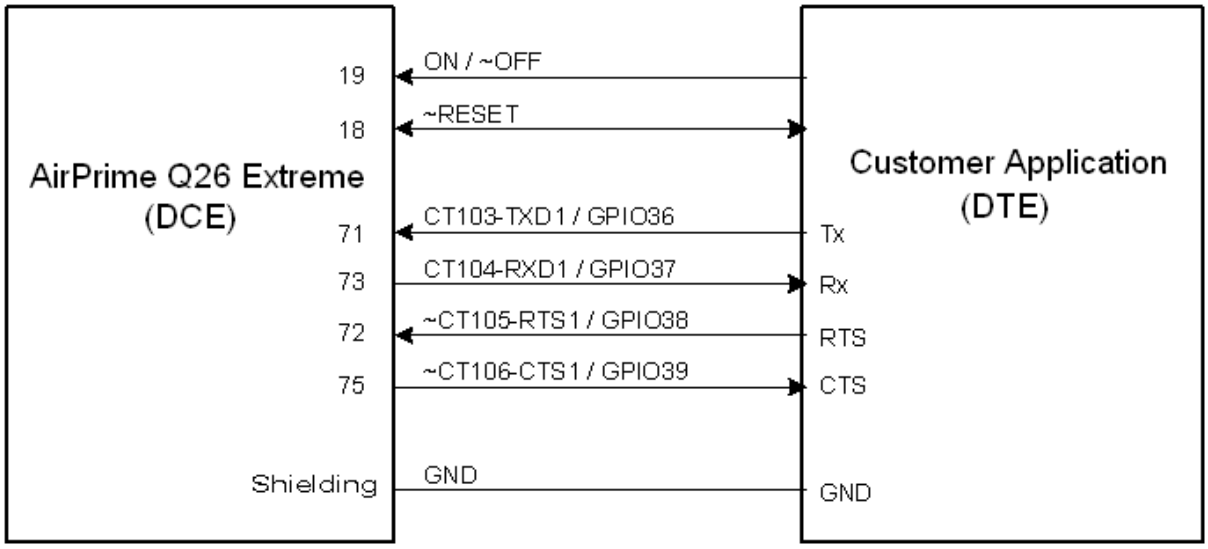


Figure 15. Example of V24/CMOS Serial Link Implementation for UART1

The design shown in the above figure is a basic design type.

However, a more flexible design to access this serial link with all the modem signals is shown below:

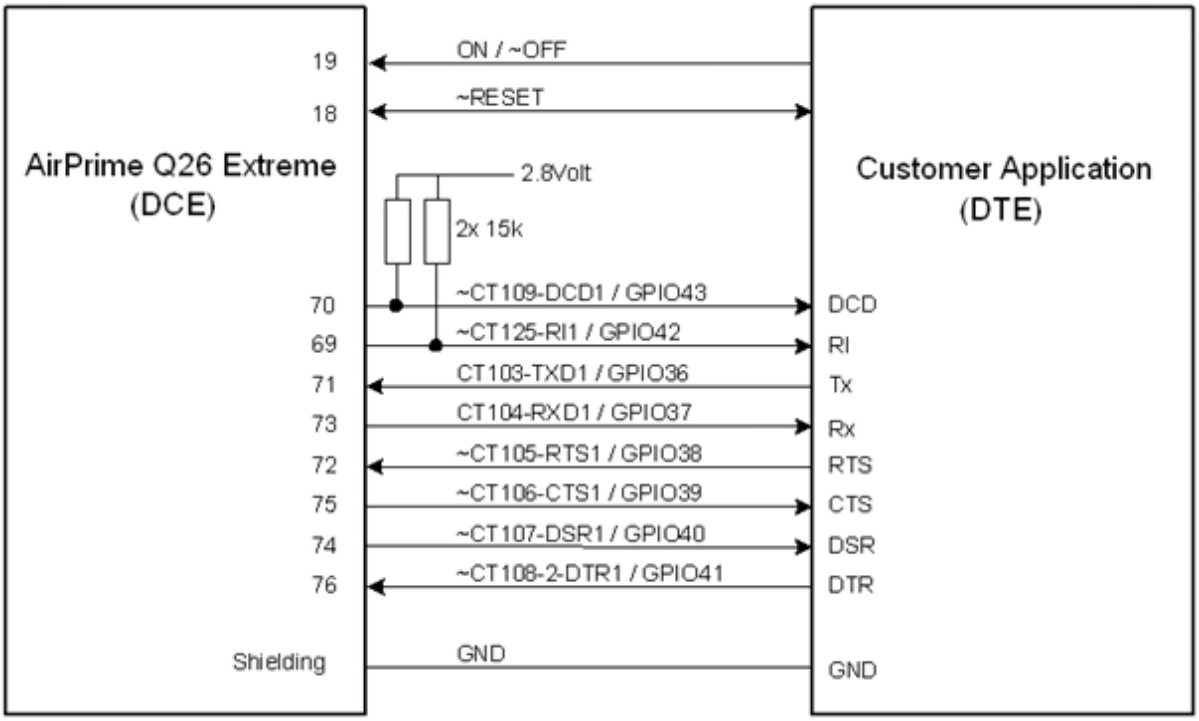


Figure 16. Example of Full Modem V24/CMOS Serial Link Implementation for UART1

It is recommended to add 15kΩ pull-up resistors on ~CT125-RI1 and ~CT109-DCD1 to set them to high level during the reset state.

The UART1 interface is 2.8 volts type. Moreover, it is 3.3 volts tolerant.

3.7.1.2. For Use with 5-wire Serial Interface

- Signals: CT103-TXD1, CT104-RXD1, ~CT105-RTS1, ~CT106-CTS1, ~CT108-2/DTR1
- The signal ~CT108-2-DTR1 must be managed by following the V24 protocol signaling, if you want to use sleep idle mode.
- Other signals and their multiplexes are not available.
- Please refer to the technical appendixes of document [5] Firmware v7.4 AT Commands Manual for more information.

3.7.1.3. For Use with 4-wire Serial Interface

- Signals: CT103-TXD1, CT104-RXD1, ~CT105-RTS1, ~CT106-CTS1
- The signal ~CT108-2-DTR1 must be configured at low level.
- Other signals and their multiplexes are not available.
- Please refer to the technical appendixes of document [5] Firmware v7.4 AT Commands Manual for more information.

3.7.1.4. For Use with 2-wire Serial Interface

This case is possible for a connected external chip, but not recommended (and forbidden for AT command or modem use).

The flow control mechanism has to be managed at the customer side.

- Signals: CT103-TXD1, CT104-RXD1
- The signal ~CT108-2-DTR1 must be configured at low level.
- The signals ~CT105-RTS1, ~CT106-CTS1 are not used, please configure the AT command (**AT+IFC=0,0** see document [5] Firmware v7.4 AT Commands Manual for more information).
- The signal ~CT105-RTS1 must be configured at low level.
- Other signals and their multiplexes are not available.
- Please refer to the technical appendixes of document [5] Firmware v7.4 AT Commands Manual for more information.

3.8. Auxiliary Serial Link (UART2)

An auxiliary serial interface (UART2) is available on the Q26 Extreme embedded module. This interface may be used to connect a Bluetooth or a GPS chip controlled by a Plug-in.

Table 25. UART2 Interface Pin Description

Signal*	Pin #	I/O	I/O Type	Reset State	Description	Multiplexed with
CT103-TXD2	31	I	1V8	Z	Transmit serial data	GPIO14
CT104-RXD2	30	O	1V8	Z	Receive serial data	GPIO15
~CT106-CTS2	32	O	1V8	Z	Clear To Send	GPIO16
~CT105-RTS2	33	I	1V8	Z	Request To Send	GPIO17

* According to PC view

Refer to section 3.3 Electrical Information for Digital I/O for open drain, 2V8 and 1V8 voltage characteristics, and reset state definitions.

Caution: *UART2 of the Q26 Extreme embedded module is designed to operate using all the serial interface signals. In particular, it is recommended to use RTS and CTS for hardware flow control in order to avoid data corruption during transmission.*

The maximum baud rate of UART2 is **921**kbit/s for the Sierra Wireless Software Suite firmware.

3.8.1. Typical Implementation

The voltage level shifter must be 1.8 volts with V28 electrical signal compliance.

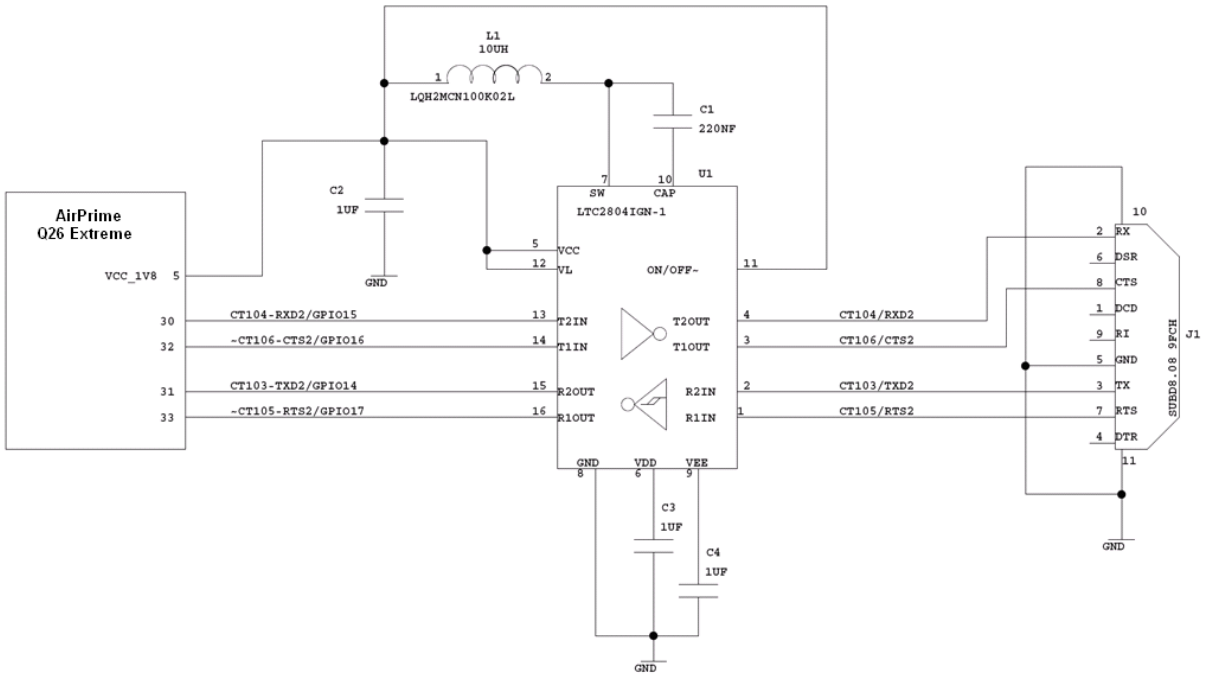


Figure 17. Example of RS-232 Level Shifter Implementation for UART2

3.8.1.1. Recommended Components

- Capacitors
  - C1: 220nF
  - C2, C3, C4: 1μF
- Inductor
  - L1: 10μH
- RS-232 Transceivers
  - U1: LINEAR TECHNOLOGY LTC®2804IGN
  - J1: SUB-D9 female

The LTC2804 may be powered either by VCC_1V8 (pin 5) of the Q26 Extreme embedded module or by an external regulator at 1.8 volts.

The UART2 interface may be connected directly to other components, if the voltage interface is 1.8V.

3.8.1.2. For Use with 4-wire Serial Interface

- Signals: CT103-TXD2, CT104-RXD2, ~CT105-RTS2, ~CT106-CTS2
- Other signals and their multiplexes are not available.
- Please refer to the technical appendixes of document [5] Firmware v7.4 AT Commands Manual for more information.

3.8.1.3. For Use with 2-wire Serial Interface

This case is possible for a connected external chip, but not recommended (and forbidden for AT command or modem use).

The flow control mechanism has to be managed at the customer side.

- Signals: CT103-TXD2, CT104-RXD2
- The signals ~CT105-RTS2, ~CT106-CTS2 are not used; you must configure the AT command (**AT+IFC=0,0** see document [5] Firmware v7.4 AT Commands Manual).
- The signal ~CT105-RTS2 must be configured at low level.
- Other signals and their multiplexes are not available.
- Please refer to the technical appendixes of document [5] Firmware v7.4 AT Commands Manual for more information.

3.9. USIM/SIM Interface

The Universal Subscriber Identification Module (USIM) may be directly connected to the Q26 Extreme embedded module via this dedicated interface. Using the USIM is recommended over the SIM card.

3.9.1. General Description

The five signals are:

- SIM-VCC: USIM power supply
- ~SIM-RST: reset
- SIM-CLK: clock
- SIM-IO: I/O port
- SIMPRES: USIM card detect

The USIM interface controls a 1V8/3V USIM.

Table 26. USIM Interface Pin Description

Signal	Pin #	I/O	I/O Type	Reset State	Description	Multiplexed with
SIM-CLK	14	O	2V9 / 1V8	0	USIM Clock	Not mux
~SIM-RST	13	O	2V9 / 1V8	0	USIM Reset	Not mux
SIM-IO	11	I/O	2V9 / 1V8	Pull-up*	USIM Data	Not mux
SIM-VCC	9	O	2V9 / 1V8		USIM Power Supply	Not mux
SIMPRES	12	I	1V8	Z	USIM Card Detect	GPIO18

* USIM-IO pull-up is about 10kΩ

Refer to section 3.3 Electrical Information for Digital I/O for open drain, 2V8 and 1V8 voltage characteristics, and reset state definitions.

Table 27. USIM Interface Electrical Characteristics

Parameter	Condition	Minimum	Typical	Maximum	Unit
SIM-IO V_{IH}	I_{IH} = ± 20µA	0.7xSIMVCC			V
SIM-IO V_{IL}	I_{IL} = 1mA			0.4	V
~SIM-RST, SIM-CLK V_{OH}	Source current = 20µA	0.9xSIMVCC			V
SIM-IO V_{OH}	Source current = 20µA	0.8xSIMVCC			
~SIM-RST, SIM-IO, SIM-CLK V_{OL}	Sink current = -200µA			0.4	V
SIM-VCC Output Voltage	SIMVCC = 2.9V IVCC= 1mA	2.84	2.9	2.96	V
	SIMVCC = 1.8V IVCC= 1mA	1.74	1.8	1.86	V
SIM-VCC current	VBATT = 3.8V			10	mA
SIM-CLK Rise/Fall Time	Loaded with 30pF		20		ns
~SIM-RST, Rise/Fall Time	Loaded with 30pF		20		ns
SIM-IO Rise/Fall Time	Loaded with 30pF		0.7	1	µs
SIM-CLK Frequency	Loaded with 30pF			3.25	MHz

*Note: When **SIMPRES** is used, a **low to high** transition means that the USIM card is inserted and a **high to low** transition means that the USIM card is removed.*

3.9.2. Typical Implementation with SIM Detection

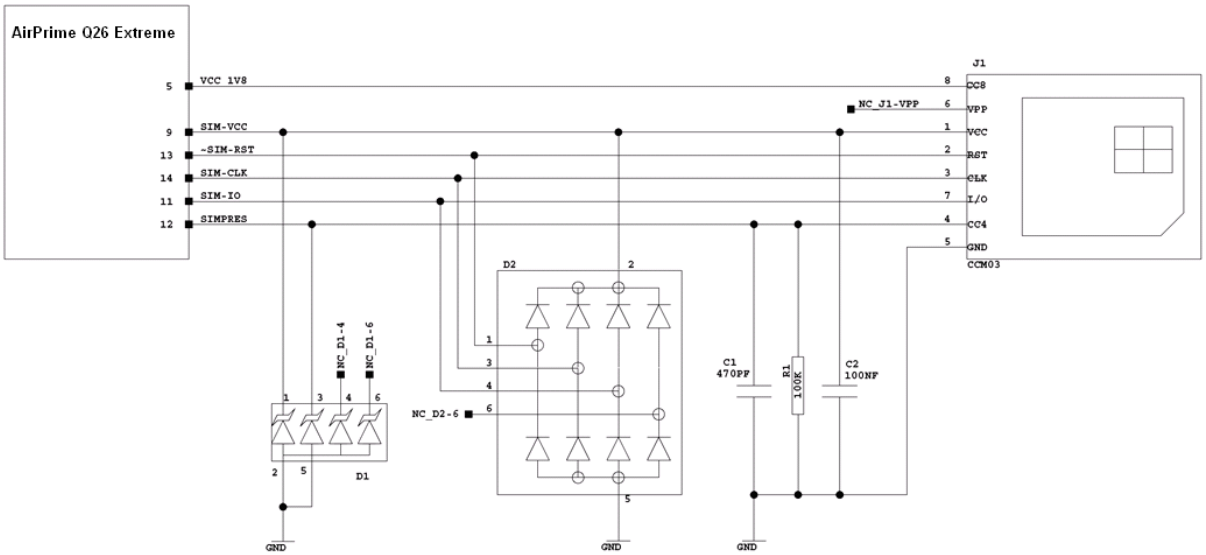


Figure 18. Example of SIM Socket Implementation

3.9.2.1. Recommended Components

- R1: 100 kΩ
- C1: 470 pF
- C2: 100 nF
- D1: ESDA6V1SC6 from ST
- D2: DALC208SC6 from SGS-THOMSON
- J1: ITT CANNON CCM03 series

The capacitor (C2) placed on the SIM-VCC line must not exceed 330nF.

Table 28. SIM Socket Pin Description

Signal	Pin Number	Description
VCC	1	SIM-VCC
RST	2	~SIM-RST
CLK	3	SIM-CLK
CC4	4	SIMPRES with 100 kΩ pull-down resistor
GND	5	GROUND
VPP	6	Not connected
I/O	7	SIM-IO
CC8	8	VCC_1V8 of the embedded module (pin 5)

3.10. General Purpose Input/Output

The Q26 Extreme embedded module provides up to 45 General Purpose I/Os, used to control any external device such as an LCD or a Keyboard backlight.

Table 29. GPIO Pin Description

Signal	Pin #	I/O	I/O Type	Reset State	Description	Multiplexed with
GPIO0	43	I/O	2V8	Undefined	32kHz**	
GPIO1	51	I/O	1V8	Pull-up	~CS2 / INT2	
GPIO2	53	I/O	1V8	Z	A24	
GPIO3***	50	I/O	1V8	Z	INT0	
GPIO4	59	I/O	1V8	Pull-up	COL0	
GPIO5	60	I/O	1V8	Pull-up	COL1	
GPIO6	61	I/O	1V8	Pull-up	COL2	
GPIO7	62	I/O	1V8	Pull-up	COL3	
GPIO8	63	I/O	1V8	Pull-up	COL4	
GPIO9	68	I/O	1V8	0	ROW0	
GPIO10	67	I/O	1V8	0	ROW1	
GPIO11	66	I/O	1V8	0	ROW2	
GPIO12	65	I/O	1V8	0	ROW3	
GPIO13	64	I/O	1V8	0	ROW4	
GPIO14	31	I/O	1V8	Z	CT103-TXD2	
GPIO15	30	I/O	1V8	Z	CT104-RXD2	
GPIO16	32	I/O	1V8	Z	~CT106-CTS2	
GPIO17	33	I/O	1V8	Z	~CT105-RTS2	
GPIO18	12	I/O	1V8	Z	SIMPRES	
GPIO19	45	I/O	2V8	Z	Not mux	
GPIO20	48	I/O	2V8	Undefined	Not mux	
GPIO21	47	I/O	2V8	Undefined	Not mux	
GPIO22	57	I/O	2V8	Z	Not mux*	
GPIO23	55	I/O	2V8	Z	Not mux	
GPIO24	58	I/O	2V8	Z	Not mux	
GPIO25	49	I/O	2V8	Z	INT1	
GPIO26	44	I/O	Open drain	Z	SCL1	
GPIO27	46	I/O	Open drain	Z	SDA1	
GPIO28	23	I/O	2V8	Z	SPI1-CLK	
GPIO29	25	I/O	2V8	Z	SPI1-IO	
GPIO30	24	I/O	2V8	Z	SP1-I	
GPIO31	22	I/O	2V8	Z	SPI1_LOAD	
GPIO32	26	I/O	2V8	Z	SPI2-CLK	
GPIO33	27	I/O	2V8	Z	SPI2-IO	
GPIO34	29	I/O	2V8	Z	SPI2-I	
GPIO35	28	I/O	2V8	Z	SPI2_LOAD	
GPIO36	71	I/O	2V8	Z	CT103-TXD1	

Signal	Pin #	I/O	I/O Type	Reset State	Description	Multiplexed with
GPIO37	73	I/O	2V8	1	CT104-RXD1	
GPIO38	72	I/O	2V8	Z	~CT105-RTS1	
GPIO39	75	I/O	2V8	Z	~CT106-CTS1	
GPIO40	74	I/O	2V8	Z	~CT107-DSR1	
GPIO41	76	I/O	2V8	Z	~CT108-2-DTR1	
GPIO42	69	I/O	2V8	Undefined	~CT125-RI1	
GPIO43	70	I/O	2V8	Undefined	~CT109-DCD1	
GPIO44	83	I/O	2V8	Pull-up	PWM1 / ~CS3	

* If a Bluetooth module is used with the Q26 Extreme embedded module, these GPIOs must be reserved.

** With the Sierra Wireless Software Suite. See document [5] Firmware v7.4 AT Commands Manual

*** GPIO3 is the associated GPIO used with **AT+WTBI** to monitor TDM bursts. For more information about this AT command, refer to document [5] Firmware v7.4 AT Commands Manual.

Refer to section 3.3 Electrical Information for Digital I/O for open drain, 2V8 and 1V8 voltage characteristics, and reset state definitions.

Reset State:

- 0: Set to GND
- 1: Set to supply 1V8 or 2V8 depending on I/O type.
- Pull-down: Internal pull-down with ~60k resistor.
- Pull-up: Internal pull-up with ~60kΩ resistor to supply 1V8 or 2V8 depending on I/O type.
- Z: High impedance.
- Undefined: this must not be used in your application if a special state at reset is needed. These pins may be of toggling signals.

3.11. Analog to Digital Converter

Two Analog to Digital Converter inputs are provided by the Q26 Extreme embedded module. The converters are more than 10-bit resolution, ranging from 0 volt to 2 volts.

The ADC1/BAT-TEMP input can be used, typically, to monitor external temperature, which can be used as an indicator to safely power off the application in case of overheating (for Li-Ion battery).

The ADC2 input can be used for customer applications.

Table 30. ADC Pin Description

Signal	Pin #	I/O	I/O Type	Description
ADC1/BAT-TEMP*	20	I	Analog	A/D converter
ADC2	21	I	Analog	A/D converter

* This input can be used for a battery charging temperature sensor; see section 3.15 Battery Charging Interface.

Table 31. Electrical Characteristics of the ADC

Parameter		Minimum	Typical	Maximum	Unit
Maximum output code			1635		LSB
Sampling period		0,5		3*	s
Input signal range		0		2	V
Input impedance	ADC1/BAT-TEMP		1M		Ω
	ADC2		1M		Ω

* Sampling rate only for ADC2 and the Sierra Wireless Software Suite application.

3.12. Digital to Analog Converter

One Digital to Analog Converter (DAC) input is provided by the embedded module.

The converter is 8-bit resolution, guaranteed monotonic with a range from 0V to 2.3V. This output assumes a typical external load of 2kΩ and 50pF in parallel to GND.

Table 32. DAC Pin Description

Signal	Pin #	I/O	I/O Type	Description
DAC0	82	O	Analog	D/A converter

Table 33. Electrical Characteristics of the DAC

Parameter	Minimum	Typical	Maximum	Unit
Resolution	-	8	-	bits
Maximum Output voltage	2.1	2.2	2.3	V
Minimum Output voltage	0	-	40	mV
Output voltage after reset	-	1.147	-	V
Integral Accuracy	-5	-	+5	LSB
Differential Accuracy	-1	-	+1	LSB
Full scale settling time (load: 50pF // 2kΩ to GND)	-	40	-	µs
One LSB settling time (load: 50pF // 2kΩ to GND)	-	8	-	µs

3.13. Analog Audio Interface

Two different microphone inputs and two different speaker outputs are supported. The Q26 Extreme embedded module also includes an echo cancellation feature and noise reduction, which allows hands-free functionality.

In some cases, ESD protection must be added on the audio interface lines.

3.13.1. Microphone Features

The connection can be either differential or single-ended, but using a differential connection in order to reject common mode noise and TDMA noise is strongly recommended. When using a single-ended connection, be sure to have a very good ground plane, very good filtering as well as shielding in order to avoid any disturbance on the audio path.

The gain of MIC inputs is internally adjusted and can be tuned using an AT command.

Both can be configured in differential or single-ended.

The MIC2 inputs already include the biasing for an electret microphone allowing for an easy connection.

3.13.1.1. MIC1 Microphone Inputs

By default, MIC1 inputs are single-ended but can be configured in differential.

MIC1 inputs do not include an internal bias. The MIC1 input needs to have an external biasing if an electret microphone is used.

AC coupling is already embedded in the Q26 Extreme embedded module.

Table 34. Equivalent Circuits of MIC1

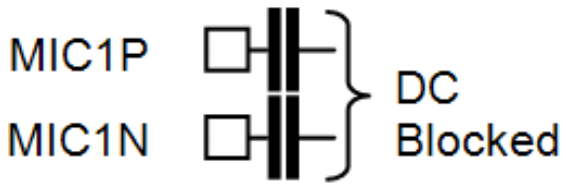
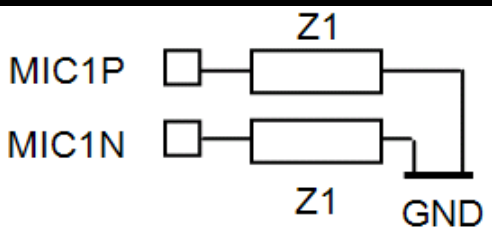
DC Equivalent Circuit	AC Equivalent Circuit
	

Table 35. Electrical Characteristics of MIC1

Parameters		Minimum	Typical	Maximum	Unit
DC Characteristics			N/A		V
AC Characteristics 200 Hz < F < 4 kHz	Z1	70	120	160	kΩ
Working voltage (MIC1P-MIC1N)	AT+VGT*=3500[1]		13.8	18.6**	mVrms
	AT+VGT*=2000[1]		77.5	104**	
	AT+VGT*=700[1]		346	465**	
Maximum rating	Positive			+7.35	V

Parameters		Minimum	Typical	Maximum	Unit
voltage (MIC1P or MIC1N)	Negative	-0.9			

* The input voltage depends of the input micro gain set by AT command. Please refer to document [5] Firmware v7.4 AT Commands Manual.

** This value is obtained with digital gain = 0 and for frequency = 1kHz.

1 This value is given in dB, but it's possible to toggle to index value. Please refer to document [5] Firmware v7.4 AT Commands Manual.

Warning: *The voltage input value for MIC1 can't exceed the maximum working voltage, otherwise clipping will appear.*

3.13.1.2. MIC1 Differential Connection Example

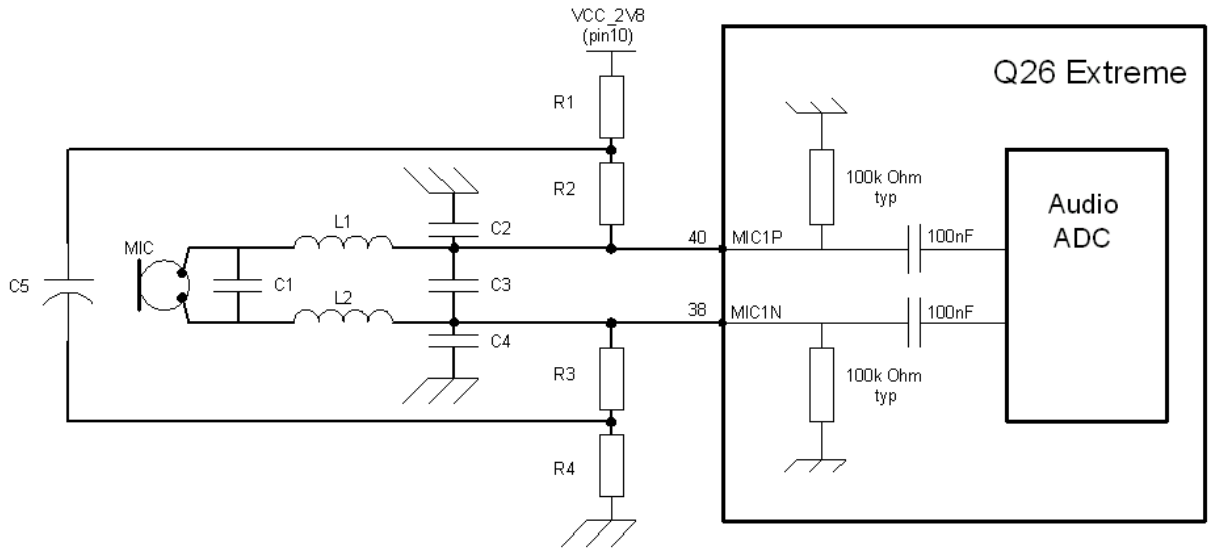


Figure 19. Example of MIC1 Input Differential Connection with LC Filter

Depending on the design, audio quality may be good without L1, L2, C2, C3, and C4. Moreover, if there is EMI perturbation, this filter may reduce TDMA noise. The filter (L1, L2, C2, C3, and C4) is not mandatory. If this filter is not used, then the capacitor must be removed and the coil replaced with 0Ω resistors, as shown in the following diagram.

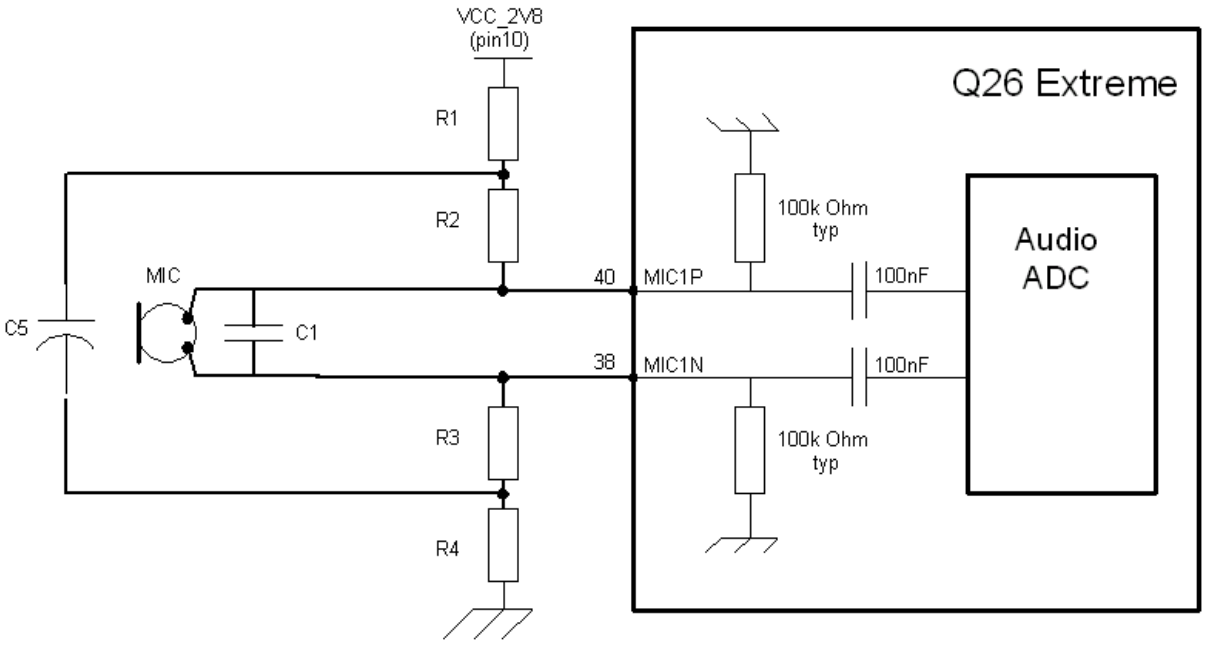


Figure 20. Example of MIC1 Input Differential Connection without LC Filter

Capacitor C1 is highly recommended to eliminate TDMA noise. C1 must be close to the microphone.

Vbias may be VCC_2V8 (pin 10) of the Q26 Extreme embedded module, but it is possible to use another 2 volts to 3 volts supply voltage depending on the microphone characteristics.

Caution: *If an external supply is used other than VCC_2V8 (pin 10), it is important to make sure that the voltage is clean and free from noise; otherwise, the audio quality will be degraded.*

3.13.1.2.1. Recommended Components

- R1: 4.7kΩ (for Vbias equal to 2.8V)
- R2, R3: 820Ω
- R4: 1Ω
- C1: 12pF to 33pF (needs to be tuned depending on the design)
- C2, C3, C4: 47pF (needs to be tuned depending on the design)
- C5: 2.2µF +/- 10%
- L1, L2: 100nH (needs to be tuned depending on the design)

3.13.1.3. MIC1 Single-Ended Connection Example

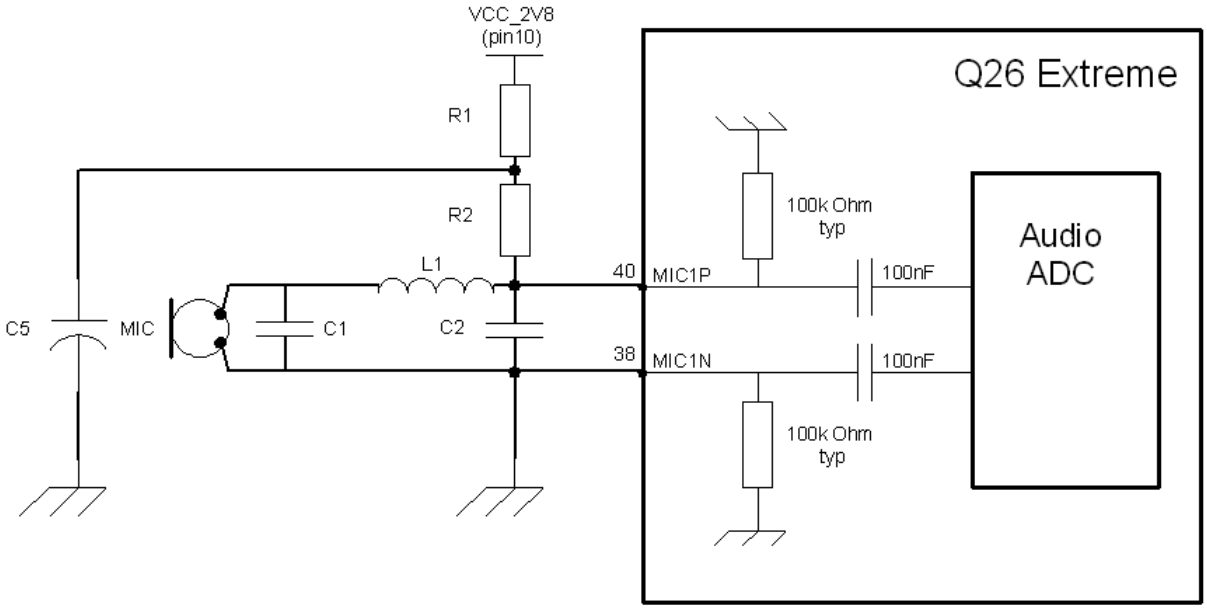


Figure 21. Example of MIC1 Input Single-Ended Connection with LC Filter

The single-ended design is not recommended to improve TDMA noise rejection. Usually, it is difficult to eliminate TDMA noise from a single-ended design.

It is recommended to add L1 and C2 footprint and an LC EMI filter in order to eliminate TDMA noise.

When not used, the filter may be removed by replacing L1 with a 0Ω resistor and by disconnecting C2, as shown in the following diagram.

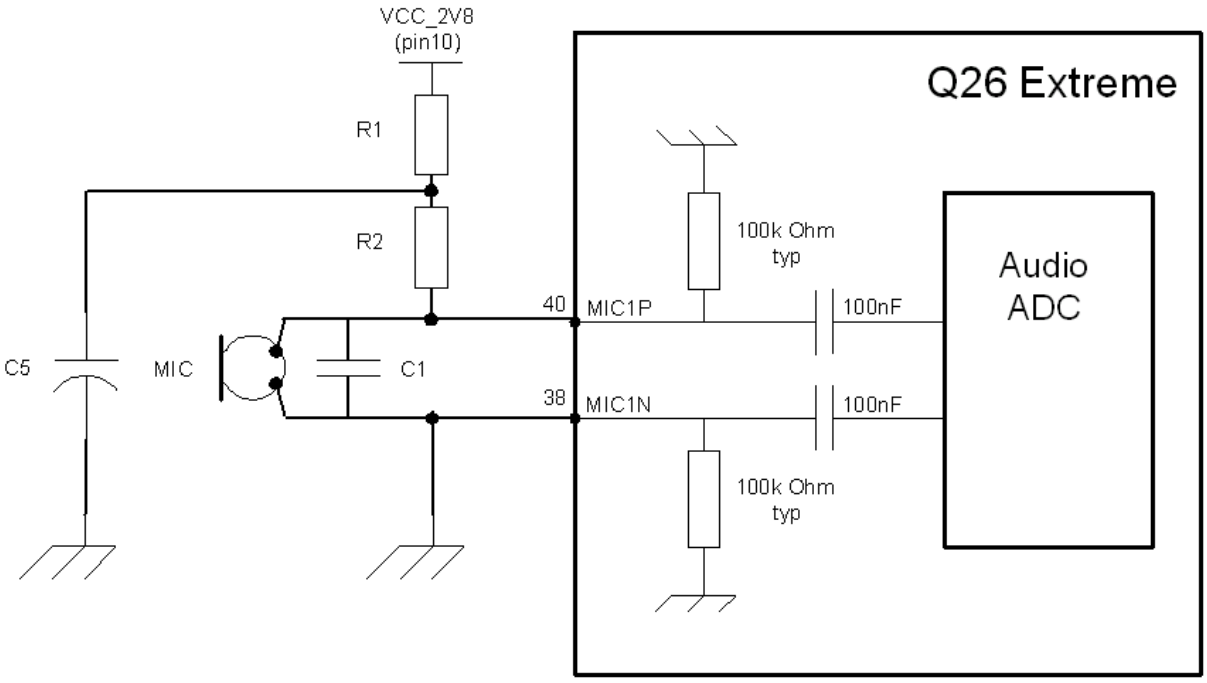


Figure 22. Example of MIC1 Input Single-Ended Connection without LC Filter

3.13.1.3.1. Recommended Components

- R1: 4.7kΩ (for Vbias equal to 2.8V)
- R2: 820Ω
- C1: 12pF to 33pF (needs to be tuned depending on the design)
- C2: needs to be tuned depending on the design
- L1: needs to be tuned depending on the design

Vbias must be very "clean" to avoid bad performance in case of a single-ended implementation. It is highly recommended to use the VCC_2V8 supply which is available on the system connector (pin 10), in order to avoid this problem.

The capacitor C1 is highly recommended to eliminate the TDMA noise. C1 must be close to the microphone.

3.13.1.4. MIC2 Microphone Inputs

By default, the MIC2 inputs are differential, but can be configured in single-ended. They already include the convenient biasing for an electret microphone. The electret microphone can be directly connected on these inputs, thus allowing easy connection to a handset.

AC coupling is already embedded in the module.

Table 36. Equivalent Circuits of MIC2

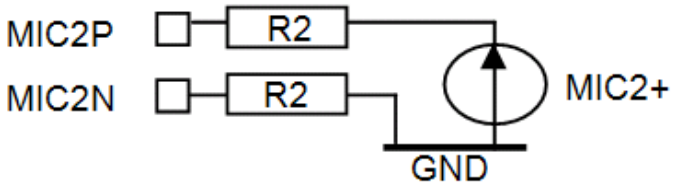
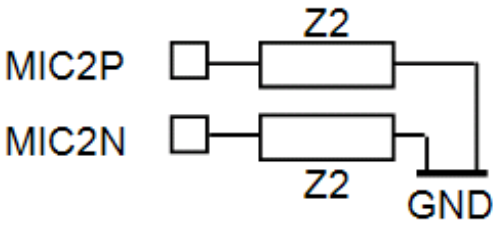
DC Equivalent Circuit	AC Equivalent Circuit
	

Table 37. Electrical Characteristics of MIC2

Parameters		Minimum	Typical	Maximum	Unit
Internal biasing DC Characteristics	MIC2+	2	2.1	2.2	V
	Output current		0.5	1.5	mA
	R2	1650	1900	2150	Ω
AC Characteristics 200 Hz<F<4 kHz	Z2 MIC2P (MIC2N=Open)	1.1	1.3	1.6	kΩ
	Z2 MIC2N (MIC2P=Open)				
	Z2 MIC2P (MIC2N=GND)	0.9	1.1	1.4	
	Z2 MIC2N (MIC2P=GND)				
	Impedance between MIC2P and MIC2N	1.3	1.6	2	
Working voltage	AT+VGT*=3500[1]		13.8	18.6 ***	mVrms

Parameters		Minimum	Typical	Maximum	Unit
(MIC2P-MIC2N)	AT+VGT*=2000[1]		77.5	104***	
	AT+VGT*=700[1]		346	466***	
Maximum rating voltage (MIC2P or MIC2N)	Positive			+7.35**	V
	Negative	-0.9			

* The input voltage depends of the input micro gain set by AT command. Please refer to document [5] Firmware v7.4 AT Commands Manual.

** Because MIC2P is internally biased, it is necessary to use a coupling capacitor to connect an audio signal provided by an active generator. Only a passive microphone can be directly connected to the MIC2P and MIC2N inputs.

*** This value is obtained with digital gain = 0 and for frequency = 1kHz.

1 This value is given in dB, but it's possible to toggle to index value. Please refer to document [5] Firmware v7.4 AT Commands Manual.

Warning: *The voltage input value for MIC2 can't exceed the maximum working voltage, otherwise clipping will appear.*

3.13.1.5. MIC2 Differential Connection Example

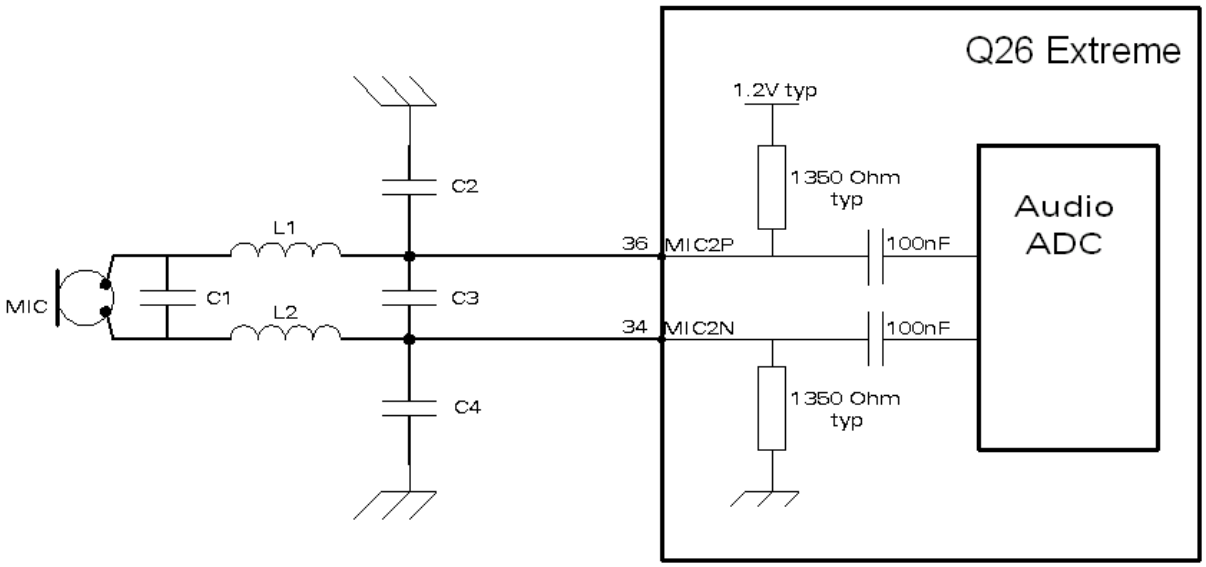


Figure 23. Example of MIC2 Input Differential Connection with LC Filter

Depending on the design, the audio quality may be good without L1, L2, C2, C3, and C4. Moreover, if there is EMI perturbation, this filter may reduce TDMA noise. The filter (L1, L2, C2, C3, and C4) is not mandatory. If this filter is not used, then the capacitor must be removed and the coil replaced with 0Ω resistors, as shown in the following diagram.

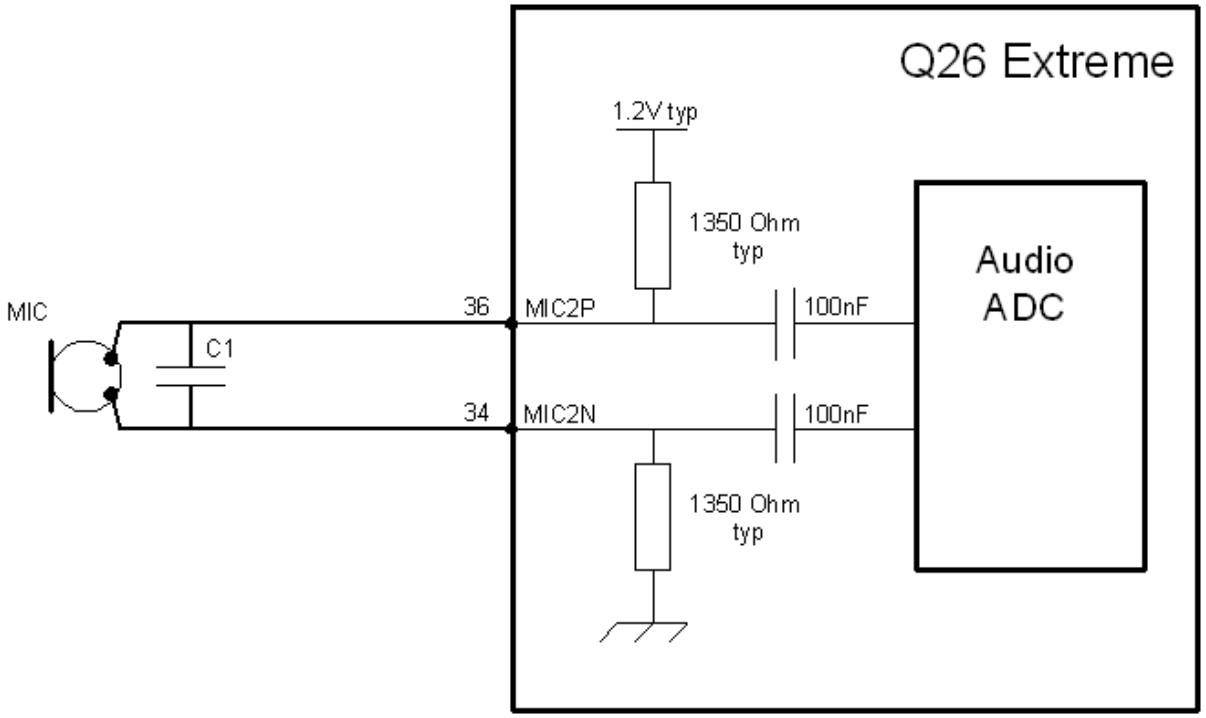


Figure 24. Example of MIC2 Input Differential Connection without LC Filter

Capacitor C1 is highly recommended to eliminate TDMA noise. C1 must be close to the microphone.

3.13.1.5.1. Recommended Components

- C1: 12pF to 33pF (needs to be tuned depending on the design)
- C2, C3, C4: 47pF (needs to be tuned depending on the design)
- L1, L2: 100nH (needs to be tuned depending on the design)

3.13.1.6. MIC2 Single-Ended Connection Example

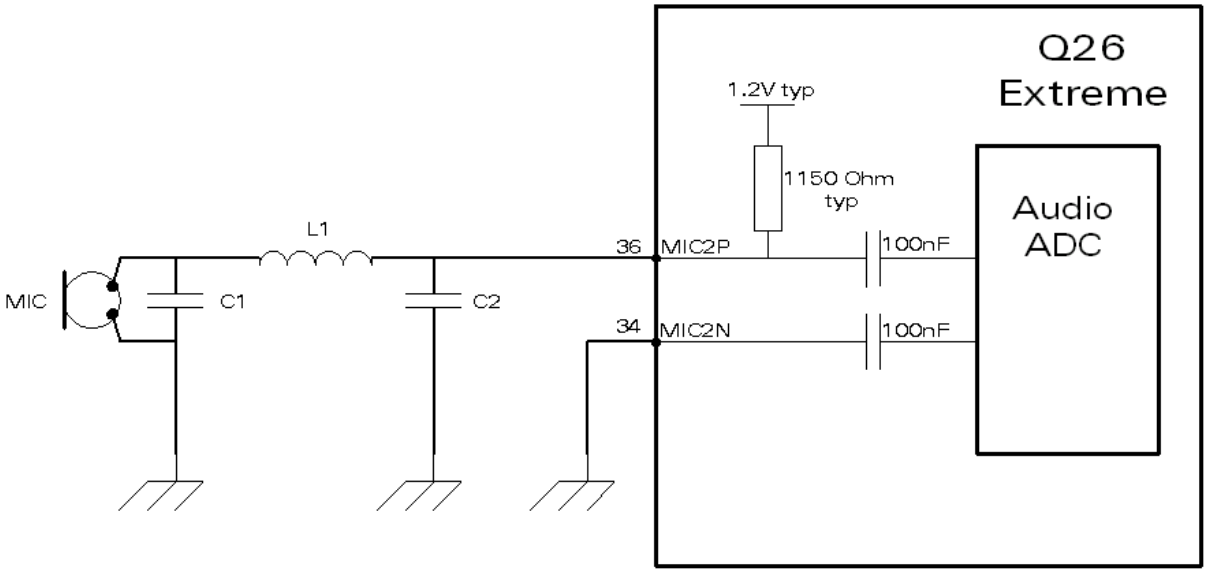


Figure 25. Example of MIC2 Input Single-Ended Connection with LC Filter

The internal input resistor value becomes 1150Ω, due to the connection of MIC2N to the ground plane.

The single-ended design is not recommended to improve TDMA noise rejection. Usually, it is difficult to eliminate TDMA noise from a single-ended design.

It is recommended to add L1, C2 footprint and an LC filter, in order to eliminate TDMA noise.

When not used, the filter can be removed by replacing L1 with a 0Ω resistor and by disconnecting C2, as shown in the following diagram.

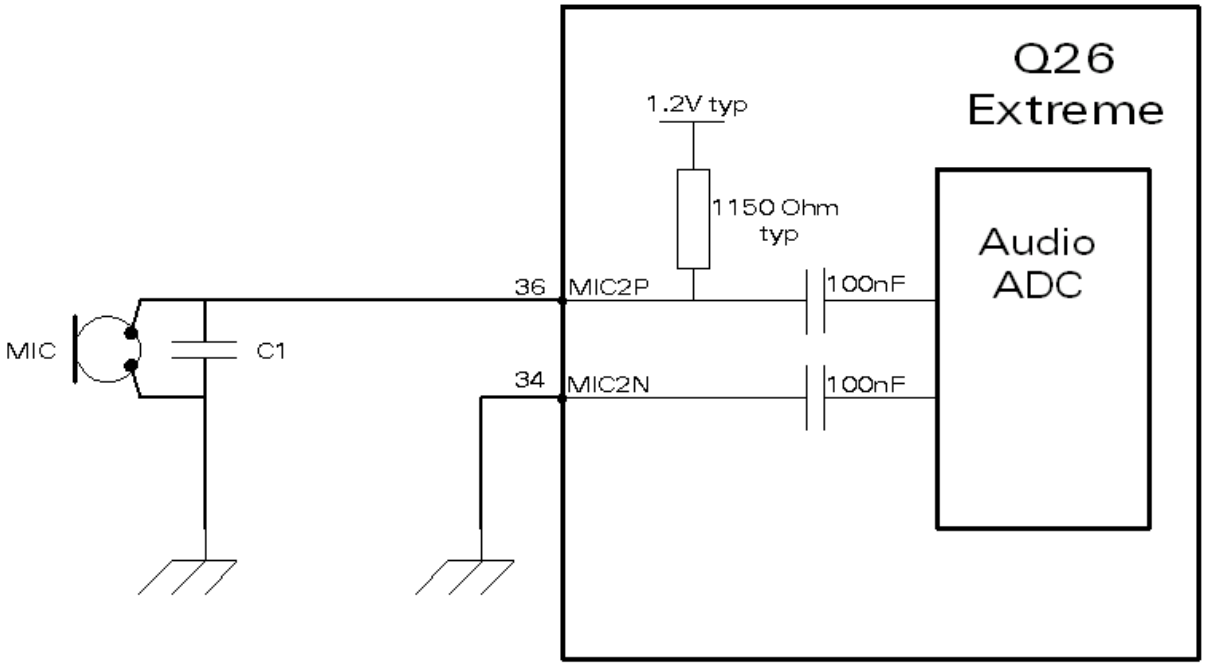


Figure 26. Example of MIC2 Input Single-Ended Connection without LC Filter

Capacitor C1 is highly recommended to eliminate the TDMA noise. C1 must be close to the microphone.

3.13.1.6.1. Recommended Components

- C1: 12pF to 33pF (needs to be tuned depending on the design)
- C2: needs to be tuned depending on the design
- L1: needs to be tuned depending on the design

3.13.2. Speaker Features

The connection is single-ended on SPK1 and differential or single-ended on SPK2. Using a differential connection to reject common mode noise and TDMA noise is strongly recommended. Moreover, in single-ended mode, the power is divided by 4. When using a single-ended connection, be sure to have a very good ground plane, very good filtering as well as shielding in order to avoid any disturbance on the audio path.

Table 38. Speaker Information

Parameter	Typical	Unit	Connection
Z (SPK1P, SPK1N)	16 or 32	Ω	Single-ended mode

Parameter	Typical	Unit	Connection
Z (SPK2P, SPK2N)	4	Ω	Single-ended mode
Z (SPK2P, SPK2N)	8	Ω	Differential mode

3.13.2.1. Speakers Outputs Power

The maximum power outputs of both speakers are not similar, due to the different configuration between SPK1 which is only single-ended, and SPK2 which can be either differential or single-ended – so SPK2 can provide more power.

The maximal specifications given below are available with the maximum power output configuration values set by an AT command. The typical values are recommended.

3.13.2.2. SPK1 Speaker Outputs

With the SPK1 interface, only single-ended speaker connection is allowed.

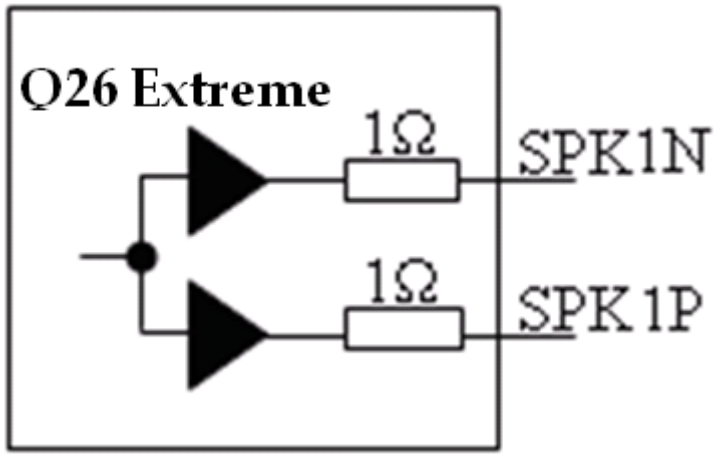


Figure 27. Equivalent Circuits of SPK1

Table 39. Electrical Characteristics of SPK1

Parameters			Minimum	Typical	Maximum	Unit
Biasing voltage	-			1.30		V
Output swing voltage	RL=16Ω: AT+VGR=-1600**; single-ended		-	1.7	-	Vpp
	RL=32Ω; AT+VGR=-1600**; single-ended		-	1.9	2.75	Vpp
RL	Load resistance		14.5	32	-	Ω
IOUT	Output current; single-ended; peak value	RL=16Ω	-	40	85	mA
		RL=32Ω	-	22	-	mA
POUT	RL=16Ω; AT+VGR*=-1600**		-	25		mW
	RL=32Ω; AT+VGR*=-1600**		-	16	27	mW
RPD	Output pull-down resistance at power-down		28	40	52	kΩ

* The output voltage depends of the output speaker gain set by AT command. Please refer to document [5] Firmware v7.4 AT Commands Manual.

** This value is given in dB, but it's possible to toggle to index value. Please refer to document [5] Firmware v7.4 AT Commands Manual.

3.13.2.3. SPK2 Speaker Outputs

The SPK2 interface allows both differential and single-ended speaker connection.

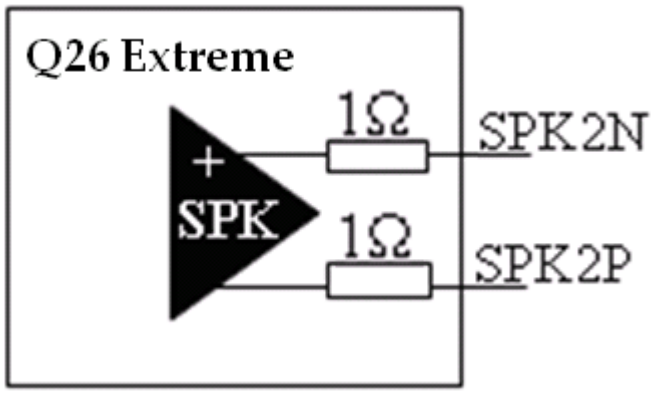


Figure 28. Equivalent Circuits of SPK2

Table 40. Electrical Characteristics of SPK2

Parameters		Minimum	Typical	Maximum	Unit
Biasing voltage	SPK2P and SPK2N		1.30		V
Output swing voltage	RL=8Ω: AT+VGR=-1000*; single ended	-	-	2	Vpp
	RL=8Ω: AT+VGR=-1000*; differential	-	-	4	Vpp
	RL=32Ω: AT+VGR=-1000*; single ended	-	-	2.5	Vpp
	RL=32Ω: AT+VGR=-1000*; differential	-	-	5	Vpp
RL	Load resistance	6	8	-	Ω
IOUT	Output current; peak value; RL=8Ω	-	-	180	mA
POUT	RL=8Ω; AT+VGR=-1000*;	-	-	250	mW
RPD	Output pull-down resistance at power-down	28	40	52	kΩ
VPD	Output DC voltage at power-down	-	-	100	mV

* The output voltage depends of the output speaker gain set by AT command. Please refer document [5] Firmware v7.4 AT Commands Manual. This value is given in dB, but it's possible to toggle to index value.

If a singled-ended solution is used with the SPK2 output, only one of either SPK2 has to be chosen. The result is a maximal output power divided by 4.

3.13.2.4. Differential Connection

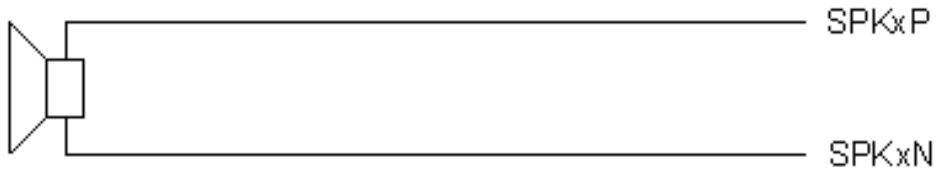


Figure 29. Example of Speaker Differential Connection

The impedance of the speaker amplifier output in differential mode is: **R ≤ 1Ω +/-10 %**.

The connection between the embedded module pins and the speaker must be designed in order to keep the serial impedance lower than 3Ω in differential mode.

3.13.2.5. Single-Ended Connection

A typical implementation is shown below:

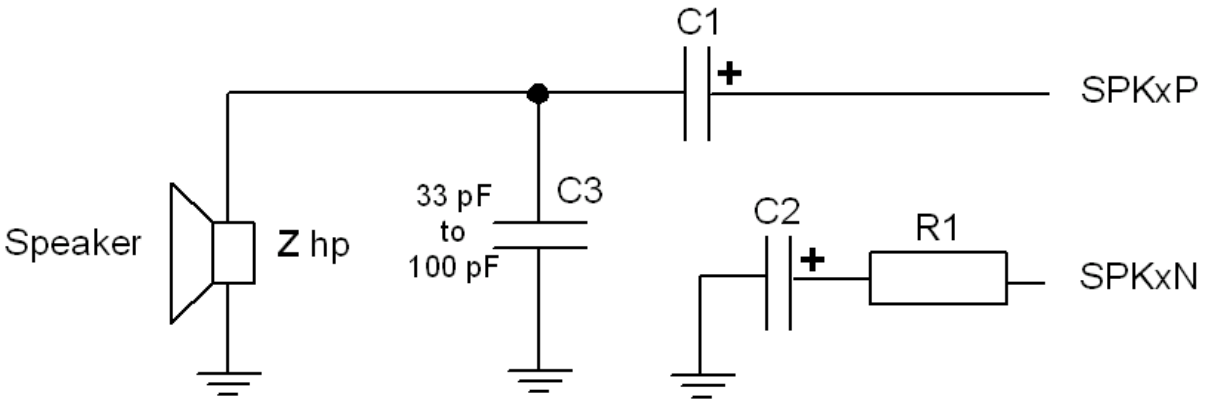


Figure 30. Example of Speaker Single-Ended Connection

Take note of the following when connecting the speaker in single-ended mode:

- 6.8µF < C1 < 47µF (depends on speaker characteristics and output power)
- C1 = C2
- R1 = Zhp
- Use of a single-ended connection results in output power loss (-6dB) when compared to a differential connection.

Nevertheless, in a 32Ω speaker case, you should use a cheaper and smaller solution where R1 = 82Ω and C2 = 6.8µF (ceramic).

The connection between the embedded module pins and the speaker must be designed in order to keep the serial impedance lower than 1.5Ω in differential mode.

When SPK1 channel is used, only SPK1P is useful, SPK1N may be left open.

3.13.2.6. Recommended Characteristics for the Speaker

- Type: 10mW, electro-magnetic
- Impedance
  - Z = 8Ω for hands-free (SPK2)
  - Z = 32Ω for headset kit (SPK1)
- Sensitivity: 110 dB SPL minimum (0 dB = 20µPa)
- Frequency response compatible with the GSM specifications

3.13.3. Pin Description

Table 41. Analog Audio Interface Pin Description

Signal	Pin #	I/O	I/O Type	Description
MIC1P	40	I	Analog	Microphone 1 positive input
MIC1N	38	I	Analog	Microphone 1 negative input
MIC2P	36	I	Analog	Microphone 2 positive input
MIC2N	34	I	Analog	Microphone 2 negative input
SPK1P	35	O	Analog	Speaker 1 positive output
SPK1N	37	O	Analog	Speaker 1 negative output
SPK2P	39	O	Analog	Speaker 2 positive output
SPK2N	41	O	Analog	Speaker 2 negative output

3.14. Buzzer Output

This output is controlled by a pulse width modulation controller and may only be used as a buzzer.

BUZZER0 is an open drain output. A buzzer can be directly connected between this output and VBATT. The maximum current is 100mA (PEAK).

Table 42. Buzzer Output Pin Description

Signal	Pin #	I/O	I/O Type	Reset State	Description
BUZZER0	15	O	Open drain	Z	Buzzer output

Refer to section 3.3 Electrical Information for Digital I/O for open drain, 2V8 and 1V8 voltage characteristics, and reset state definitions.

Table 43. Electrical Characteristics of the Buzzer Output

Parameter	Condition	Minimum	Minimum	Unit
$V_{OL\ on}$	Iol = 100mA		0.4	V
I_{PEAK}	VBATT = VBATTmax		100	mA
Frequency		1	50000	Hz

The maximum peak current is 80mA and the maximum average current is 40mA. A diode against transient peak voltage must be added as described below.

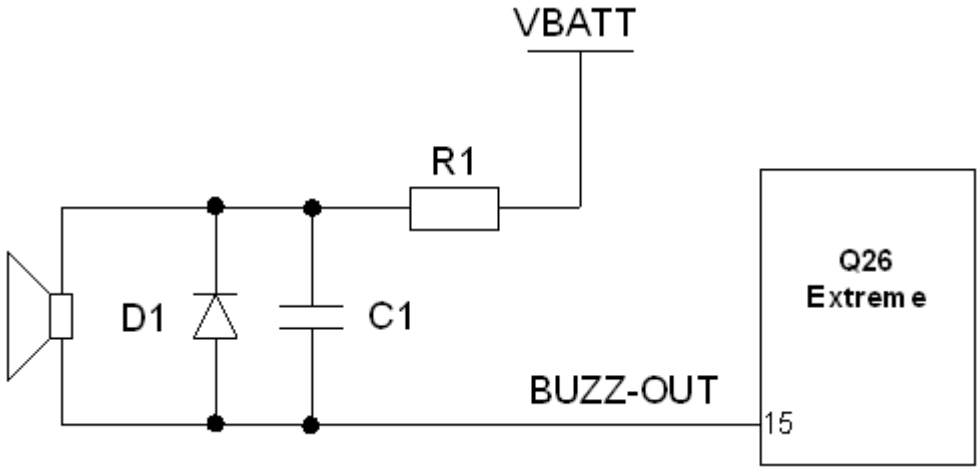


Figure 31. Example of BUZZER Implementation

Where:

- R1 must be selected in order to limit the current at I_{PEAK} max
- C1 = 0 to 100nF (depends on the buzzer type)
- D1 = BAS16 (for example)

3.14.1. Recommended Characteristics

- Electro-magnetic type
- Impedance: 7 to 30Ω
- Sensitivity: 90dB SPL min @ 10cm
- Current: 60 to 90mA

The BUZZ-OUT output may also be used to drive a LED as shown in the following figure.

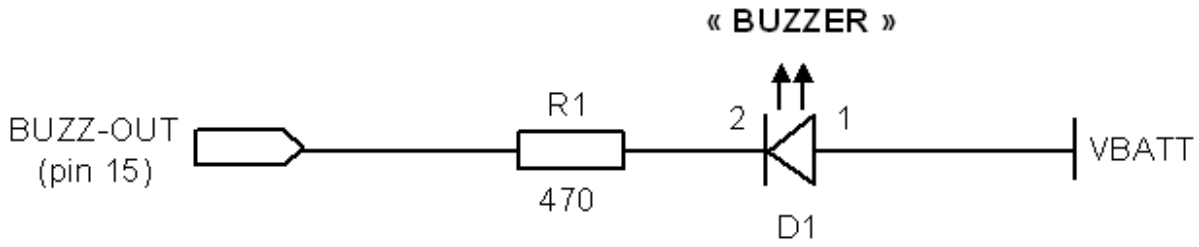


Figure 32. Example of LED Driven by the BUZZ-OUT Output

The value of R1 depends on the LED (D1) characteristics.

3.15. Battery Charging Interface

The Q26 Extreme embedded module supports one battery charging circuit, two algorithms and one hardware charging mode (pre-charging) for 3 battery technologies:

- Ni-Cd (Nickel-Cadmium) with algorithm 0
- Ni-Mh (Nickel-Metal Hydride) with algorithm 0
- Li-Ion (Lithium-Ion) with the embedded PCM (Protection Circuit Module) algorithm 1

The two algorithms control a switch, which connects the CHG-IN signal to the VBATT signal. The algorithm controls the frequency and the connected time of the switching. During the charging procedure, battery charging level is monitored and when the Li-Ion algorithm is used, battery temperature is monitored via the ADC1/BAT-TEMP input.

One more charging procedure is provided by the Q26 Extreme embedded module. This is called "Pre-charging" mode. It is a special charging mode because it is activated only when the embedded module is OFF. Control in this case is only performed by the hardware. The purpose of this charging mode is to avoid battery damage by preventing the battery from being discharged to below the minimum battery level.

3.15.1. Synopsis

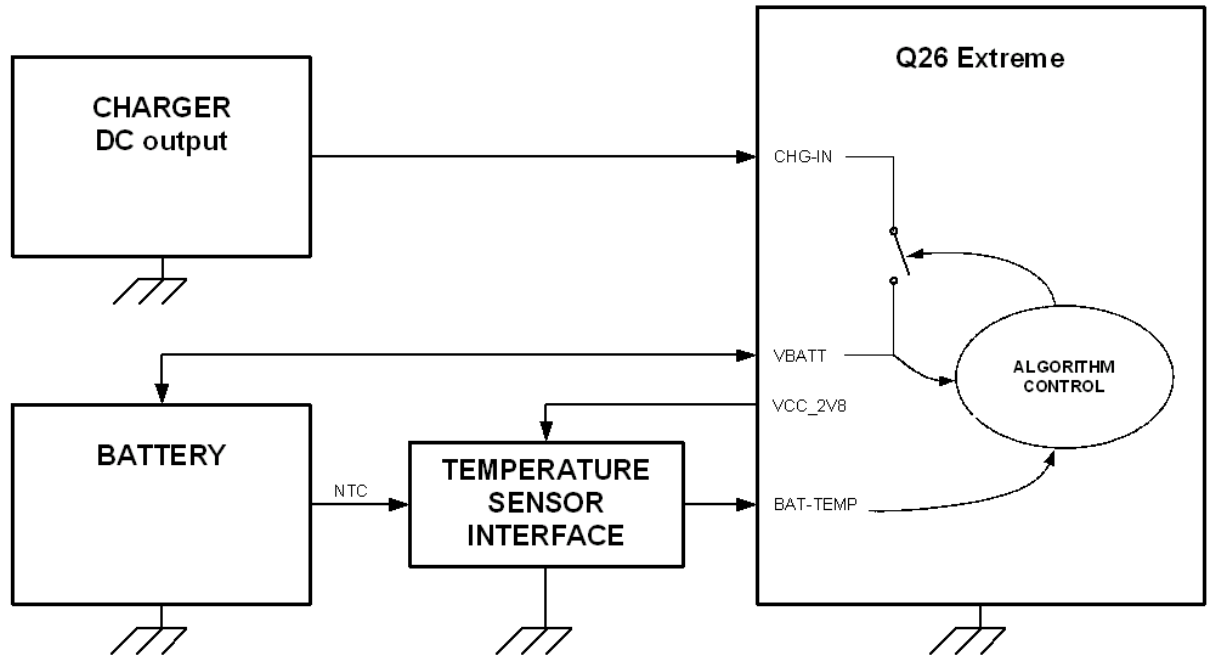


Figure 33. Synoptic of Battery Charging

The Q26 Extreme embedded module charging circuit is composed of a transistor switch (between CHG-IN pins 6, 8 and VBATT pins 1, 2, 3, 4). Charging is controlled by 2 software algorithms.

A dedicated ADC input BAT-TEMP (pin 20) for temperature monitoring (only for Li-Ion battery technology) is also available.

To use the charging functionality, 3 hardware items are required:

- Charger power supply
  - It provides a DC current power supply limited to 800mA and with voltage range, according to the battery choice and to the Q26 Extreme embedded module specification.
- Battery
  - The charging functionality must be used with rechargeable batteries only. Three battery types are supported: Li-Ion, Ni-Mh and Ni-Cd.
  - If the Q26 Extreme embedded module is not powered (VBATT pins 1, 2, 3, 4) by a rechargeable battery, it is mandatory to leave the CHG-IN input (pin 6, 8) open.
- Analog temperature sensor
  - The analog temperature sensor is only used for Li-Ion batteries to monitor the battery temperature. This sensor is composed of an NTC sensor and several resistors.

3.15.2. Charger Recommendations

The following table defines and specifies the AC/DC adapter for a battery cell.

Table 44. Charger Recommendations

Parameter	Minimum	Typical	Maximum	Unit	Remark
Input voltage	90		265	Vac	
Input frequency	45		65	Hz	
Output voltage limit			6	V	No load
Output voltage limit	4.6			V	Io max
Output current	*	1C**	***	mA	
Output Voltage Ripple			150	mVpp	Io max
					Vout=5.3V

* See the cell battery specifications for conditions of current charging.

** 1C = Nominal capacity (of the battery cell).

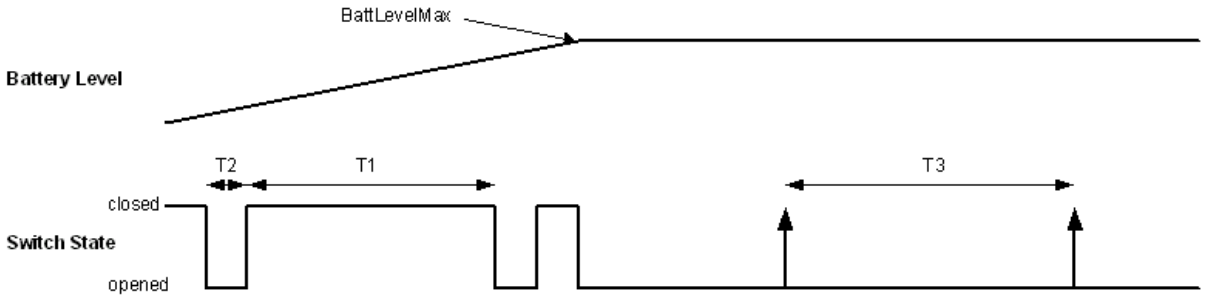
*** See the cell battery specifications for conditions of current charging.

Sierra Wireless recommends that the output voltage (Vo) fall under 1.18V in less than 1 second when the adapter AC/DC is unplugged.

3.15.3. Charging Algorithm

3.15.3.1. Ni-Cd/Ni-Mh Charging Algorithm

To charge the battery, the algorithm measures battery level when the switch is open (time T2) and charges the battery by closing the switch (time T1). When the battery is charged (battery voltage has reached BattLevelMax) the switch is open for time T3.



T1 : Charging pulse duration 1sec
T2 : TPulseINCharge Time between charging pulses
T3 : TPulseOutCharge Time between Battery Monitoring events (Battery charged)

Figure 34. Ni-Cd/Ni-Mh Charging Waveform

Table 45. Electrical Characteristics of Ni-Cd/Ni-Mh Battery Timing Charge

Parameter	Minimum	Typical	Maximum	Unit
T1		1		s
T2		0.1		s
T3		5		s

Note: T1, T2, T3 and BattLevelMax may be configured by AT command.

The battery level is monitored by the software (but not the temperature).

The Li-Ion algorithm provides battery temperature monitoring, which is highly recommended to prevent battery damage during the charging phase.

3.15.3.2. Li-Ion Charging Algorithm

The Li-Ion charger algorithm can be broken down into three phases:

1. Constant charge
2. Beginning of pulse charge
3. End of pulse charge

The three phases can be seen on the following waveform for full charging:

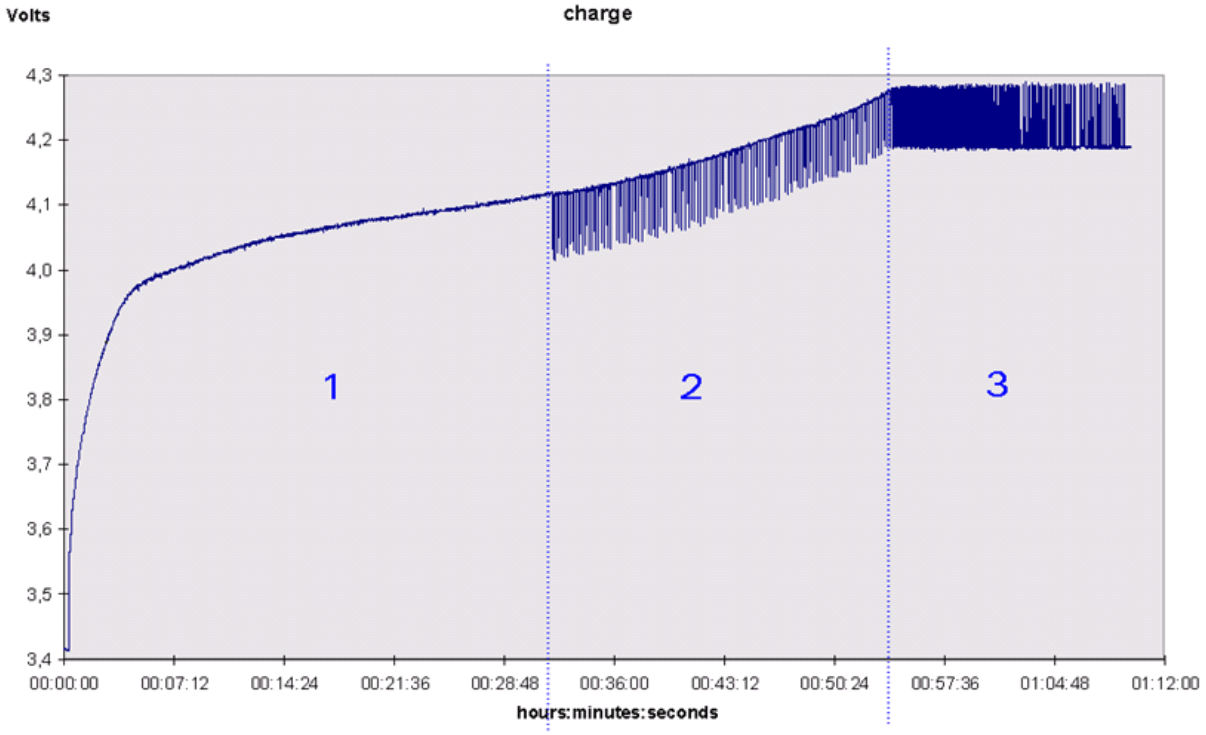


Figure 35. Li-Ion Full Charging Waveform

Table 46. Electrical Characteristics of Li-Ion Battery Timing Charge

Parameter		Minimum	Typical	Maximum	Unit
Step 1 switching	Closed		Always		s
Step 2 switching	Open		0.1		s
	Closed		1		s
Step 3 switching	Open	0.1		3	s
	Closed		1		s

3.15.4. Pre-Charging

When a charger DC power supply is connected to the CHG-IN input and if the voltage battery is between 2.8V* and 3.2V, a constant current of 50mA is provided to the battery.

When the battery is able to supply the Q26 Extreme embedded module, it is automatically powered on and the software algorithm is activated to finish the charge.

*Note: * For the Lithium-Ion battery, the minimum voltage must be higher than the PCM lock level.*

When pre-charging is launched, the LED0 output blinks automatically.

Warning: *The Q26 Extreme embedded module can not release the PCM protection inside Lithium battery pack. Voltage is forbidden on the CHG-IN signal if no battery is connected on the VBATT signals.*

3.15.5. Temperature Monitoring

Temperature monitoring is only available for the Li-Ion battery with algorithm 1. The ADC1/BAT-TEMP (pin 20) input must be used to sample the temperature analog signal provided by an NTC temperature sensor. The minimum and maximum temperature range may be set by AT command.

Table 47. Battery Charging Interface Pin Description

Signal	Pin #	I/O	I/O Type	Description
CHG-IN	6, 8	I	Analog	Current source input
BAT-TEMP	20	I	Analog	A/D converter

Table 48. Electrical Characteristics of the Battery Charging Interface

Parameter		Minimum	Typical	Maximum	Unit
Charging operating temperature		0		50	°C
ADC1/BAT-TEMP (pin 20)	Maximum output code		1635		LSB
	Sampling rate		216		S/s
	Input Impedance (R)		1		MΩ
	Input signal range	0		2	V
CHG-IN (pin 6, 8)	Voltage (for I=Imax)	4.8*			V
	Voltage (for I=0)			6*	V
	DC Current	400**		800	mA

* To be configured as specified by the battery manufacturer.

** Take care as this value has to be selected in function of the power consumption mode used; please refer to the power consumption table in section 3.2.2 Power Consumption.

3.15.5.1. Schematic

The VCC_2V8 (pin 10) voltage provided by the Q26 Extreme embedded module may be used to polarize the NTC. However, the additional resistors R1 and R2 must be used to adjust the maximum voltage of the ADC input to 2 volts.

If any other polarized voltage is used, the resistors must be adapted.

It is not recommended to use the VCC_1V8 (pin 5) voltage.

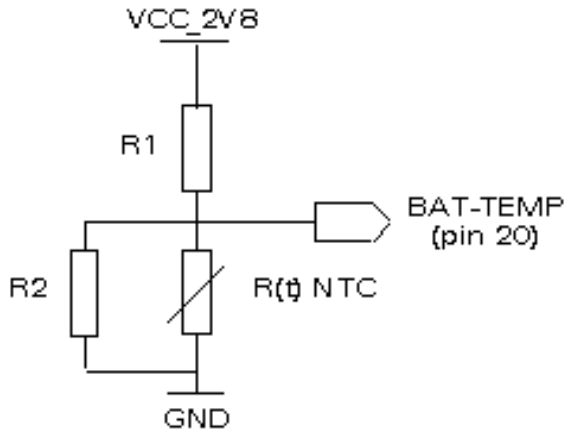


Figure 36. Example of ADC Application

The R(t) resistor is the NTC and must be close to the battery; it is usually integrated into the battery.

Warning: *The DC power supply charger must have an output current limited to 800mA.*

The maximum charger output current, provided to the battery, must be in accordance with the battery electrical characteristics.

Li-Ion batteries must be used with the embedded PCM (Protection Circuit Module).

The maximum charging voltage is up to 4.3V (software driven).

At the first plug, if the Li-ion battery is locked by its PCM, the charger function does not work.

3.16. ON/~OFF Signal

This input is used to switch the Q26 Extreme embedded module ON or OFF.

A high-level signal must be provided on the ON/~OFF pin to switch ON the embedded module. The voltage of this signal has to be maintained higher than 0.8 x VBATT for a minimum of 1500ms. This signal can be left at high level until switch-off.

To switch OFF the embedded module, the ON/OFF pin must be released. The embedded module can be switched off via the operating system.

Table 49. On/~OFF Signal Pin Description

Signal	Pin #	I/O	I/O Type	Description
ON/~OFF	19	I	CMOS	Embedded module Power-ON

Table 50. Electrical Characteristics of the ON/~OFF Signal

Parameter	I/O Type	Minimum	Minimum	Unit
V_{IL}	CMOS		VBATT x 0.2	V
V_{IH}	CMOS	VBATT x 0.8	VBATT	V

Warning: *All external signals must be inactive when the embedded module is OFF to avoid any damage when starting and to allow the embedded module to start and stop correctly.*

3.16.1. Operating Sequences

3.16.1.1. Power-ON

Once the embedded module is supplied, the application must set the ON/OFF signal to high to start the embedded module power-ON sequence. The ON/OFF signal must be held high during a minimum delay of $\mathbf{T_{on/off\text{-}hold}}$ (Minimum hold delay on the ON/~OFF signal) to power-ON. After this delay, an internal mechanism maintains the embedded module in power-ON condition.

During the power-ON sequence, an internal reset is automatically performed by the embedded module for 40ms (typical). Any external reset should be avoided during this phase.

Once initialization is completed (timing is USIM- and network-dependent), the AT interface answers "OK" to the application. For further details, please refer to document [5] Firmware v7.4 AT Commands Manual.

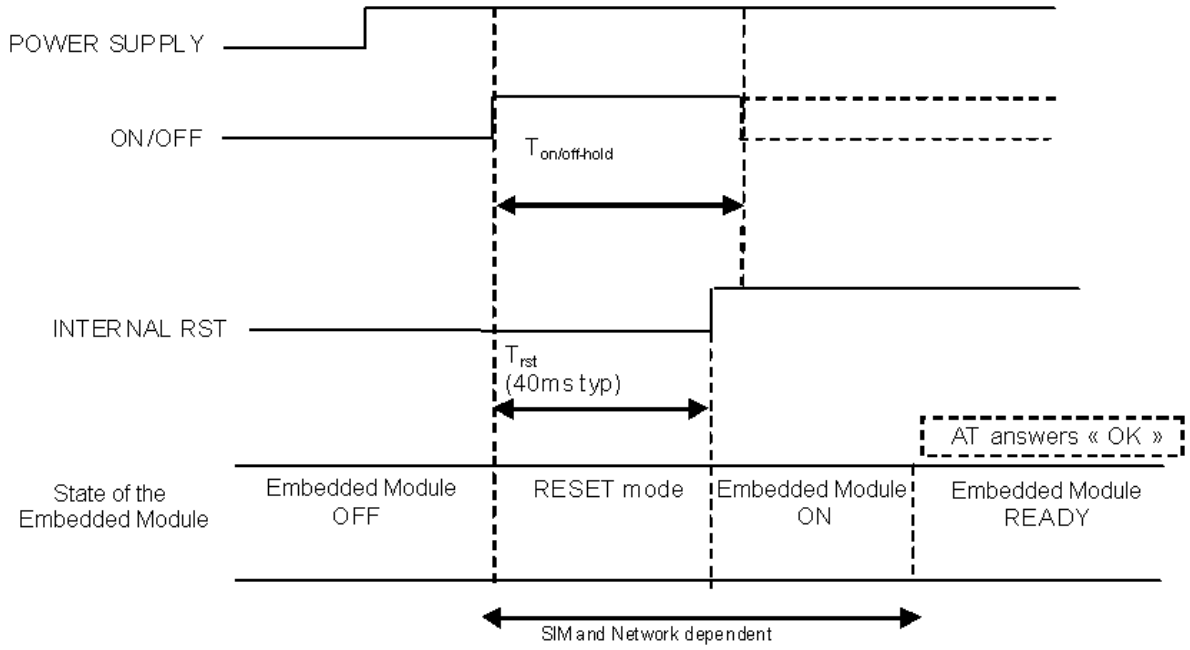


Figure 37. Power-ON Sequence (no PIN code activated)

The duration of the firmware power-up sequence depends on:

- the need to perform a recovery sequence if the power has been lost during a flash memory modification.

Other factors have a minor influence

- the number of parameters stored in EEPROM by the AT commands received so far
- the ageing of the hardware components, especially the flash memory
- the temperature conditions

The *recommended* way to de-assert the ON/~OFF signal is to use either an AT command or WIND indicators: the application must detect the end of the power-up initialization and de-assert ON/~OFF afterwards.

- Send an “AT” command and wait for the “OK” answer: once the initialization is complete the AT interface answers « OK » to “AT” message[1].
- Wait for the “+WIND: 3” message: after initialization, the embedded module, if configured to do so, will return an unsolicited “+WIND: 3” message. The generation of this message is enabled or disabled via an AT command.

Note: See also document [5] Firmware v7.4 AT Commands Manual for more information on these commands.

Proceeding thus – by software detection - will always prevent the application from de-asserting the ON/~OFF signal too early.

If WIND indicators are disabled or AT commands unavailable or not used, it is still possible to de-assert ON/~OFF after a delay long enough (**$T_{on/off-hold}$**) to ensure that the firmware has already completed its power-up initialization.

The table below gives the minimum values of **$T_{on/off-hold}$**:

1 If the application manages hardware flow control, the AT command can be sent during the initialization phase.

Table 51. $T_{on/off-hold}$ Minimum Values

Sierra Wireless Software Suite	$T_{on/off-hold}$ Safe Evaluations of the Firmware Power-Up Time
Sierra Wireless Software Suite 2.30	8s (TBC)

The above figure take the worst cases into account: power-loss recovery operations, slow flash memory operations in high temperature conditions, and so on. But, they are safe because they are large enough to ensure that ON/~OFF is not de-asserted too early.

3.16.1.2. Additional Notes

- Typical power-up initialization time figures for best case conditions (no power-loss recovery, fast and new flash memory) at approximately 3.5 seconds in every firmware version. But releasing ON/~OFF after this delay does not guarantee that the application will actually start-up if, for example, the power plug has been pulled off during a flash memory operation, like a phone book entry update or an AT&W command.
- The ON/~OFF signal can be left at a high level until switched OFF. But this is not recommended as it will prevent the **AT+CPOF** command from performing a clean power-off. (see also Note in section 3.16.1.3 Power-OFF for an alternate usage)
- When using a battery as power source, it is not recommended to let this signal high:
- If the battery voltage is too low and the ON/~OFF signal at low level, an internal mechanism switches OFF the embedded module. This automatic process prevents the battery to be over discharged and optimize its life span.
- During the power-ON sequence, an internal reset is automatically performed by the embedded module for 40 ms (typical). Any external reset should be avoided during this phase.

3.16.1.3. Power-OFF

To power-OFF the embedded module correctly, the application must reset the ON/OFF signal and then send the **AT+CPOF** command to deregister from the network and switch off the embedded module.

Once the "OK" response is issued by the embedded module, the power supply can be switched off.

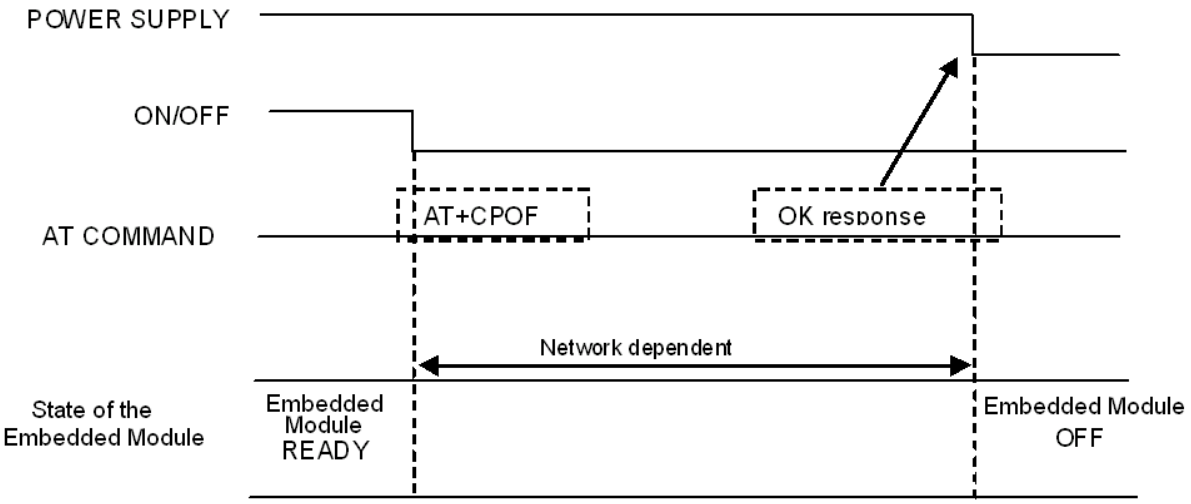


Figure 38. Power-OFF Sequence

Note: *If the ON/~OFF pin is maintained to ON (High Level), then the embedded module can't be switched OFF.*

Connecting a charger on the embedded module has exactly the same effect as setting the ON/~OFF signal. In particular, the embedded module will not POWER-OFF after the ***AT+CPOF*** *command, unless the charger is disconnected.*

3.17. BOOT Signal

A specific BOOT control pin is available to download to the Q26 Extreme embedded module only if the standard XModem download, controlled with AT command, is not possible.

A specific PC software program, provided by Sierra Wireless, is needed to perform this specific download.

The BOOT pin must be connected to VCC_1V8 for this specific download.

Table 52. Operating Mode Description

BOOT	Operating Mode	Comment
Leave open	Normal use	No download
Leave open	Download XModem	AT command for Download **AT+WDWL**
1	Download specific	Need Sierra Wireless PC software

For more information, see document [5] Firmware v7.4 AT Commands Manual.

This BOOT pin must be left open either for normal use or XModem download.

However, in order to render the development and maintenance phases easier, it is **highly recommended** to set a test point, either a jumper or a switch, on the VCC_1V8 (pin 5) power supply.

Table 53. BOOT Signal Pin Description

Signal	Pin #	I/O	I/O Type	Description
BOOT	16	I	1V8	Download mode selection

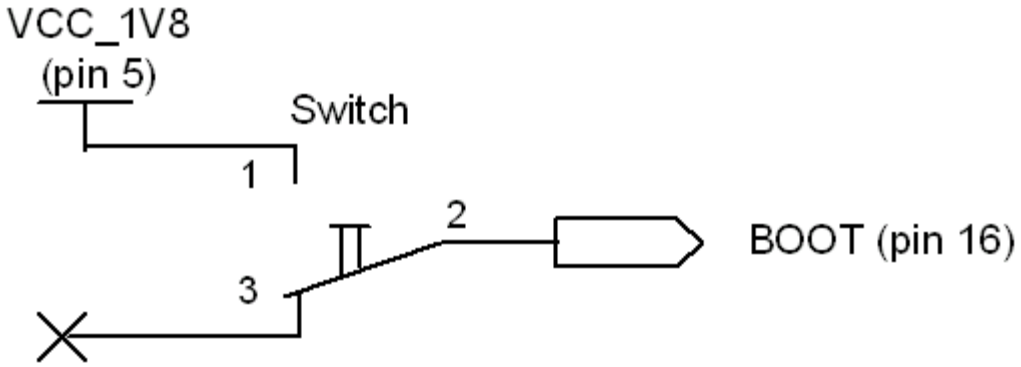


Figure 39. Example of BOOT Pin Implementation

3.18. Reset Signal (~RESET)

This signal is used to force a reset procedure by providing low level for at least 200µs. This signal must be considered as an emergency reset only. A reset procedure is already driven by the internal hardware during the power-up sequence.

This signal may also be used to provide a reset to an external device (at power-up only). If no external reset is necessary, this input may be left open. If used (emergency reset), it must be driven by an open collector or an open drain.

The embedded module remains in reset mode as long as the ~RESET signal is held low.

Caution: *This signal should only be used for "emergency" resets.*

An operating system reset is to be preferred to a hardware reset.

3.18.1. Reset Sequence

To activate the "emergency" reset sequence, the ~RESET signal must be set to low for 200µs minimum. As soon as the reset is completed, the AT interface answers "OK" to the application.

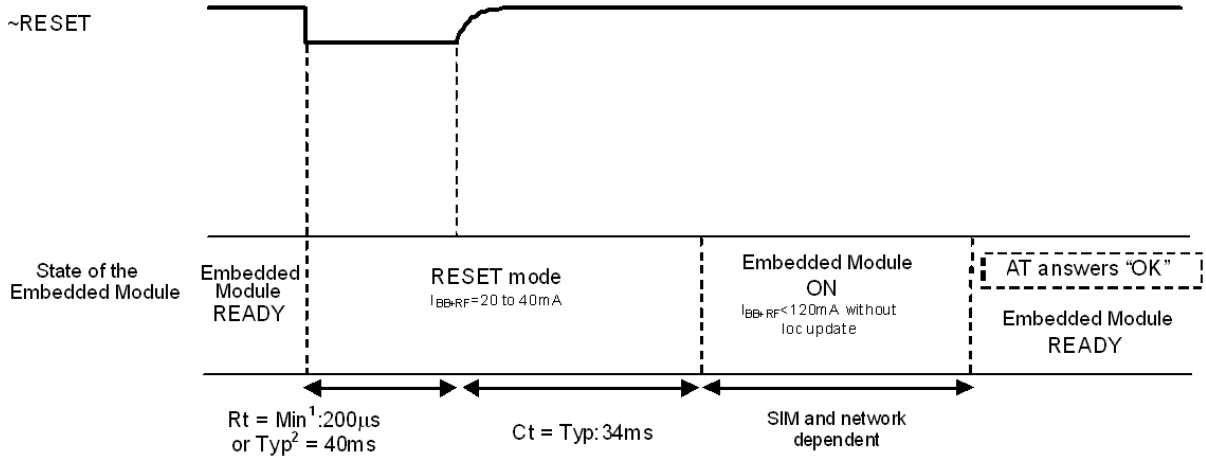


Figure 40. Reset Sequence Waveform

At power-up, the ~RESET time (Rt) is carried out after switching ON the embedded module. It is generated by the internal Q26 Extreme embedded module voltage supervisor.

The ~RESET time is provided by the internal RC component. To keep the same time, it is not recommended to connect another R or C component on the ~RESET signal. Only a switch or an open drain gate is recommended.

Ct is the cancellation time required for the Q26 Extreme embedded module initialization. Ct is automatically carried out by the Q26 Extreme embedded module after a hardware reset.

Table 54. Electrical Characteristics of the ~RESET Signal

Parameter	Minimum	Typical	Maximum	Unit
Input Impedance (R)*		100		kΩ
Input Impedance (C)		10		nF
~RESET time (Rt)[1]	200			µs
~RESET time (Rt)[2] at power up only	20	40	100	ms
Cancellation time (Ct)		34		ms
V_H**	0.57			V

Parameter	Minimum	Typical	Maximum	Unit
V_{IL}	0		0.57	V
V_{IH}	1.33			V

* Internal pull-up

** VH: Hysterisis Voltage

1 This reset time is the minimum time to be carried out on the ~RESET signal when the power supply is already stabilized.

2 This reset time is internally carried out by the embedded module power supply supervisor only when the embedded module power supplies are powered ON.

Table 55. RESET Signal Pin Description

Signal	Pin #	I/O	I/O Type	Description
~RESET	18	I/O Open Drain	1V8	Embedded module Reset

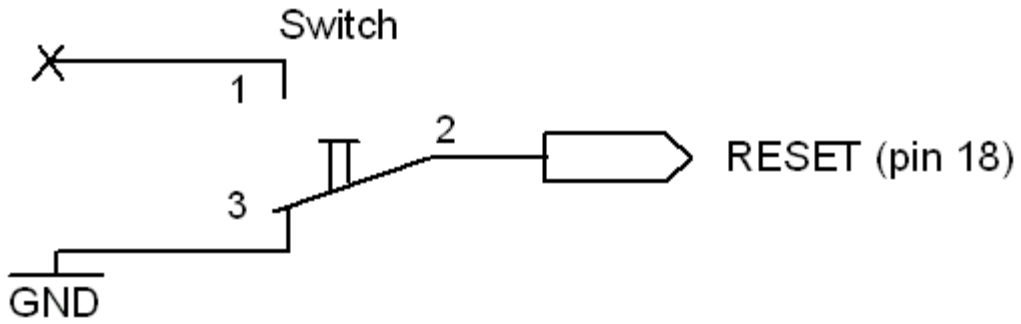


Figure 41. Example of ~RESET Pin Connection with Switch Configuration

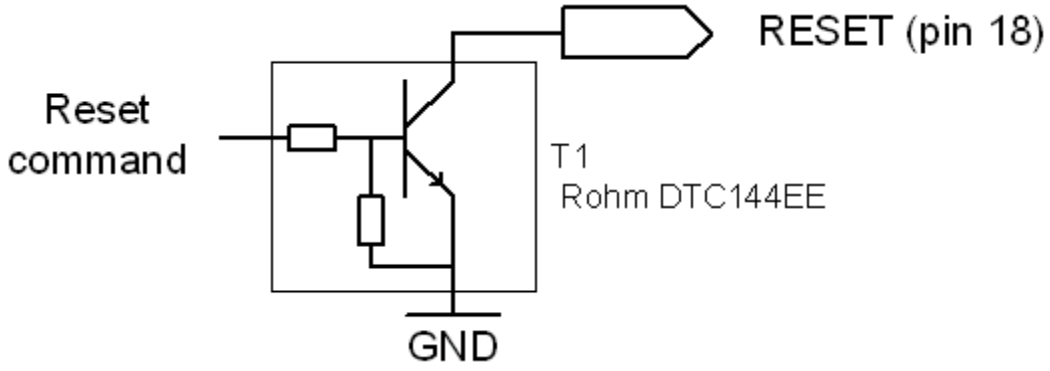


Figure 42. Example of ~RESET Pin Connection with Transistor Configuration

Open collector or open drain transistor may be used. If an open collector is selected, T1 may be a Rohm DTC144EE.

Table 56. Reset Command

Reset Command	~RESET (pin 18)	Operating Mode
1	0	Reset activated
0	1	Reset inactive

3.19. External Interrupt

The Q26 Extreme embedded module provides three external interrupt inputs. These interrupt inputs can be activated on:

- High to low edge
- Low to high edge
- Low to high and high to low edge

When used, the interrupt inputs must not be left open.

If not used, they must be configured as GPIOs.

Table 57. External Interrupt Pin Description

Signal	Pin #	I/O	I/O Type	Reset State	Description	Multiplexed with
INT2	51	I	1V8	Pull-up	External Interrupt 2	~CS2 / GPIO1
INT1	49	I	2V8	Z	External Interrupt 1	GPIO25
INT0	50	I	1V8	Z	External Interrupt 0	GPIO3

Refer to section 3.3 Electrical Information for Digital I/O for open drain, 2V8 and 1V8 voltage characteristics, and reset state definitions.

Table 58. Electrical Characteristics of the External Interrupt

Parameter		Minimum	Minimum	Unit
INT1	V_{IL}		0.84	V
	V_{IH}	1.96		V
INT0 , INT2	V_{IL}		0.54	V
	V_{IH}	1.33		V

3.20. VCC_2V8 and VCC_1V8 Output

These outputs may be used to power some external functions and only available when the embedded module is ON.

Table 59. VCC_2V8 and VCC_1V8 Output Pin Description

Signal	Pin #	I/O	I/O Type	Description
VCC_2V8	10	O	Supply	Digital supply
VCC_1V8	5	O	Supply	Digital supply

Table 60. Electrical Characteristics of the VCC_2V8 and VCC_1V8 Output

Parameter		Minimum	Typical	Maximum	Unit
VCC_2V8	Output voltage	2.74	2.8	2.86	V
	Output Current			15	mA
VCC_1V8	Output voltage	1.76	1.8	1.94	V
	Output Current			15	mA

These digital power supplies are mainly used to:

- Pull-up signals such as I/Os
- Supply the digital transistors driving the LEDs
- Supply the SIMPRES signal
- Act as a voltage reference for ADC interface AUX-ADC (only for VCC_2V8)

The maximum current to be provided by each output is 15mA.

3.21. BAT-RTC (Backup Battery)

The Q26 Extreme embedded module provides an input/output to connect a Real Time Clock (RTC) power supply.

3.21.1. Interface Description

This pin is used as a back-up power supply for the internal Real Time Clock. The RTC is supported by the embedded module when VBATT is available, but a back-up power supply is needed to save date and time when VBATT is switched off (VBATT = 0V).

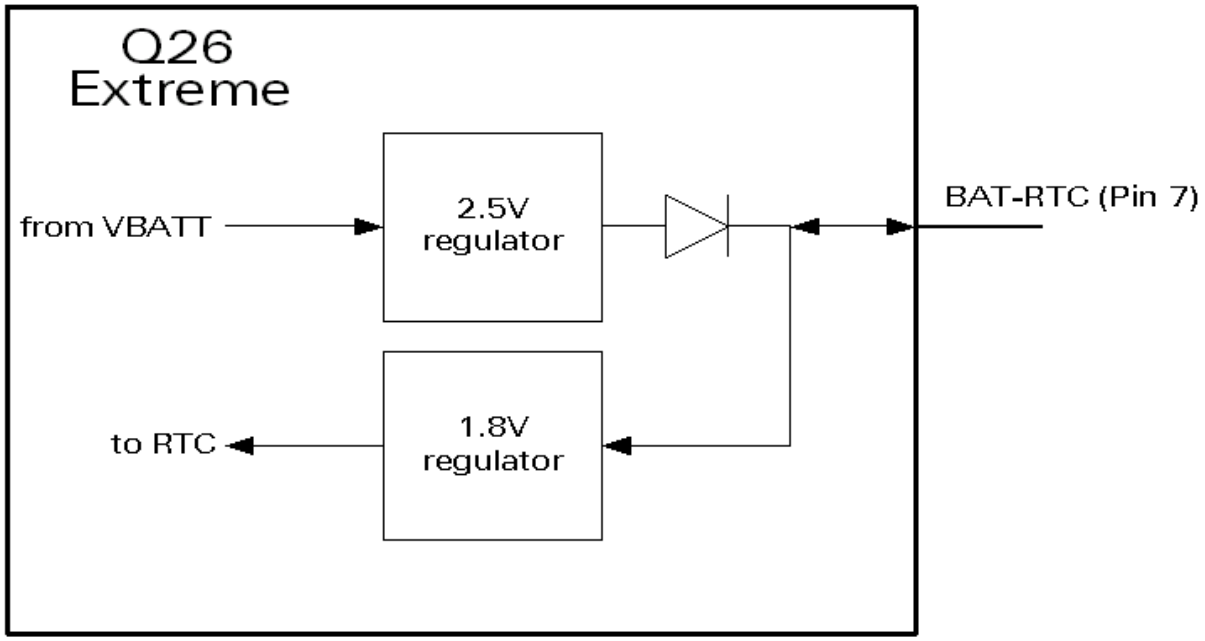


Figure 43. Real Time Clock Power Supply

If the RTC is not used, this pin can be left open.

If VBATT is available, the back-up battery can be charged by the internal 2.5V power supply regulator.

Table 61. BAT-RTC Pin Description

Signal	Pin #	I/O	I/O Type	Description
BAT-RTC	7	I/O	Supply	RTC Back-up supply

Table 62. Electrical Characteristics of BAT-RTC

Parameter	Minimum	Typical	Maximum	Unit
Input voltage	1.85		3.0	V
Input current consumption*		3.3		µA
Output voltage		2.45		V
Output current			2	mA

* Provided by an RTC back-up battery when the embedded module power supply is OFF (VBATT = 0V).

3.21.2. Typical Application Electrical Diagram

3.21.2.1. Super Capacitor

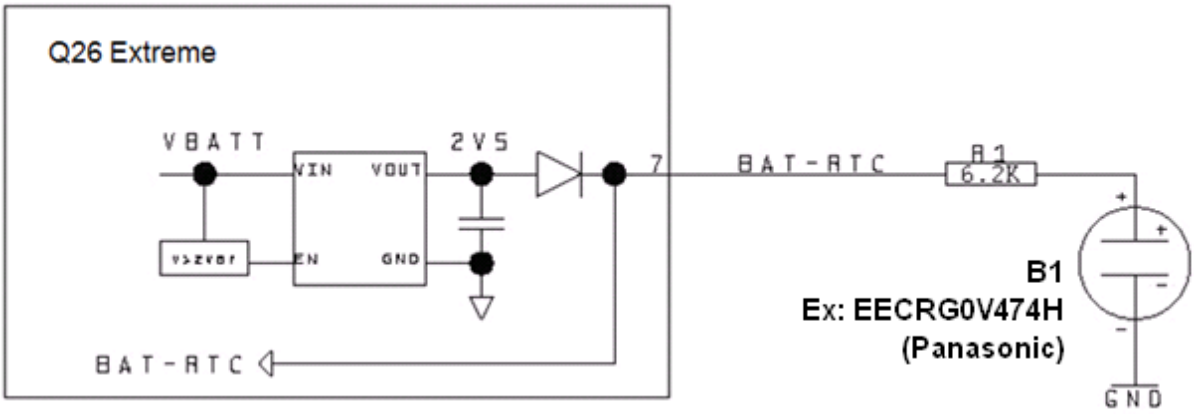


Figure 44. RTC Supplied by a Gold Capacitor

Estimated range with 0.47 Farad Gold Cap: 25 hours for 3µA.

Note: The gold capacitor maximum voltage is 2.5 V.

3.21.2.2. Non-Rechargeable Battery

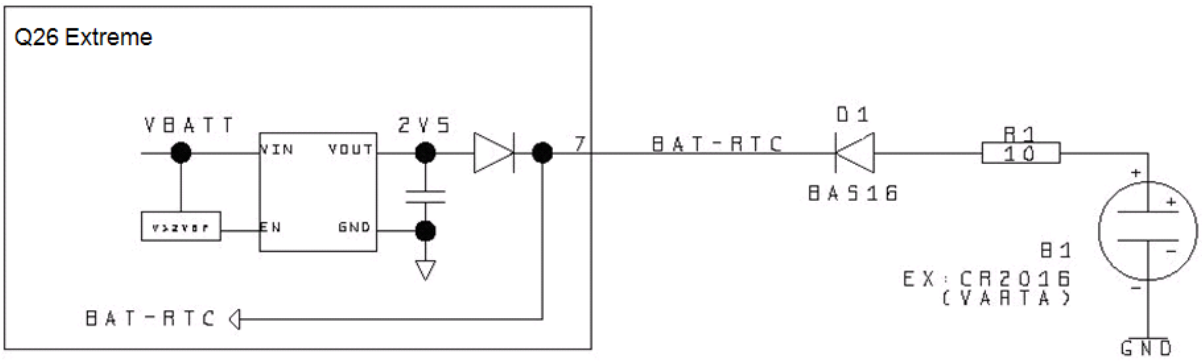


Figure 45. RTC Supplied by a Non-Rechargeable Battery

The diode D1 is mandatory, in order to protect the non-rechargeable battery.

Estimated range with 85 mAh battery: 800 h minimum.

3.21.2.3. Rechargeable Battery

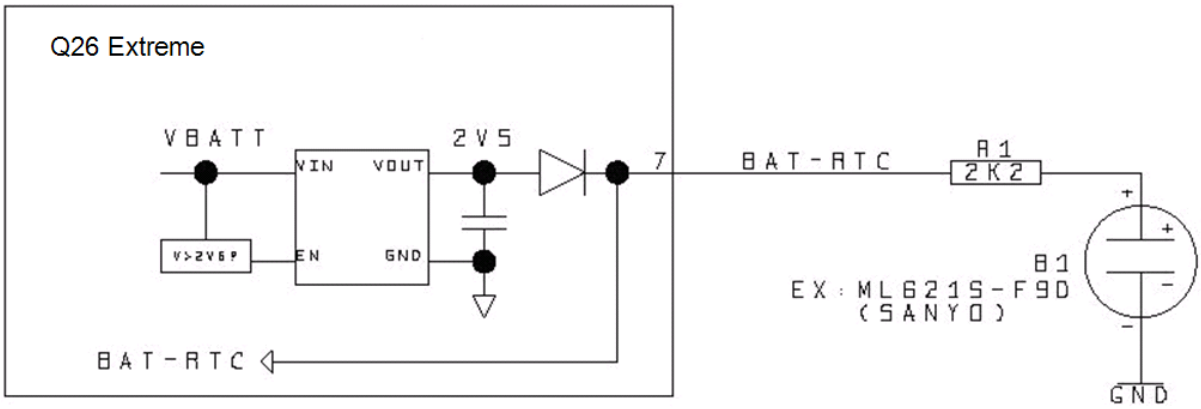


Figure 46. RTC Supplied by a Rechargeable Battery Cell

Estimated range with 2 mAh rechargeable battery: ~15 hours.

Warning: *Before the battery cell assembly, ensure that the cell voltage is lower than 2.75 V to avoid any damage to the embedded module.*

3.22. LED0 Signal

LED0 is an open drain output. A LED and a resistor can be directly connected between this output and VBATT.

When the Q26 Extreme embedded module is OFF, if 2.8V < VBATT < 3.2V and a charger is connected on CHG-IN inputs, this output flashes (100 ms ON, 900 ms OFF) to indicate the pre-charging phase of the battery.

When the Q26 Extreme embedded module is ON, this output is used to indicate network status.

Table 63. LED0 Status

Embedded Module State	VBATT Status	LED0 Status	Embedded Module Status
Embedded Module OFF	VBATT < 2.8V or VBATT > 3.2V	OFF	Embedded Module is OFF
	2.8V < VBATT < 3.2V	Pre-charge flash LED ON for 100ms, OFF for 900ms	Embedded Module is OFF, Pre-charging mode (charger must be connected on CHG-IN to activate this mode)
Embedded Module ON	VBATT > 3.2V	Permanent	Embedded Module switched ON, not registered on the network
		Slow flash LED ON for 200ms, OFF for 2s	Embedded Module switched ON, registered on the network
		Quick flash LED ON for 200ms, OFF for 600ms	Embedded Module switched ON, registered on the network, communication in progress
		Very quick flash LED ON for 100ms, OFF for 200ms	Embedded Module switched on, software downloaded is either corrupted or non-compatible ("BAD SOFTWARE")

Table 64. LED0 Pin Description

Signal	Pin #	I/O	I/O Type	Reset State	Description
LED0	17	O	Open Drain Output	1 and Undefined	LED driving

Refer to section 3.3 Electrical Information for Digital I/O for open drain, 2V8 and 1V8 voltage characteristics, and reset state definitions.

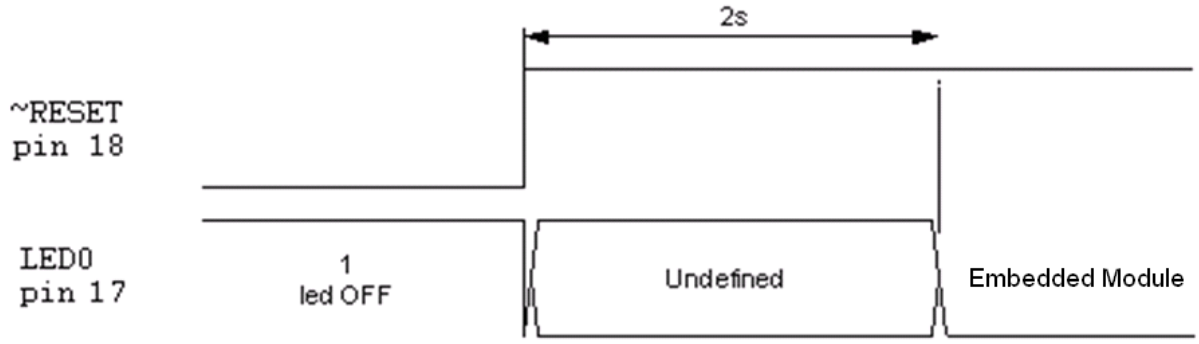


Figure 47. LED0 State During RESET and Initialization Time

LED0 state is high during RESET time and undefined during software initialization time. During software initialization time, for a maximum of 2 seconds after RESET cancellation, the LED0 signal is toggling and does not provide the embedded module status. After the 2s period, the LED0 provides the true status of the embedded module.

Table 65. Electrical Characteristics of LED0

Parameter	Condition	Minimum	Typical	Maximum	Unit
V_{OL}				0.4	V
I_{OUT}				8	mA

The GSM activity status indication signal LED0 (pin 17) may be used to drive an LED. This signal is an open-drain digital transistor in accordance to the embedded module activity status.

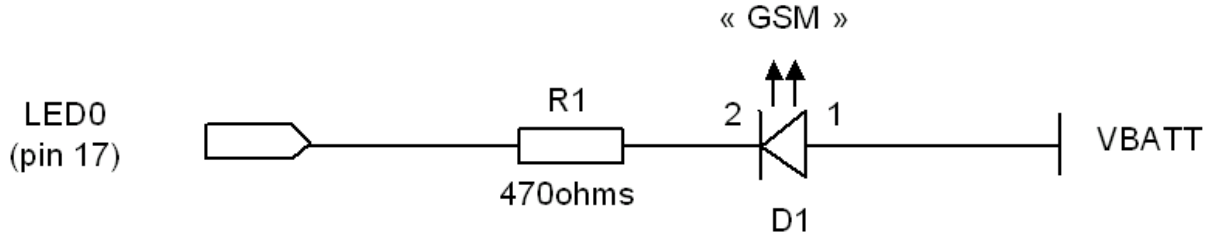


Figure 48. Example of GSM Activity Status Implementation

The value of R1 may be harmonized depending on the LED (D1) characteristics.

3.23. Digital Audio Interface (PCM)

Digital audio interface (PCM) interface mode allows connectivity with audio standard peripherals. It can be used, for example, to connect an external audio codec.

The programmability of this mode provides the ability to address a large range of audio peripherals.

PCM features:

- IOM-2 compatible device on physical level
- Master mode only with 6 slots by frame, user only on slot 4
- Bit rate single clock mode at 768kHz only
- 16 bits data word MSB first only
- Linear Law only (no compression law)
- Long Frame Synchronization only
- Push-pull configuration on PCM-OUT and PCM-IN

The digital audio interface configuration cannot differ from those specified above.

3.23.1. Description

The PCM interface consists of 4 wires:

- **PCM-SYNC** (output): The frame synchronization signal delivers an 8kHz frequency pulse that synchronizes the frame data in and the frame data out.
- **PCM-CLK** (output): The frame bit clock signal controls data transfer with the audio peripheral.
- **PCM-OUT** (output): The frame “data out” relies on the selected configuration mode.
- **PCM-IN** (input): The frame “data in” relies on the selected configuration mode.

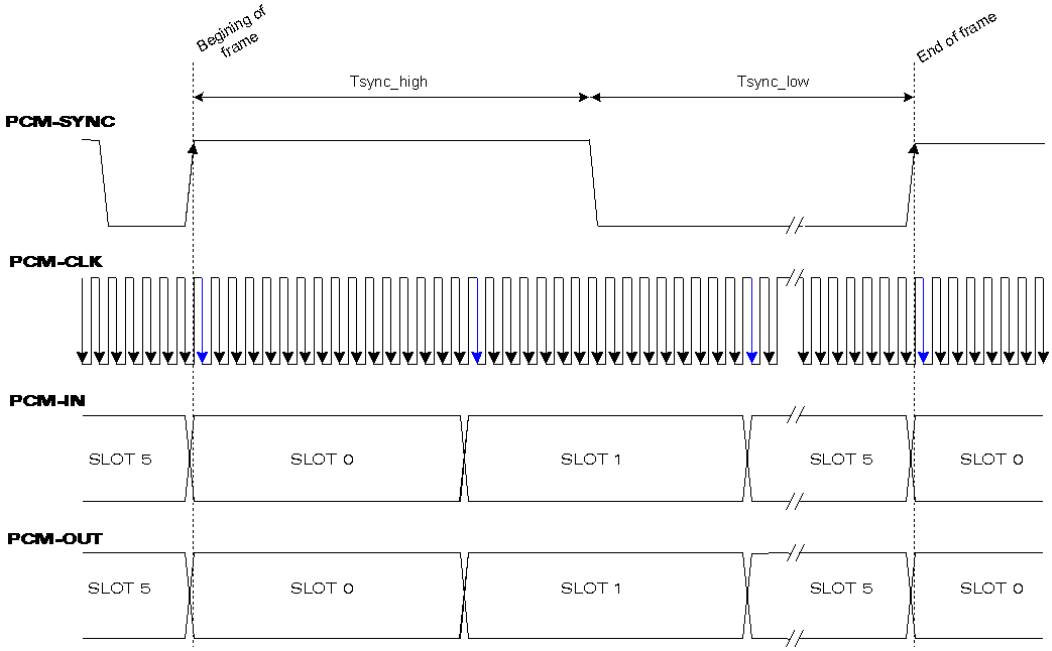


Figure 49. PCM Frame Waveform

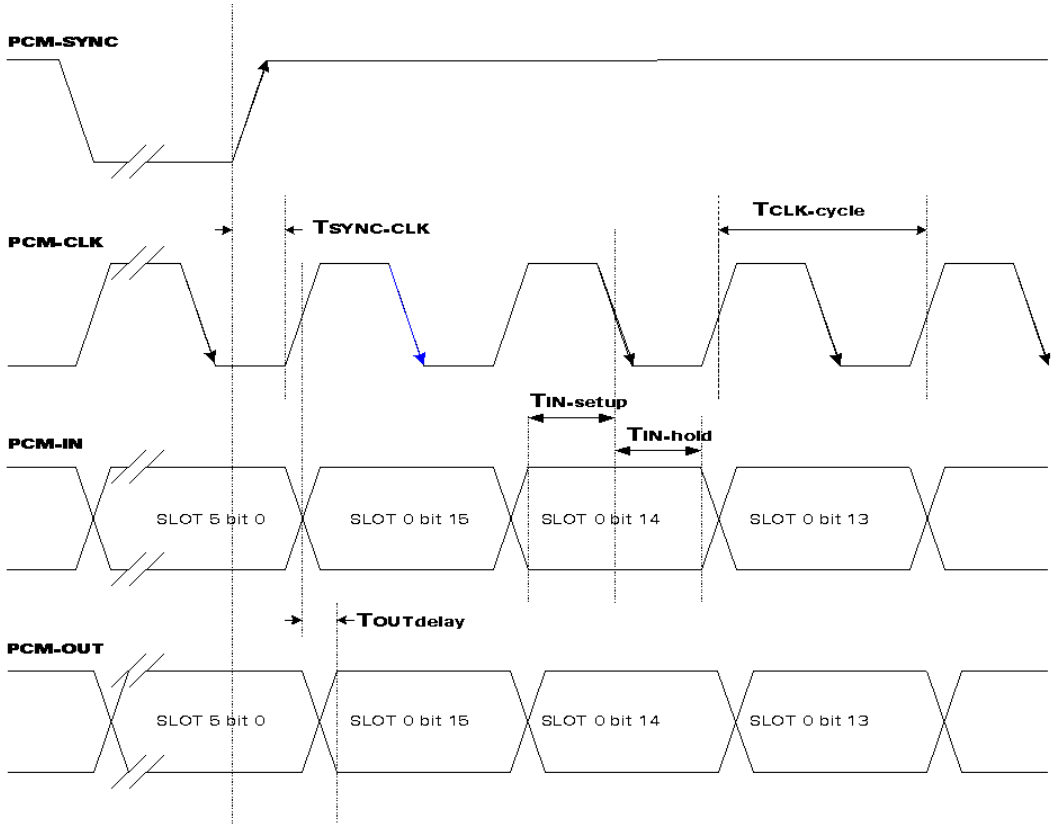


Figure 50. PCM Sampling Waveform

Table 66. AC Characteristics of the PCM Interface

Signal	Description	Minimum	Typical	Minimum	Unit
Tsync_low + Tsync_high	PCM-SYNC period		125		µs
Tsync_low	PCM-SYNC low time		93		µs
Tsync_high	PCM-SYNC high time		32		µs
TSYNC-CLK	PCM-SYNC to PCM-CLK time		-154		ns
TCLK-cycle	PCM-CLK period		1302		ns
TIN-setup	PCM-IN setup time	50			ns
TIN-hold	PCM-IN hold time	50			ns
TOUT-delay	PCM-OUT delay time			20	ns

Table 67. PCM Interface Pin Description

Signal	Pin #	I/O	I/O Type	Reset State	Description
PCM-SYNC	77	O	1V8	Pull-down	Frame synchronization 8kHz
PCM-CLK	79	O	1V8	Pull-down	Data clock
PCM-OUT	80	O	1V8	Pull-up	Data output
PCM-IN	78	I	1V8	Pull-up	Data input

Refer to section 3.3 Electrical Information for Digital I/O for open drain, 2V8 and 1V8 voltage characteristics, and reset state definitions.

3.24. USB 2.0 Interface

A 4-wire USB slave interface is available which complies with USB 2.0 protocol signaling. But it is not compliant with the electrical interface due to the 5V interface of VPAD-USB.

The USB interface signals are VPAD-USB, USB-DP, USB-DM and GND.

The USB interface features:

- 12Mbit/s full-speed transfer rate
- 3.3V typ compatible
- USB Softconnect feature
- CDC 1.1 – ACM compliant

Note: A 5V to 3.3V typ voltage regulator is needed between the external interface power in line (+5V) and the embedded module line (VPAD-USB).

Table 68. USB Interface Pin Description

Signal	Pin #	I/O	I/O Type	Description
VPAD-USB	52	I	VPAD_USB	USB Power Supply
USB-DP	54	I/O	VPAD_USB	Differential data interface positive
USB-DM	56	I/O	VPAD_USB	Differential data interface negative

Table 69. Electrical Characteristics of the USB Interface

Parameter	Minimum	Typical	Maximum	Unit
VPAD-USB, USB-DP, USB-DM	3.0	3.3	3.6	V
VPAD-USB Input current consumption		8		mA

The typical diagram is presented below:

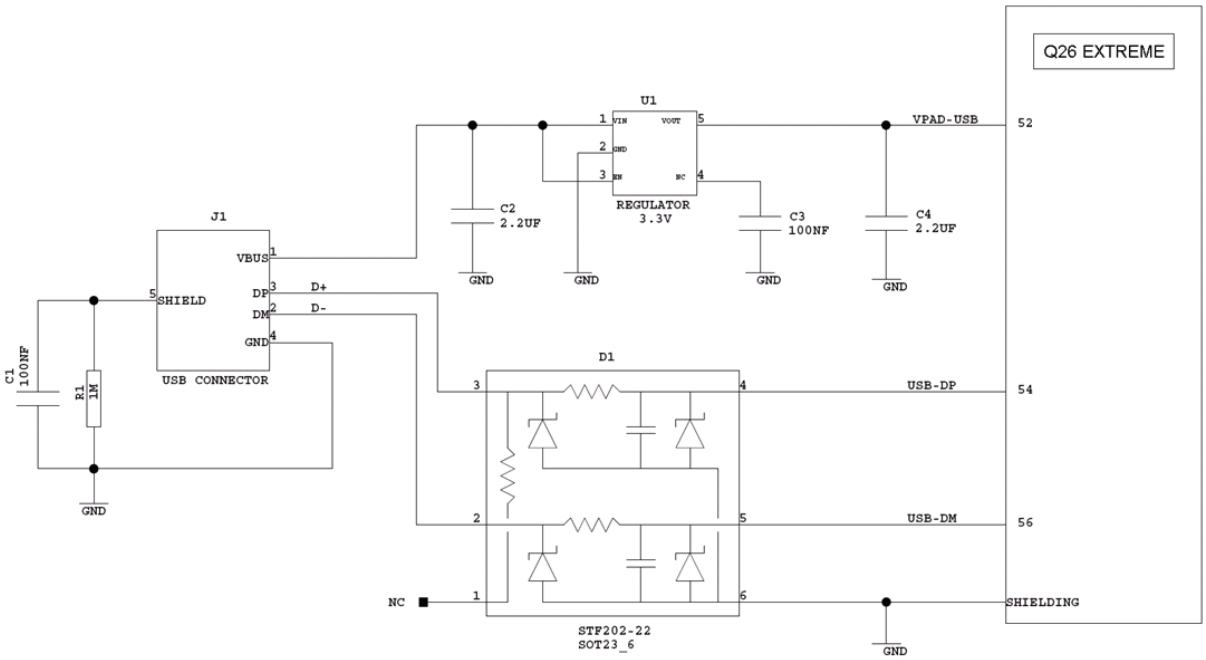


Figure 51. Example of a USB Implementation

3.24.1. Recommended Components

- R1: 1MΩ
- C1, C3: 100nF
- C2, C4: 2.2µF
- D1: STF2002-22 from SEMTECH
- U1: LP2985AIM 3.3V from NATIONAL SEMICONDUCTOR

The regulator used is a 3.3V regulator. It supplies via J1 when the USB wire is plugged.

D1 is the EMI/RFI filter with ESD protection. The D1 internal pull-up resistor, used to detect the full speed, is not connected, because it is embedded in the embedded module.

R1 and C1 must be close to J1.

3.25. RF Interface

Q26 Extreme embedded module supports two antennas (main and diversity). The impedance is 50Ω nominal and the DC impedance is 0Ω.

3.25.1. RF Connections

The Q26 Extreme embedded module does not support an antenna switch for a car kit, but this function can be implemented externally and can be driven using a GPIO.

The antenna cable and connector should be selected in order to minimize losses in the frequency bands used for GSM 850/900MHz and 1800/1900MHz.

0.5dB may be considered as the maximum value of loss between the embedded module and an external connector.

3.25.1.1. U.FL Connector for Main Antenna

A wide variety of cables fitted with U.FL connectors is offered by different suppliers.

3.25.1.2. Soldered Solution for Main and Diversity Antenna

The soldered solution will preferably be based on an RG178 coaxial cable.

3.25.2. RF Performance

RF performance is compliant with the ETSI GSM 05.05 recommendation.

The main receiver parameters are:

- GSM850 Reference Sensitivity = -104 dBm typical (Static & TUHigh)
- E-GSM900 Reference Sensitivity = -104 dBm typical (Static & TUHigh)
- DCS1800 Reference Sensitivity = -102 dBm typical (Static & TUHigh)
- PCS1900 Reference Sensitivity = -102 dBm typical (Static & TUHigh)
- 3G Band I 2100 Reference Sensitivity = -106.7 dBm typical (Static & TUHigh)
- 3G Band II 1900 Reference Sensitivity = -106.7 dBm typical (Static & TUHigh)
- 3G Band V 850 Reference Sensitivity = -106.7 dBm typical (Static & TUHigh)
- Selectivity @ 200 kHz: > +9 dBc
- Selectivity @ 400 kHz: > +41 dBc
- Linear dynamic range: 63 dB
- Co-channel rejection: >= 9 dBc

Transmitter parameters:

- Maximum output power (EGSM & GSM850): 33 dBm +/- 2 dB at ambient temperature
- Maximum output power (GSM1800 & PCS1900): 30 dBm +/- 2 dB at ambient temperature
- Minimum output power (EGSM & GSM850): 5 dBm +/- 5 dB at ambient temperature
- Minimum output power (GSM1800 & PCS1900): 0 dBm +/- 5 dB at ambient temperature
- Maximum output power (3G all band): 24 dBm +1/-3 dB at ambient temperature

3.25.3. Antenna Specifications

The antenna must meet the requirements specified below.

The optimum operating frequency depends on the application. Either a dual-band or quad-band antenna will operate in these frequency bands and have the following characteristics:

Table 70. Antenna Specifications

Characteristics		E-GSM 900	DCS 1800	GSM 850 and WCDMA band V	PCS 1900 and WCDMA band II	WCDMA band I
TX Frequency		880 to 915 MHz	1710 to 1785 MHz	824 to 849 MHz	1850 to 1910 MHz	1920 to 1980 MHz
RX Frequency		925 to 960 MHz	1805 to 1880 MHz	869 to 894 MHz	1930 to 1990 MHz	2110 to 2170 MHz
Impedance		50 Ω				
VSWR	Rx max	1.5:1				
	Tx max	1.5:1				
Typical radiated gain		0dBi in one direction at least				

4. Technical Specifications

4.1. General Purpose Connector Pin-Out Description

Table 71. GPIO Pin-out Description

Description	I/O*	Voltage	Signal		Pin Number		Signal		Voltage	I/O*	Description
			Mux	Nominal			Mux	Nominal			
Power Supply	I	VBATT		VBATT	1	2	VBATT		VBATT	I	Power Supply
Power Supply	I	VBATT		VBATT	3	4	VBATT		VBATT	I	Power Supply
1.8V Supply Output	O	VCC_1V8		VCC_1V8	5	6	CHG-IN		CHG-IN	I	Charger input
RTC Battery connection	I/O	BAT-RTC		BAT-RTC	7	8	CHG-IN		CHG-IN	I	Charger input
USIM Power Supply	O	1V8 or 3V		SIM-VCC	9	10	VCC_2V8		VCC_2V8	O	2.8V Supply Output
USIM Data	I/O	1V8 or 3V		SIM-IO	11	12	SIMPRES	GPIO18	VCC_1V8	I	USIM Detection
USIM reset	O	1V8 or 3V		~SIM-RST	13	14	SIM-CLK		1V8 or 3V	O	USIM Clock
Buzzer Output	O	Open Drain		BUZZER0	15	16	BOOT		VCC_1V8	I	Not Used
LED0 Output	O	Open Drain		LED0	17	18	~RESET		VCC_1V8	I/O	RESET Input
ON / ~OFF Control	I	VBATT		ON/~OFF	19	20	BAT-TEMP		Analog	I	Analog temperature
Analog to Digital Input	I	Analog		ADC2	21	22	GPIO31	SPI1-LOAD	VCC_2V8	I/O	
SPI1 Clock	O	VCC_2V8	GPIO28	SPI1-CLK	23	24	SPI1-I	GPIO30	VCC_2V8	I	SPI1 Data Input
SPI1 Data Input / Output	I/O	VCC_2V8	GPIO29	SPI1-IO	25	26	SPI2-CLK	GPIO32	VCC_2V8	O	SPI2 Clock
SPI2 Data Input / Output	I/O	VCC_2V8	GPIO33	SPI2-IO	27	28	GPIO35	SPI2-LOAD	VCC_2V8	I/O	
SPI2 Data Input	I	VCC_2V8	GPIO34	SPI2-I	29	30	CT104-RXD2	GPIO15	VCC_1V8	O	Auxiliary RS232 Receive
Auxiliary RS232 Transmit	I	VCC_1V8	GPIO14	CT103-TXD2	31	32	~CT106-CTS2	GPIO16	VCC_1V8	O	Auxiliary RS232 Clear To Send

Description	I/O*	Voltage	Signal		Pin Number		Signal		Voltage	I/O*	Description
			Mux	Nominal			Mux	Nominal			
Auxiliary RS232 Request To Send	I	VCC_1V8	GPIO17	~CT105-RTS2	33	34	MIC2N		Analog	I	Micro 2 Input Negative
Speaker 1 Output Positive	O	Analog		SPK1P	35	36	MIC2P		Analog	I	Micro 2 Input Positive
Speaker 1 Output Negative	O	Analog		SPK1N	37	38	MIC1N		Analog	I	Micro 1 Input Negative
Speaker 2 Output Positive	O	Analog		SPK2P	39	40	MIC1P		Analog	I	Micro 1 Input Positive
Speaker 2 Output Negative	O	Analog		SPK2N	41	42	A1	**	VCC_1V8	O	Address bus 1
	I/O	VCC_2V8	32kHz	GPIO0	43	44	SCL1	GPIO26	Open Drain	O	I²C Clock
	I/O	VCC_2V8		GPIO19	45	46	SDA1	GPIO27	Open Drain	I/O	I²C Data
	I/O	VCC_2V8		GPIO21	47	48	GPIO20		VCC_2V8	I/O	
Interruption 1 Input	I	VCC_2V8	GPIO25	INT1	49	50	INT0	GPIO3	VCC_1V8	I	Interruption 0 Input
	I/O	VCC_1V8	**	GPIO1	51	52	VPAD-USB		VPAD-USB	I	USB Power supply input
	I/O	VCC_1V8	A24	GPIO2	53	54	USB-DP		VPAD-USB	I/O	USB Data
	I/O	VCC_2V8	**	GPIO23	55	56	USB-DM		VPAD-USB	I/O	USB Data
	I/O	VCC_2V8	**	GPIO22	57	58	GPIO24		VCC_2V8	I/O	
Keypad column 0	I/O	VCC_1V8	GPIO4	COL0	59	60	COL1	GPIO5	VCC_1V8	I/O	Keypad column 1
Keypad column 2	I/O	VCC_1V8	GPIO6	COL2	61	62	COL3	GPIO7	VCC_1V8	I/O	Keypad column 3
Keypad column 4	I/O	VCC_1V8	GPIO8	COL4	63	64	ROW4	GPIO13	VCC_1V8	I/O	Keypad Row 4
Keypad Row 3	I/O	VCC_1V8	GPIO12	ROW3	65	66	ROW2	GPIO11	VCC_1V8	I/O	Keypad Row 2
Keypad Row 1	I/O	VCC_1V8	GPIO10	ROW1	67	68	ROW0	GPIO9	VCC_1V8	I/O	Keypad Row 0
Main RS232 Ring	O	VCC_2V8	GPIO42	~CT125-RI	69	70	~CT109-DCD1	GPIO43	VCC_2V8	O	Main RS232 Data

Description	I/O*	Voltage	Signal		Pin Number		Signal		Voltage	I/O*	Description
			Mux	Nominal			Mux	Nominal			
Indicator											Carrier Detect
Main RS232 Transmit	I	VCC_2V8	GPIO36	CT103-TXD1	71	72	~CT105-RTS1	GPIO38	VCC_2V8	I	Main RS232 Request To Send
Main RS232 Receive	O	VCC_2V8	GPIO37	CT104-RXD1	73	74	~CT107-DSR1	GPIO40	VCC_2V8	O	Main RS232 Data Set Ready
Main RS232 Clear To Send	O	VCC_2V8	GPIO39	~CT106-CTS1	75	76	~CT108-2-DTR1	GPIO41	VCC_2V8	I	Main RS232 Data Terminal Ready
PCM Frame Synchro	O	VCC_1V8		PCM-SYNC	77	78	PCM-IN		VCC_1V8	I	PCM Data Input
PCM Clock	O	VCC_1V8		PCM-CLK	79	80	PCM-OUT		VCC_1V8	O	PCM Data Output
Read enable		VCC_1V8		~OE-R/W	81	82	DAC0		Analog	O	
Chip select 3		VCC_1V8		GPIO44/ ~CS3	83	84	~WE-E		VCC_1V8		Write enable
DATA bus		VCC_1V8		D0	85	86	D15		VCC_1V8		DATA bus
DATA bus		VCC_1V8		D1	87	88	D14		VCC_1V8		DATA bus
DATA bus		VCC_1V8		D2	89	90	D13		VCC_1V8		DATA bus
DATA bus		VCC_1V8		D3	91	92	D12		VCC_1V8		DATA bus
DATA bus		VCC_1V8		D4	93	94	D11		VCC_1V8		DATA bus
DATA bus		VCC_1V8		D5	95	96	D10		VCC_1V8		DATA bus
DATA bus		VCC_1V8		D6	97	98	D9		VCC_1V8		DATA bus
DATA bus		VCC_1V8		D7	99	100	D8		VCC_1V8		DATA bus

* The I/O direction information is only for the nominal signal. When the signal is configured in GPIO, it can always be an Input or an Output.

** For more information about the multiplexing of these signals, refer to section 3.10 General Purpose Input/Output.

4.2. Environmental Specifications

Sierra Wireless specifies the following temperature range for the Q26 Extreme embedded module product.

The Q26 Extreme embedded module is compliant with the following operating classes.

Table 72. Operating Temperatures

Conditions	Temperature Range
Operating / Class A	-20 °C to +55°C
Operating / Storage / Class B	-30 °C to +75°C

4.2.1. Functions Status Classification

4.2.1.1. Class A

The embedded module remains fully functional, meeting GSM performance criteria in accordance with ETSI requirements, across the specified temperature range.

4.2.1.2. Class B

Operating Class B restrictions depends on the Q26 Extreme implementation; refer to section 6 Design Guidelines for optimized implementation.

The embedded module remains functional, across the specified temperature range. Some GSM parameters may occasionally deviate from the ETSI specified requirements. Auto shut down is implemented for protection against extreme temperature (deactivated for emergency calls); refer to the following table for communication characteristic in extreme T° environment.

The table below show sample measurements in lab environment conditions (Environmental specifications will be available after Q26 Extreme environmental qualification plan).

Table 73. Operating Duration Versus Temperature

Mode	Ambient Temperature (°C)	RF Power (dBm)	Operating Duration (min)
GSM/GPRS/EGPRS Class 8	75	Max	∞
GPRS/EGPRS Class 10	70	Max	∞
GPRS/EGPRS Class 10	75	Max	1
GPRS/EGPRS Class 12	65	Max	∞
GPRS/EGPRS Class 12	70	Max	2
WCDMA	70	< 0	∞
WCDMA	65	Max	∞
WCDMA	70	Max	2
HSDPA 7.2 Mbits/s	70	< 0	∞
HSDPA 7.2 Mbits/s	60	Max	∞
HSDPA 7.2 Mbits/s	65	Max	2

Test condition: The Q26 Extreme is plugged in a starter kit light with forced air circulation Vbatt = 3.8V.

4.3. Mechanical Specifications

4.3.1. Physical Characteristics

The Q26 Extreme embedded module has a complete self-contained shield.

- Overall dimensions : 32.2x40x6.3 mm (except shielding pins)
- Weight : 11.8 g

4.3.2. Mechanical Drawings

The mechanical specifications of the Q26 Extreme embedded module are shown in the following page.

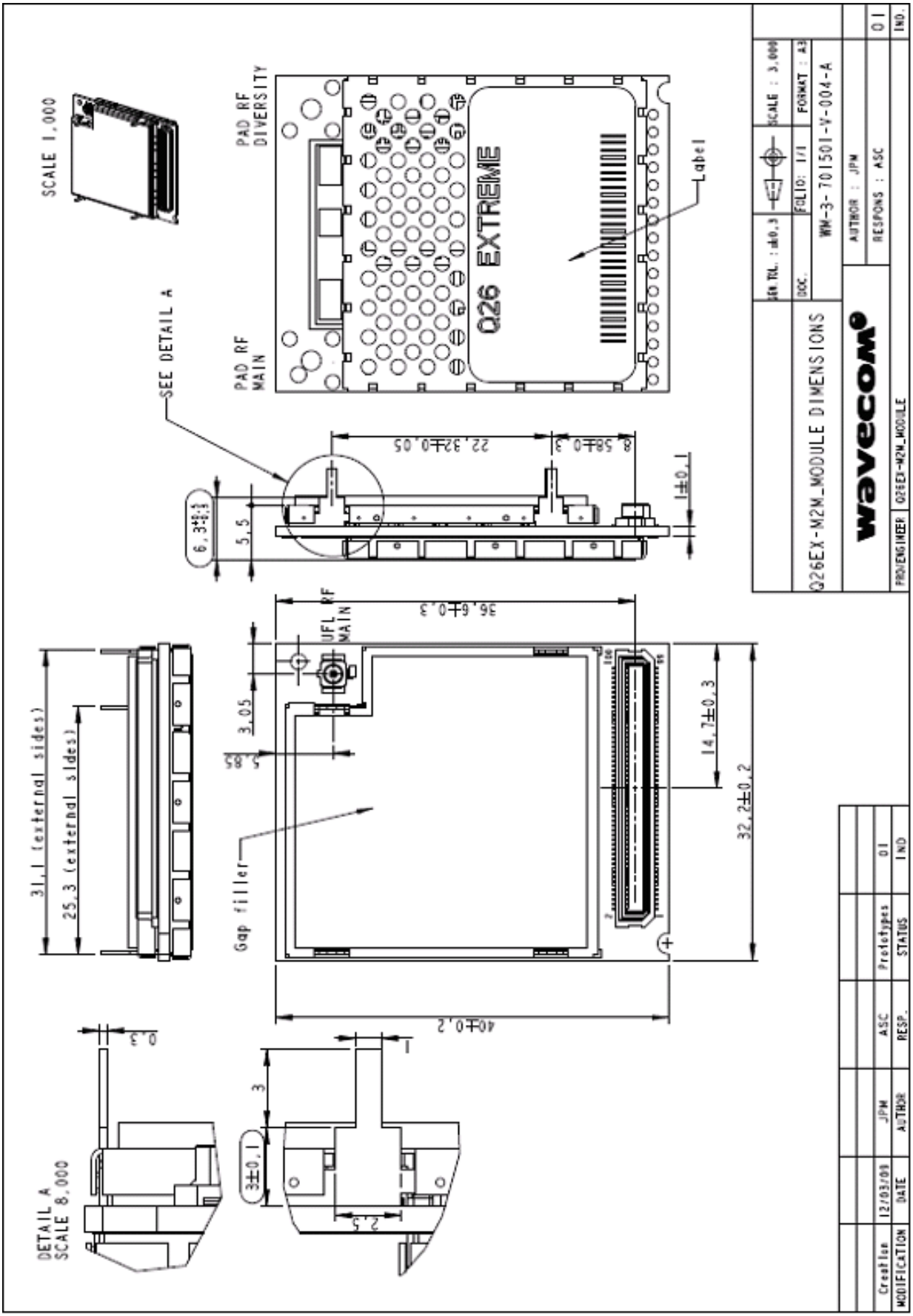


Figure 52. Mechanical Drawing

5. Connector and Peripheral Device References

5.1. General Purpose Connector

The GPC is a 100-pin connector with 0.5mm pitch from the from PANASONIC Group's P5K series, with the following reference:

AXK600347BN1

The mating connector has the following reference:

AXK500147BN1J

The stacking height is 3.0 mm.

Sierra Wireless recommends that the **AXK500147BN1J** connector be used for applications to benefit from Sierra Wireless prices. For more information, contact Panasonic and quote the Sierra Wireless connector reference: **WM18868**.

For more information about the recommended GPC, refer to the GPC data sheets available from Panasonic (see http://www.panasonic.com/host/industrl.html).

5.2. USIM Card Reader

- AMPHENOL C707 series (see http://www.amphenol.com)
- JAE (see http://www.jae.co.jp)
- MOLEX 99228-0002 (connector) / MOLEX 91236-0002 (holder) (see http://www.molex.com)

5.3. Microphone

Possible suppliers:

- HOSIDEN
- PANASONIC
- PEIKER

5.4. Speaker

Possible suppliers:

- SANYO
- HOSIDEN
- PRIMO
- PHILIPS

5.5. Antenna Cable

There is a main antenna connection for 2G and 3G and a diversity connection only for 3G.

For the main connection, there are two possibilities:

- UF-L pigtails connection on the bottom side
- Coaxial cable soldered to the RF pad (opposite side of the UF-L connector) on the top side

For the diversity connection, the only possibility is to solder a coaxial cable to the second RF pad (no UF-L connector on the opposite side) on the top side.

A wide variety of cables fitted with UF-L connectors is offered by HIROSE:

- UF-L pigtails, Ex: Ref = **U.FL-2LP(V)-04-A-(100)**
- UF-L Ref = **U.FL-R-SMT**
- UF-L cable assemblies
- Between series cable assemblies

More information is also available from http://www.hirose-connectors.com/.

For the coaxial cable soldered on the RF pad the following references have been certified for mounting on the Q26 Extreme embedded module:

- RG178
- RG316

5.6. RF Antenna

RF antennas and support for antenna adaptation can be obtained from manufacturers such as:

- TAOGLAS (http://www.taoglas.com)
- HIRSCHMANN (http://www.hirschmann.com/)

6. Design Guidelines

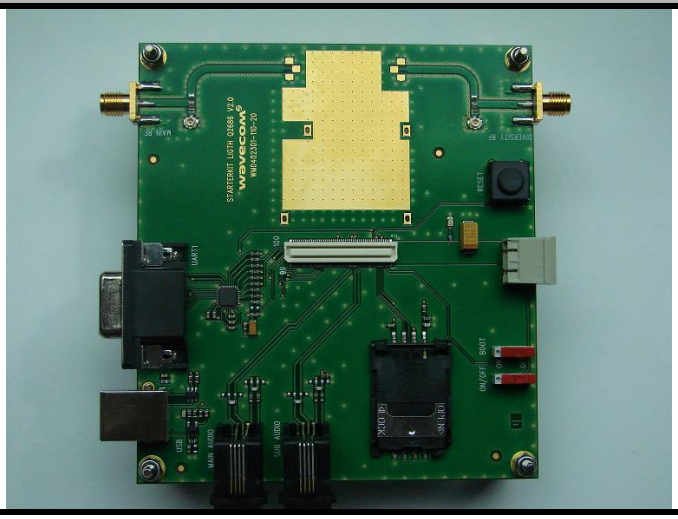
The purpose of the following paragraphs is to present design guidelines.

6.1. Hardware and RF

6.1.1. Thermal Recommendations

The Q26 Extreme is natively equipped with foam improving thermal dissipation for better behavior in extreme conditions.

In order to improve thermal dissipation in the customer board, it is recommended to add a copper area (without solder mask) on both sides of the customer PCB. Both sides shall be connected with thermal via.

Starter Kit Used for Thermal Behavior Measurement with Copper Area	Foam Mounted on the Q26 Extreme
	

6.1.2. EMC Recommendations

EMC tests must be performed on the application as soon as possible to detect any potential problems.

When designing, special attention should be paid to:

- Possible spurious emission radiated by the application to the RF receiver in the receiver band
- ESD protection is **mandatory** on all signals which have external accessibility (typically human accessibility). Typically, ESD protection is mandatory for the:
  - USIM (if accessible from outside)
  - Serial link
- EMC protection on audio input/output (filters against 900MHz emissions)
- Biasing of the microphone inputs
- Length of the USIM interface lines (preferably < 10cm)

- Ground plane: Sierra Wireless recommends a common ground plane for analog/digital/RF grounds.
- A metallic case or plastic casing with conductive paint are recommended

Note: The embedded module does not include any protection against over-voltage.

6.1.3. Power Supply

The power supply is one of the key issues in the design of a terminal.

A weak power supply design could, in particular, affect:

- EMC performance
- The emission spectrum
- The phase error and frequency error

Warning: *Careful attention should be paid to the quality of the power supply – low ripple, PFM or PSM systems should be avoided (PWM converter preferred; and the capacity to deliver high current peaks in a short time (pulsed radio emission).*

6.1.4. Layout Requirements

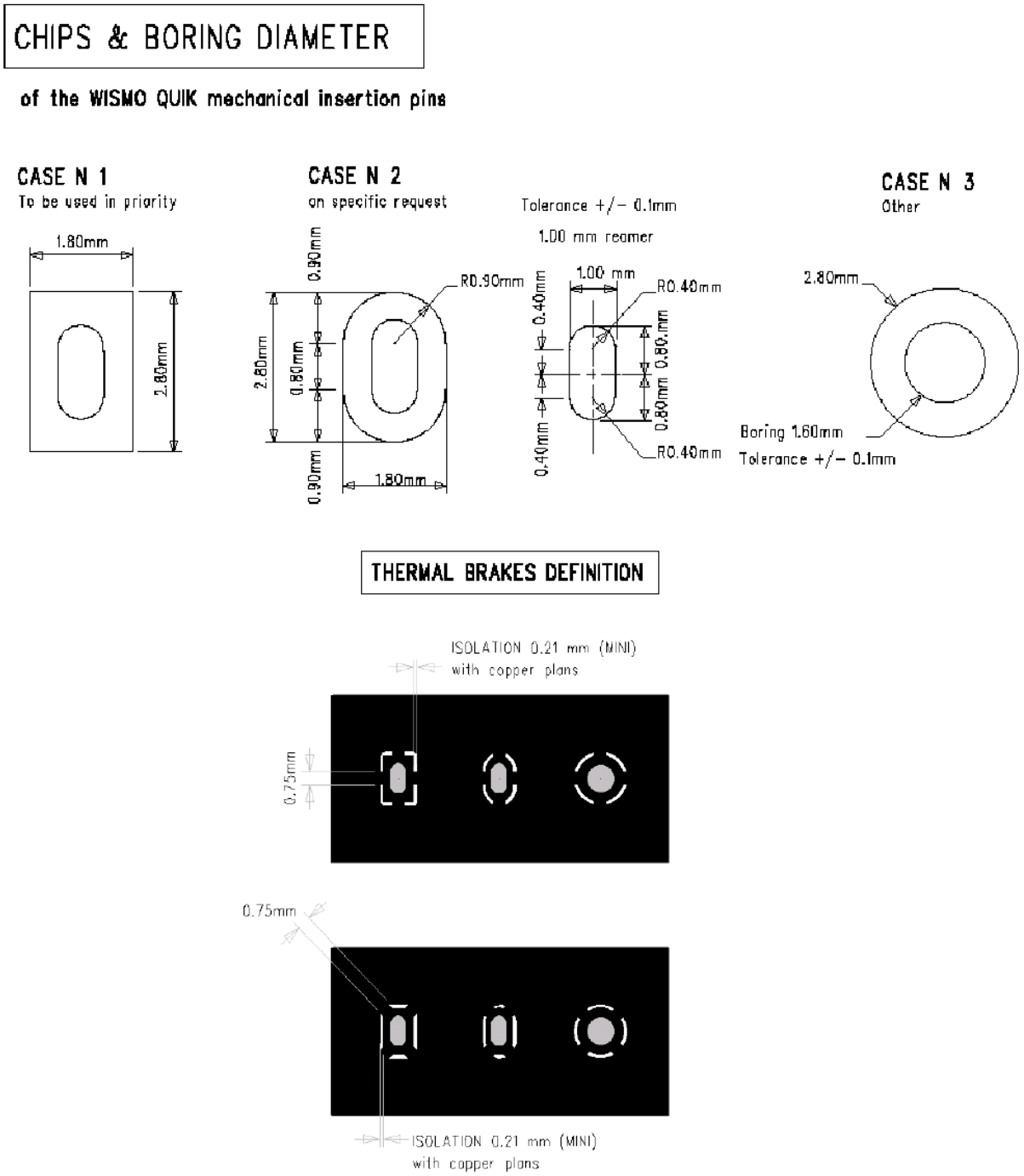


Figure 53. Layout Requirement

6.1.5. Antenna

Warning: *Sierra Wireless strongly recommends working with an antenna manufacturer either to develop an antenna adapted to the application or to adapt an existing solution to the application.*

Both the mechanical and electrical antenna adaptation is one of the key issues in the design of the GSM/UMTS terminal.

6.2. Mechanical Integration

Attention should be paid to:

- Antenna cable integration (bending, length, position, etc)
- Leads of the embedded module to be soldered to the Ground plane

6.3. Operating System Upgrade

The Q26 Extreme embedded module operating system is stored in flash memory and can be easily upgraded.

Caution:	*In order to follow regular changes in the 3GPP standard and to offer a state-of-the-art Operating System, Sierra Wireless recommends that the application designed around an embedded module (or embedded module-based product) allow easy Operating System upgrades on the embedded module via the standard X-modem protocol. Therefore, the application shall either allow a direct access to the embedded module serial link through an external connector or implement any mechanism allowing the embedded module Operating System to be downloaded via X-modem.*

The Operating System file can be downloaded to the modem using the X-modem protocol. The **AT+WDWL** command allows the download process to be launched (see the description in document [5] Firmware v7.4 AT Commands Manual).

The serial signals required to proceed with X-modem downloading are:

- Rx
- Tx
- RTS
- CTS
- GND

The Operating System file can also be downloaded to the modem using the DOTA (download over the air) feature. This feature is available with the Sierra Wireless Software Suite interface. For more details, please refer to the documents listed in section 1.2.1 Reference Documents.

7. Appendix

7.1. Standards and Recommendations

The Q26 Extreme embedded module connected on a development kit board application is compliant with the following requirements:

- R&TTE:
  - Spectrum: EN 301 511 v 9.0.2
  - Safety: EN 60950-1:2005 (Ed 2.0)
  - EMC: EN 301 489-1v 1.8.1, EN 301 489-7 v1.3.1, EN 301 489-24 v1.4.1
- GCF-CC and NAPRD.03 versions will be specified as soon as certification will be started (most updated version applicable at this time)

Federal Communications Commission (FCC) rules and Regulations: Power listed on the Grant is conducted for Part 22 and conducted for Part 24.

This device is to be used only for mobile and fixed applications. The antenna(s) used for this transmitter must be installed to provide a separation distance of at least 20cm from all persons and must not be co-located or operating in conjunction with any other antenna or transmitter within a host device, except in accordance with FCC multi-transmitter product procedures.

Antennas used for this OEM module must not exceed a gain of 4.6dBi (850MHz) and 3.4dBi (1900MHz) respectively. This device is approved as a module to be installed in other devices.

Installed in other portable devices, the exposure conditions require a separate equipment authorization.

The license module had a FCC ID label on the module itself. The FCC ID label must be visible through a window or it must be visible when an access panel, door or cover is easily removed.

If not, a second label must be placed on the outside of the device that contains the following text:

Contains FCC ID: **O9EQ26EX**

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

1. this device may not cause harmful interference,
2. this device must accept any interference received, including interference that may cause undesired operation.

Caution: *Manufacturers of mobile or fixed devices incorporating Q26 Extreme embedded module are advised to clarify any regulatory questions, have their completed product tested, have product approved for FCC compliance, and include instructions according to above mentioned RF exposure statements in end product user manual.*

Please note that changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

7.2. Safety Recommendations (for Information Only)

For the efficient and safe operation of your GSM device, please read the following information carefully.

7.2.1. RF Safety

7.2.1.1. General

Your GSM terminal is based on the GSM standard for cellular technology. The GSM standard is spread all over the world. It covers Europe, Asia and some parts of America and Africa. This is the most used telecommunication standard.

Your GSM terminal is actually a low power radio transmitter and receiver. It sends out as well as receives radio frequency energy. When you use your GSM application, the cellular system which handles your calls controls both the radio frequency and the power level of your cellular modem.

7.2.1.2. Exposure to RF Energy

There has been some public concern on possible health effects of using GSM terminals. Although research on health effects from RF energy has focused on the current RF technology for many years, scientists have begun research regarding newer radio technologies, such as GSM. After existing research had been reviewed, and after compliance to all applicable safety standards had been tested, it has been concluded that the product was fitted for use.

If you are concerned about exposure to RF energy there are things you can do to minimize exposure. Obviously, limiting the duration of your calls will reduce your exposure to RF energy. In addition, you can reduce RF exposure by operating your cellular terminal efficiently by following the guidelines below.

7.2.1.3. Efficient Terminal Operation

For your GSM terminal to operate at the lowest power level, consistent with satisfactory call quality:

If your terminal has an extendable antenna, extend it fully. Some models allow you to place a call with the antenna retracted. However your GSM terminal operates more efficiently with the antenna when it is fully extended.

Do not hold the antenna when the terminal is "IN USE". Holding the antenna affects call quality and may cause the modem to operate at a higher power level than needed.

7.2.1.4. Antenna Care and Replacement

Do not use the GSM terminal with a damaged antenna. If a damaged antenna comes into contact with the skin, a minor burn may result. Replace a damaged antenna immediately. You may repair antenna to yourself by following the instructions provided to you. If so, use only a manufacturer-approved antenna. Otherwise, have your antenna repaired by a qualified technician.

Buy or replace the antenna only from the approved suppliers list. Using of unauthorized antennas, modifications or attachments could damage the terminal and may violate local RF emission regulations or invalidate type approval.

7.2.2. General Safety

7.2.2.1. Driving

Check the laws and the regulations regarding the use of cellular devices in the area where you have to drive as you always have to comply with them. When using your GSM terminal while driving, please:

- give full attention to driving,
- pull-off from the road and park before making or answering a call if driving conditions so require.

7.2.2.2. Electronic Devices

Most electronic equipment, for example in hospitals and motor vehicles is shielded from RF energy. However, RF energy may affect some improperly shielded electronic equipment.

7.2.2.3. Vehicle Electronic Equipment

Check your vehicle manufacturer representative to determine if any on-board electronic equipment is adequately shielded from RF energy.

7.2.2.4. Medical Electronic Equipment

Consult the manufacturer of any personal medical devices (such as pacemakers, hearing aids, etc) to determine if they are adequately shielded from external RF energy.

Turn your terminal **OFF** in health care facilities when any regulations posted in the area instruct you to do so. Hospitals or health care facilities may be using RF monitoring equipment.

7.2.2.5. Aircraft

Turn your terminal OFF before boarding any aircraft.

- Use it on the ground only with crew permission.
- Do not use it in the air.

To prevent possible interference with aircraft systems, Federal Aviation Administration (FAA) regulations require you should have prior permission from a crew member to use your terminal while the aircraft is on the ground. In order to prevent interference with cellular systems, local RF regulations prohibit using your modem while airborne.

7.2.2.6. Children

Do not allow children to play with your GSM terminal. It is not a toy. Children could hurt themselves or others (by poking themselves or others in the eye with the antenna, for example). Children could damage the modem, or make calls that increase your modem bills.

7.2.2.7. Blasting Areas

To avoid interfering with blasting operations, turn your unit OFF when you are in a "blasting area" or in areas posted: "turn off two-way radio". Construction crew often uses remote control RF devices to set off explosives.

7.2.2.8. Potentially Explosive Atmospheres

Turn your terminal **OFF** when in any area with a potentially explosive atmosphere. Though it is rare, but your modem or its accessories could generate sparks. Sparks in such areas could cause an explosion or fire resulting in bodily injuries or even death.

Areas with a potentially explosive atmosphere are often, but not always, clearly marked. They include fuelling areas such as petrol stations; below decks on boats; fuel or chemical transfer or storage facilities; and areas where the air contains chemicals or particles, such as grain, dust, or metal powders.

Do not transport or store flammable gas, liquid, or explosives, in the compartment of your vehicle which contains your terminal or accessories.

Before using your terminal in a vehicle powered by liquefied petroleum gas (such as propane or butane) ensure that the vehicle complies with the relevant fire and safety regulations of the country in which the vehicle is used.

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