Product Technical Specification & Customer Design Guidelines

AirPrime Q2668

SIERRA WIRELESS

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Due to the nature of wireless communications, transmission and reception of data can never be guaranteed. Data may be delayed, corrupted (i.e., have errors) or be totally lost. Although significant delays or losses of data are rare when wireless devices such as the Sierra Wireless modem are used in a normal manner with a well-constructed network, the Sierra Wireless modem should not be used in situations where failure to transmit or receive data could result in damage of any kind to the user or any other party, including but not limited to personal injury, death, or loss of property. Sierra Wireless accepts no responsibility for damages of any kind resulting from delays or errors in data transmitted or received using the Sierra Wireless modem, or for failure of the Sierra Wireless modem to transmit or receive such data.

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1. Introduction

This document presents and defines the AirPrime Q2668 intelligent embedded module.

The Q2668 series is a self-contained GSM/GPRS/EGDE dual-band and TD-HSDPA dual-mode module with footprint compatible with other Q26 series devices and has the following characteristics.

1.1. Physical Dimensions

- Length: 40 mm
- Width: 32.2 mm
- Thickness: 6.3 mm

Note: The Q2668 has an X/Y form-factor compatible with the Q2686/87 Refreshed embedded module range.

1.2. General Features

The following table lists the Q2668 embedded module features.

Table 1. Q2668 Embedded Module Features

Feature	Description
Shielding	The Q2668 embedded module has complete body shielding.
Intelligent Embedded Module Control	• Full set of AT commands for GSM/GPRS/EGPRS including GSM 07.07 and 07.05 AT command sets • Status indication for GSM
GSM/DCS Output Power	• Class 4 (2 W) for E-GSM • Class 1 (1 W) for DCS
GPRS	• GPRS multislot class 10 • Multislot class 2 supported • PBCCH support • Coding schemes: CS1 to CS4
EGPRS	• EGPRS multislot class 10 • Multislot class 2 supported • PBCCH support • Coding schemes MCS5 to MCS9
Voice	• GSM Voice Features with Emergency calls 118 XXX • Full Rate (FR)/ Enhanced Full Rate (EFR) / Half Rate (HR) / Adaptive Multi Rate (AMR) • Echo cancellation and noise reduction • Full duplex Hands free
SMS	• SMS MT, MO • SMS CB • SMS storage into SIM card

Feature	Description
GSM Supplementary Services	• Call Forwarding, Call Barring • Multiparty • Call Waiting, Call Hold
Data/Fax	• Data circuit asynchronous, transparent, and non-transparent up to 14400 bits/s
SIM Interface	• 1.8V/3V SIM interface • SIM Tool Kit Release 99
Real Time Clock	Real Time Clock (RTC) with calendar

1.3. Approvals & Quality

- The Q2668 is compliant with Regulatory: SRRC directive
- Manufacturing: ISO9001/14001

1.4. Telecom Features

- 3GPPTDD Release 5 HSDPA Compliant
  - Dual mode TD-SCDMA/EDGE 2010-2025/1880-1920/1800/900 MHz Downlink data rates up to 2.8Mbps in HSDPA mode
- Uplink data rates up to 384kbps in TD-SCDMA mode
- GPRS class 10
  - EDGE (E-GPRS) multi-slot class 10
- Dual mode with fully automated handover between 2G and 3G networks
- Voice: HR, FR and EFR; Adaptive multi-rate AMR in GSM

1.5. Interfaces

- Digital section running under 2.9 volts and 1.8 volts
- 3V/1V8 USIM interface
- Complete interfacing:
  - Power supply
  - Serial link
  - Analog audio
  - PCM digital audio
  - USIM card
  - Keyboard
  - USB 2.0 slave FS
  - Serial LCD (not available with AT commands)

1.6. Connection Interfaces

The Q2668 has the following external connections:

- Two solutions for main RF antenna connection
  - UFL connector
  - Soldered connection
- Analog and digital interfaces
  - 100-pin I/O connector

1.7. Operating System

- Real Time Clock (RTC) with calendar
- Battery charger
- Echo cancellation + noise reduction (quadri codec)
- Full GSM or GSM/GPRS/EGPRS Operating System stack

2. Functional Specifications

2.1. Functional Architecture

The global architecture of the Q2668 is described in the figure below.

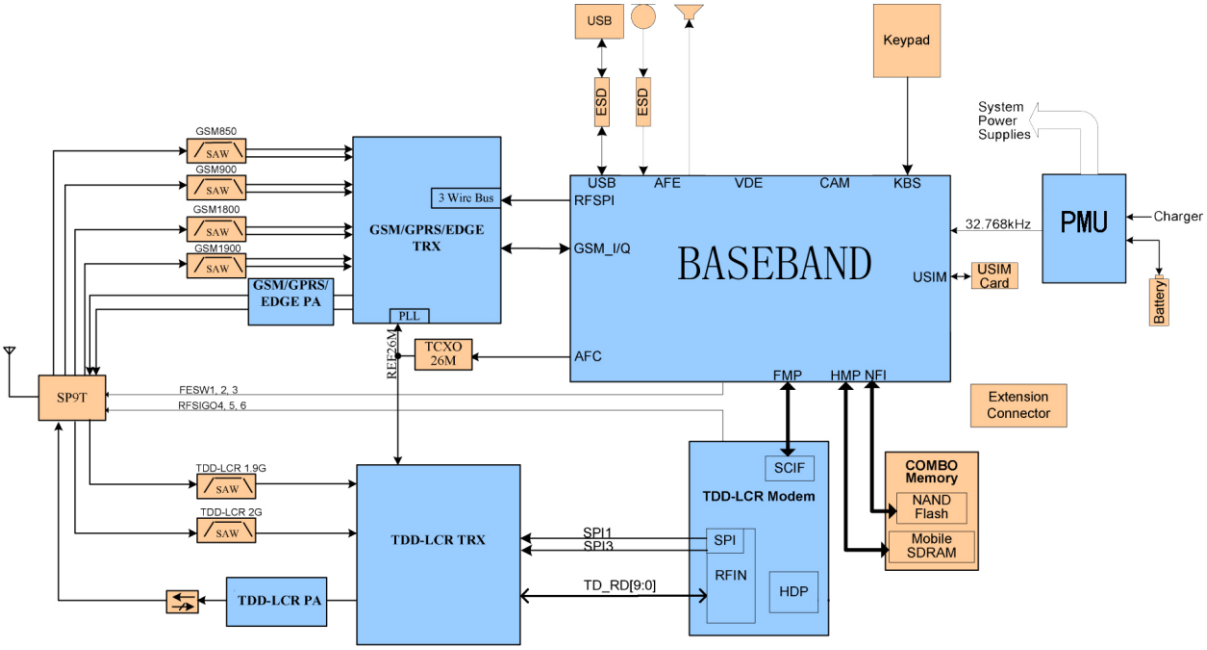


Figure 1. Functional Architecture

2.2. RF Functionalities

The Radio Frequency (RF) range complies with Phase II EGSM 900/DCS 1800 recommendations. The frequency range for the transmit band and the receive band are given in the table below.

Table 2. RF Frequency Ranges

RF Bandwidth	Transmit band (Tx)	Receive band (Rx)
E-GSM 900	880 to 915 MHz	925 to 960 MHz
DCS 1800	1710 to 1785 MHz	1805 to 1880 MHz
TD-SCDMA Band I	1880 to 1920MHz	
TD-SCDMA Band I	2010 to 2025MHz	

The Radio Frequency (RF) component is based on a specific quad-band chip with a:

- Direct down conversion Rx architecture
- Linear direct up-conversion Tx architecture
- On chip Tx power control
- Analog I/Q base band interface for all modes
- On chip multi-band true Rx diversity

2.3. Application Processor

The Q2668 supports the complete family of software Plug-Ins.

- ARM926EJ-S 32 bit processor
- 208MHz operation
- Internal Memory (32 kbyte instruction cache and 32 kbyte data cache)
- Supports multiple interfaces including SPI, I^2C, UART, USB, Audio, etc.

2.4. Operating System

- Linux
- WinCE 5.0/6.0
- Window XP/Vista
- Windows 7

The operating system allows for the Q2668 Embedded Module to be controlled by AT commands. However, some interfaces in the Q2668 embedded module may still not be available even with AT command control as these interfaces are dependent on the peripheral devices connected to the Q2668 embedded module.

3. Technical Specifications

3.1. Power Supply

3.1.1. Design Requirements

The power supply is one of the key issues in the design of a GSM terminal and careful attention should be paid to the following when designing with the Q2668:

- Quality of the power supply
  - Linear regulation (recommended) or PWM (Pulse Width Modulation) converters (usable) are preferred for low noise.
  - PFM (Power Frequency Modulation) or PSM (Phase Shift Modulation) systems must be avoided.
- Capacity to deliver high current peaks in a short time (bursted radio emission).
- The VBATT line must support peak currents with an acceptable voltage drop which guarantees a minimal VBATT value of 3.7V (lower limit of VBATT).

For PCB design constraints related to power supply tracks, ground planes and shielding, refer to section 10 Design Guidelines.

Refer to the following table for the voltage values that are needed to guarantee normal functioning of the Q2668.

Table 3. Input Power Supply Voltage

	V_{min}	V_{nom}	V_{max}
VBATT[1,2]	3.7V	4.0V	4.8V

1 This value must be guaranteed during the burst (with **1.6A** (TBD) Peak in GSM or GPRS mode).

2 Maximum operating Voltage Stationary Wave Ratio (VSWR) 2:1.

3.1.2. Constraints and Recommendations

Only VBATT (external power supply source) input is necessary to supply the Q2668. VBATT also provides for the following functions:

- Directly supplies the RF components with 4.0V*.
- Internally used to provide through several regulators, the power supplies VCC_2V9 and VCC_1V8, which are needed for the baseband signals.

Note: * *It is essential to keep a minimum voltage ripple at this connection in order to avoid any phase error or spectrum modulation degradation. On the other hand, insufficient power supply could dramatically affect some RF performances such as TX power, modulation spectrum, EMC performance, spurious emission and frequency error.*

Due to the burst emission mode used in GSM/GPRS/EGPRS, the power supply must be able to deliver high current peaks in a short time. During the peaks, the ripple (U_{ripp}) on the supply voltage must not exceed a certain limit (Refer to Table 3 Input Power Supply Voltage).

Listed below are the corresponding radio burst rates in communication mode:

- GSM/GPRS class 2 terminals emit 577µs radio bursts every 4.615ms (refer to Figure 2 Power Supply During GSM Burst Emission)
- GPRS class 10 terminals emit 1154µs radio bursts every 4.615ms

In communication mode, the RF Power Amplifier current (1.6A peak in GSM /GPRS mode) flows with a ratio of:

- 1/4 of the time (around 1154µs every 4.615ms for GSM /GPRS cl 10 – 3RX/2TX)

  with the rising time at around 10µs.

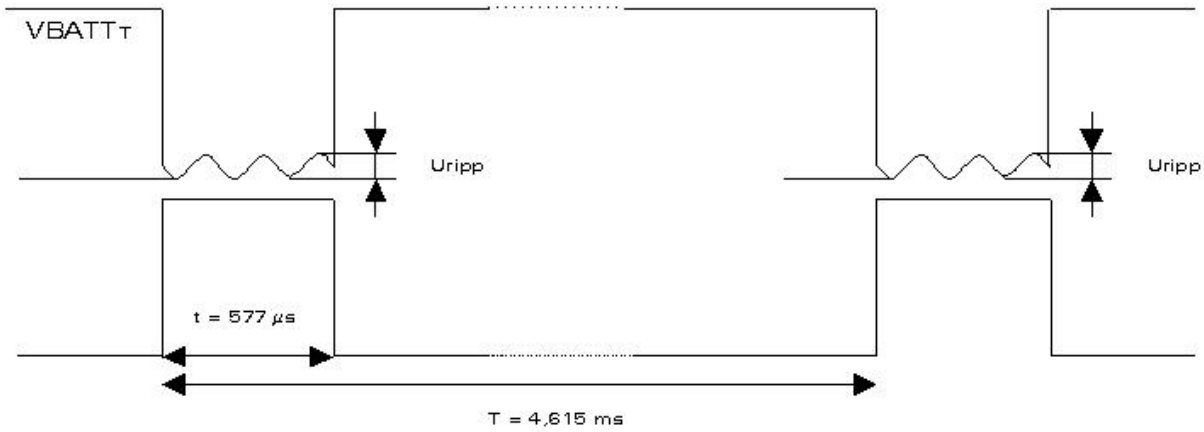


Figure 2. Power Supply During GSM Burst Emission

As the radio power amplifier is directly connected to VBATT, the Q2668 is sensitive to any alternative current on its lines. When a DC/DC converter is used, Sierra Wireless recommends setting the converter frequency in such a way that the resulting voltage does not exceed the values in the following table.

Table 4. Maximum Voltage Ripple (U_{ripp}) vs. Frequency

Frequency (Hz)	U_{ripp} Max (mVpp)
f ≤ 300	200 (TBD)
300 < f ≤ 800	10 (TBD)
800 < f ≤ 1100	30 (TBD)
f > 1100	60 (TBD)

Refer to the following list for other electrical constraints, recommendations and design requirements.

- Recommendations:
  - Peak Maximum Current = 1.6A
  - Operational Average Maximum Current = 500mA
- The Q2668 shielding case is the grounding. The ground must be connected to the motherboard through a complete layer on the PCB.
- When the Q2668 is supplied with a battery, the total impedance (battery + protections + PCB) should be < 150 mΩ.
- When the Q2668 is in Alarm/Off mode, no voltage has to be applied on any pin of the 100-pin connector, except on VBATT (pins 1 to 4), BAT-RTC (pin 7) for RTC operation or ON/~OFF (pin 19) to power-ON the Q2668.

3.1.3. Power Supply Pin-out

Table 5. Power Supply Pin-Out

Signal	Pin Number
VBATT	1, 2, 3, 4
GND	Shielding

Caution: *The grounding connection is made through the shielding. That is, the four leads must be soldered to the ground plane.*

3.1.4. Decoupling of Power Supply Signals

Decoupling capacitors on VBATT lines are embedded in the Q2668. Hence, it should not be necessary to add decoupling capacitors close to the Q2668.

However, in case of EMI/RFI problem, VBATT signal may require some EMI/RFI decoupling: parallel 33pF capacitors and a 0.1µF close to the Q2668 or a serial ferrite bead (or both to get better results) may be used. Low frequency decoupling capacitors (220µF to 2.2mF) may be used to reduce the voltage ripple.

Caution: *When ferrite beads are used, the recommendation given for the power supply connection must be followed with care (high current capacity and low impedance).*

3.2. Mechanical Specifications

3.2.1. Physical Characteristics

The Q2668 has a complete self-contained shield.

- Overall dimensions : 32.2 x 40 x 6.3 mm (excluding shielding pins)
- Weight : 11±1 g

3.2.2. Mechanical Drawing

The mechanical specifications of the Q2668 are shown in the following diagram.

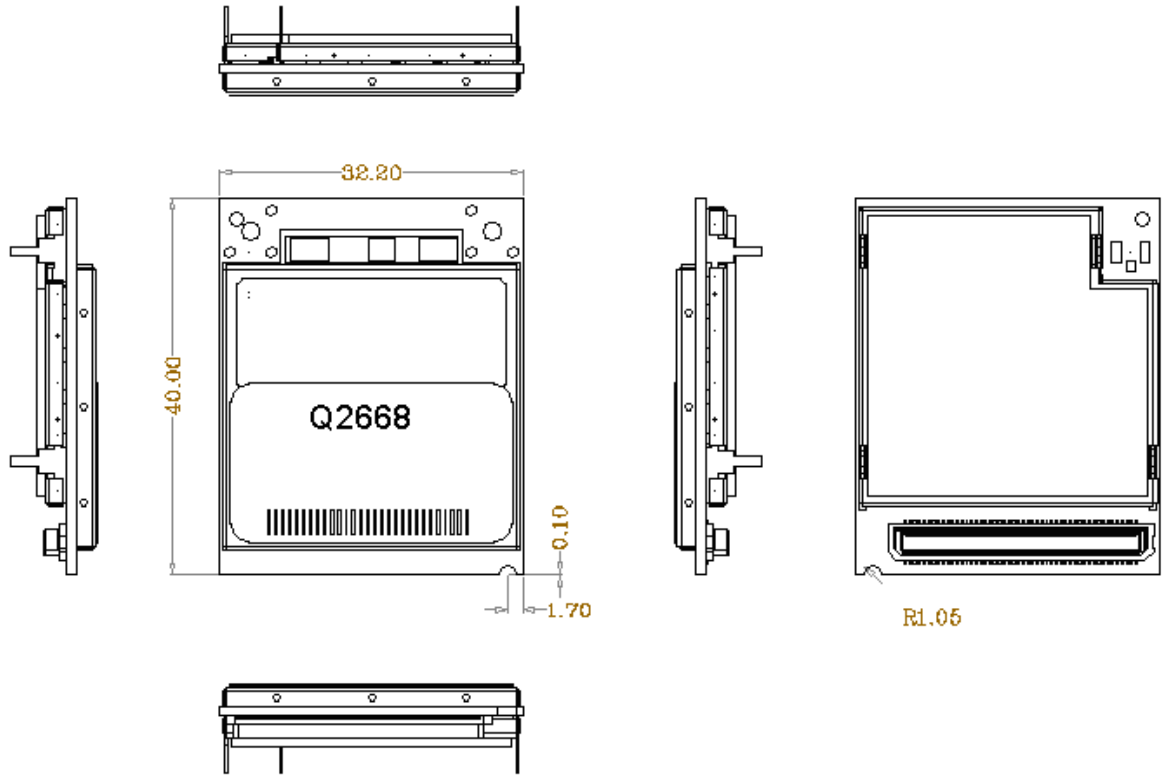


Figure 3. Mechanical Drawing

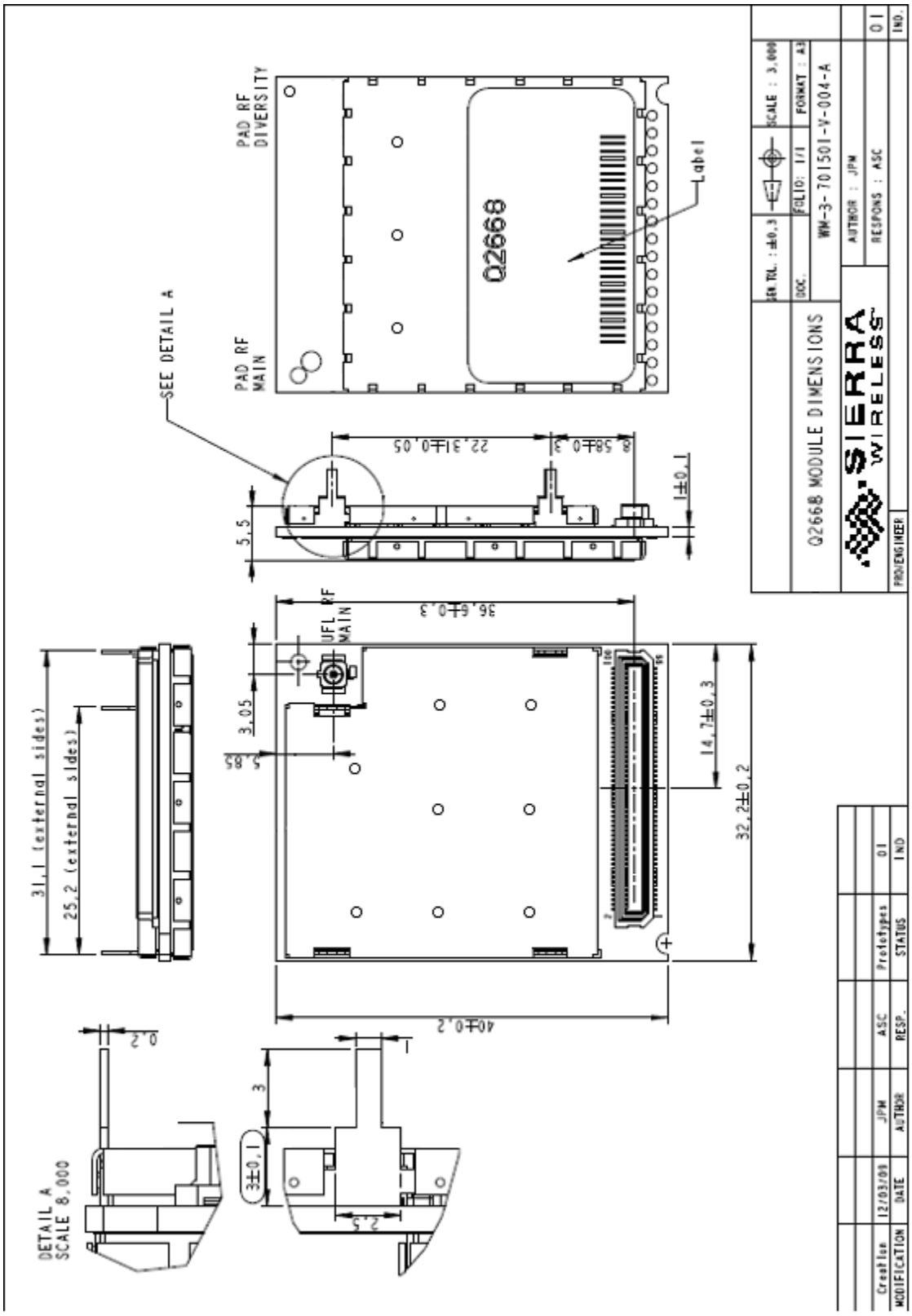


Figure 4. Maximum Bulk Occupied on the Host Board

3.3. Firmware Upgrade

The firmware upgrade process consists of downloading GSM/GPRS/EGPRS software into the corresponding internal flash memories of the Q2668 Intelligent Embedded Module.

Downloading is done through either of the following:

- USB
- Main Serial link port (UART1) using 4-wire interface (CT103-TXD1, CT104-RXD1, ~CT105-RTS1, ~CT106-CTS1)

while connected to a PC using a download tool.

Consequently, it is very important to plan and define easy access to these signals during the hardware design of the application board. For more information about these signals, refer to section 4.6 Main Serial Link (UART1).

4. Interfaces

4.1. General Purpose Connector (GPC)

A 100-pin connector is provided to interface the Q2668 with a board containing a serial LCD, a keyboard, a USIM connector, or a battery connection.

4.1.1. Pin Description

Table 6. General Purpose Pin Description

Description	I/O*	Voltage	Signal Name		Pin Number		Signal Name		Voltage	I/O*	Description
			Mux	Nominal			Nominal	Mux			
Power Supply	I	VBATT		VBATT	1	2	VBATT		VBATT	I	Power Supply
Power Supply	I	VBATT		VBATT	3	4	VBATT		VBATT	I	Power Supply
1.8V Supply Output	O	VCC_1V8		VCC_1V8	5	6	CHG-IN		CHG-IN	I	Charger input
RTC Battery connection	I/O	BAT-RTC		BAT-RTC	7	8	CHG-IN		CHG-IN	I	Charger input
USIM Power Supply	O	1V8 or 3V		SIM-VCC	9	10	VCC_2V9		VCC_2V9	O	2.9V Supply Output
USIM Data	I/O	1V8 or 3V		SIM-IO	11	12	NC				Not Connected
USIM reset	O	1V8 or 3V		~SIM-RST	13	14	SIM-CLK		1V8 or 3V	O	USIM Clock
Buzzer Output	O	Open Drain		BUZZER0	15	16	BOOT		VCC_1V8	I	Not Used
LED0 Output	O	Open Drain		LED0	17	18	~RESET		VCC_1V8	I/O	RESET Input
ON / ~OFF Control	I	MAX(VBATT/ CHG-IN)		ON/~OFF	19	20	BAT-TEMP		Analog	I	Analog temperature
Analog to Digital Input	I	Analog		ADC2	21	22	GPIO31	SPI1-LOAD	VCC_2V9	I/O	
SPI1 Clock	O	VCC_2V9	GPIO28	SPI1-CLK	23	24	SPI1-I	GPIO30	VCC_2V9	I	SPI1 Data Input
SPI1 Data Output	I/O	VCC_2V9	GPIO29	SPI1-IO	25	26	SPI2-CLK	GPIO32	VCC_2V9	O	SPI2 Clock
SPI2 Data Output	I/O	VCC_2V9	GPIO33	SPI2-IO	27	28	GPIO35	SPI2-LOAD	VCC_2V9	I/O	
SPI2 Data Input	I	VCC_2V9	GPIO34	SPI2-I	29	30	CT104-RXD2	GPIO15	VCC_1V8	O	Auxiliary RS232 Receive
Auxiliary RS232 Transmit	I	VCC_1V8	GPIO14	CT103-TXD2	31	32	CT106-CTS2	GPIO16	VCC_1V8	O	Auxiliary RS232 Clear to Send

Description	I/O*	Voltage	Signal Name		Pin Number		Signal Name		Voltage	I/O*	Description
			Mux	Nominal			Nominal	Mux			
Auxiliary RS232 Request to Send	I	VCC_1V8	GPIO17	CT105-RTS2	33	34	MIC2N		Analog	I	Micro 2 Input Negative
Speaker 1 Output Positive	O	Analog		SPK1P	35	36	MIC2P		Analog	I	Micro 2 Input Positive
Speaker 1 Output Negative	O	Analog		SPK1N	37	38	MIC1N		Analog	I	Micro 1 Input Negative
Speaker 2 Output Positive	O	Analog		SPK2P	39	40	MIC1P		Analog	I	Micro 1 Input Positive
Speaker 2 Output Negative	O	Analog		SPK2N	41	42	NC				Not Connected
General Purpose Input/Output	I/O	VCC_2V9		GPIO0	43	44	SCL1	GPIO26	VCC_2V9	O	I²C Clock
General Purpose Input/Output	I/O	VCC_2V9		GPIO19	45	46	SDA1	GPIO27	VCC_2V9	I/O	I²C Data
General Purpose Input/Output	I/O	VCC_2V9		GPIO21	47	48	GPIO20		VCC_2V9	I/O	
Interruption 1 Input	I	VCC_2V9	GPIO25	INT1	49	50	INT0	GPIO3	VCC_1V8	I	Interruption 0 Input
Interruption 2 Input	I/O	VCC_1V8	GPIO1	INT2	51	52	VPAD-USB		VPAD-USB	I	USB Power supply input
General Purpose Input/Output	I/O	VCC_1V8		GPIO2	53	54	USB-DP		VPAD-USB	I/O	USB Data
General Purpose Input/Output	I/O	VCC_2V9	**	GPIO23	55	56	USB-DM		VPAD-USB	I/O	USB Data
General Purpose Input/Output	I/O	VCC_2V9	**	GPIO22	57	58	GPIO24		VCC_2V9	I/O	
Keypad Column 0	I/O	VCC_1V8	GPIO4	COL0	59	60	COL1	GPIO5	VCC_1V8	I/O	Keypad Column 1
Keypad Column 2	I/O	VCC_1V8	GPIO6	COL2	61	62	COL3	GPIO7	VCC_1V8	I/O	Keypad Column 3
Keypad Column 4	I/O	VCC_1V8	GPIO8	COL4	63	64	ROW4	GPIO13	VCC_1V8	I/O	Keypad Row 4
Keypad Row 3	I/O	VCC_1V8	GPIO12	ROW3	65	66	ROW2	GPIO11	VCC_1V8	I/O	Keypad Row 2
Keypad Row 1	I/O	VCC_1V8	GPIO10	ROW1	67	68	ROW0	GPIO9	VCC_1V8	I/O	Keypad Row 0
General Purpose Input/Output	O	VCC_2V9		GPIO42	69	70	GPIO43		VCC_2V9	O	General Purpose Input/Output
Main RS232 Transmit	I	VCC_2V9	GPIO37	CT103-TXD1	71	72	~CT105-RTS1	GPIO39	VCC_2V9	I	Main RS232 Request To Send
Main RS232 Receive	O	VCC_2V9	GPIO36	CT104-RXD1	73	74	~CT107-DSR1	GPIO40	VCC_2V9	O	Main RS232 Data Set Ready
Main RS232 Clear To Send	O	VCC_2V9	GPIO38	~CT106-CTS1	75	76	~CT108-2-DTR1	GPIO41	VCC_2V9	I	Main RS232 Data Terminal Ready
PCM Frame Synchro	O	VCC_1V8		PCM-SYNC	77	78	PCM-IN		VCC_1V8	I	PCM Data Input
PCM Clock	O	VCC_1V8		PCM-CLK	79	80	PCM-OUT		VCC_1V8	O	PCM Data Output
Not Connected				NC	81	82	DAC0		Analog	O	Digital to Analog Converter
General Purpose Input/Output		VCC_1V8		GPIO44	83	84	NC				Not Connected
Not Connected				NC	85	86	NC				Not Connected
Not Connected				NC	87	88	NC				Not Connected
Not Connected				NC	89	90	NC				Not Connected
Not Connected				NC	91	92	NC				Not Connected

Description	I/O*	Voltage	Signal Name		Pin Number		Signal Name		Voltage	I/O*	Description
			Mux	Nominal			Nominal	Mux			
Not Connected				NC	93	94	NC				Not Connected
Not Connected				NC	95	96	NC				Not Connected
Not Connected				NC	97	98	NC				Not Connected
Not Connected				NC	99	100	NC				Not Connected

NC shows there's no need to use this pin.

***** The I/O direction information is only for the nominal signal. When the signal is configured in GPIO, it can always be an Input or an Output.

****** For more information about the multiplexing of these signals, refer to section 4.3 General Purpose Input/Output.

Refer to section 4.2 Electrical Information for Digital I/O for open drain, 2V9 and 1V8 voltage characteristics and reset state definitions.

4.2. Electrical Information for Digital I/O

The three types of digital I/O on the Q2668 are:

- 2.9Volt CMOS
- 1.8Volt CMOS
- Open drain

Refer to the tables below for the electrical characteristics of these three digital I/Os.

Table 7. Electrical Characteristics for a 2.9 Volt Type (2V9) Digital I/O

Parameter		I/O Type	Minimum	Typical	Maximum	Condition
Internal 2.9V power supply		VCC_2V9	2.75V	2.9V	2.95V	
Input/Output pin	V_{IL}	CMOS	0V	0V	0.3V	
	V_{IH}	CMOS	2.75V	2.9V	2.9V	
	V_{OL}	CMOS	0V	0V	0.1V	
	V_{OH}	CMOS	2.75V	2.9V	3.0V	
	I_{OH}		6.6mA			
	I_{OL}		3.1mA			

All 2.9V I/O pins do not accept input signal voltage above the maximum voltage specified above, except for the UART1 interface, which is 3.3V tolerant.

Table 8. Electrical Characteristics of a 1.8 Volt type (1V8) Digital I/O

Parameter		I/O Type	Minimum	Typical	Maximum	Condition
Internal 1V8 power supply		VCC_1V8	1.7V	1.8V	1.9V	
Input/Output pin	V_{IL}	CMOS	0V	0V	0.2V	
	V_{IH}	CMOS	1.7V	1.8	1.8V	
	V_{OL}	CMOS	0V	0V	0.1V	
	V_{OH}	CMOS	1.7V	1.8V	1.8V	
	I_{OH}		1.4mA			
	I_{OL}		2.7mA			

Table 9. Electrical Characteristics of an Open Drain Digital I/O

Signal Name	Parameter	I/O Type	Minimum	Typical	Maximum	Condition
LED0	V_{OL}	Open Drain			0.4V	
	I_{OL}	Open Drain	10mA		20mA	
BUZZER0	V_{OL}	Open Drain			0.1V	
	I_{OL}	Open Drain	20mA		100mA	
SDA1/GPIO27	V_{TOL}	Open Drain			3.3V	Tolerated voltage
	V_{IH}	Open Drain	2.9V			

Signal Name	Parameter	I/O Type	Minimum	Typical	Maximum	Condition
and SCL1/GPIO26	V_{IL}	Open Drain			0.4V	
	V_{OL}	Open Drain			0.4V	
	I_{OL}	Open Drain			3mA	

The reset states of the I/Os are given in each interface description chapter. Definitions of these states are given below.

Table 10. Reset State Definition

Parameter	Definition
0	Set to GND
1	Set to supply to 1V8 or 2V9 depending on I/O type
Pull-down	Internal pull-down
Pull-up	Internal pull-up
Z	High impedance
L	Low level
H	High level
L WEAK	Low weak level
H WEAK	High weak level
-	Not steady
Undefined	**Caution:** *Undefined must not be used in an application if a special state is required at reset. These pins may be a toggling a signal during reset.*

4.3. General Purpose Input/Output

The Q2668 provides up to 45 General Purpose I/Os, used to control any external device such as an LCD or a keyboard backlight.

Table 11. GPIO Pin Description

Pin Number	Signal	I/O	I/O Type	Reset State	Multiplexed With
43	GPIO0	I/O	2V9	-	Not mux
51	GPIO1	I/O	1V8	-	~CS2 / INT2
53	GPIO2	I/O	1V8	-	A24
50	GPIO3	I/O	1V8	-	INT0
59	GPIO4	I/O	1V8	L WEAK	COL0
60	GPIO5	I/O	1V8	L WEAK	COL1
61	GPIO6	I/O	1V8	L WEAK	COL2
62	GPIO7	I/O	1V8	L WEAK	COL3
63	GPIO8	I/O	1V8	L WEAK	COL4
68	GPIO9	I/O	1V8	H	ROW0
67	GPIO10	I/O	1V8	H	ROW1
66	GPIO11	I/O	1V8	H	ROW2
65	GPIO12	I/O	1V8	H	ROW3

Pin Number	Signal	I/O	I/O Type	Reset State	Multiplexed With
64	GPIO13	I/O	1V8	H	ROW4
30	GPIO14	I/O	1V8	-	CT103-TXD2
31	GPIO15	I/O	1V8	-	CT104-RXD2
33	GPIO16	I/O	1V8	-	~CT106-CTS2
32	GPIO17	I/O	1V8	-	~CT105-RTS2
12	GPIO18	I/O	1V8	-	SIMPRES
45	GPIO19	I/O	2V9	-	Not mux
48	GPIO20	I/O	2V9	-	Not mux
47	GPIO21	I/O	2V9	-	Not mux
57	GPIO22	I/O	2V9	-	Not mux
55	GPIO23	I/O	2V9	-	Not mux
58	GPIO24	I/O	2V9	-	Not mux
49	GPIO25	I/O	2V9	-	INT1
44	GPIO26	I/O	Open drain	-	SCL1
46	GPIO27	I/O	Open drain	-	SDA1
23	GPIO28	I/O	2V9	-	SPI1-CLK
25	GPIO29	I/O	2V9	-	SPI1-IO
24	GPIO30	I/O	2V9	-	SP1-I
22	GPIO31	I/O	2V9	-	SPI1_LOAD
26	GPIO32	I/O	2V9	L WEAK	SPI2-CLK
27	GPIO33	I/O	2V9	-	SPI2-IO
29	GPIO34	I/O	2V9	-	SPI2-I
28	GPIO35	I/O	2V9	-	SPI2_LOAD
73	GPIO36	I/O	2V9	-	CT103-TXD1
71	GPIO37	I/O	2V9	-	CT104-RXD1
75	GPIO38	I/O	2V9	-	~CT105-RTS1
72	GPIO39	I/O	2V9	-	~CT106-CTS1
76	GPIO40	I/O	2V9	-	~CT107-DSR1
74	GPIO41	I/O	2V9	-	~CT108-2-DTR1
69	GPIO42	I/O	2V9	H WEAK	~CT125
70	GPIO43	I/O	2V9	-	~CT109
83	GPIO44	I/O	2V9	-	PWM1 / ~CS3

Refer to section 4.2 Electrical Information for Digital I/O for open drain, 2V9 and 1V8 voltage characteristics and reset state definitions.

4.4. Serial Interface

The Q2668 provides two SPI buses (i.e. for LCD, memories, etc.) and an I^2C 2-wire interface.

4.4.1. SPI Bus

Both SPI bus interfaces include:

- A CLK signal (SPIx-CLK)
- An O signal (SPIx-O)
- An I signal (SPIx-I)
- A CS (Chip Select) signal complying with the standard SPI bus (any GPIO)
- An optional Load signal (only the SPIx-LOAD signal)

4.4.1.1. Characteristics

The following lists the features available on the SPI bus:

- Master mode operation
- The CS signal may be any GPIO
- The LOAD signal (optional) is used for the word handling mode (only the SPIx-LOAD signal)
- SPI speed is from 50 Kbit/s to 26 Mbit/s in master mode operation
- 3 or 4-wire interface (5-wire possible with the optional SPIx-LOAD signal)
- SPI-mode configuration: 0 to 3
- 1 to 16 bits data length

4.4.1.2. SPI Waveforms

The figure below shows the waveforms for SPI transfers with a 4-wire configuration in master mode 0.

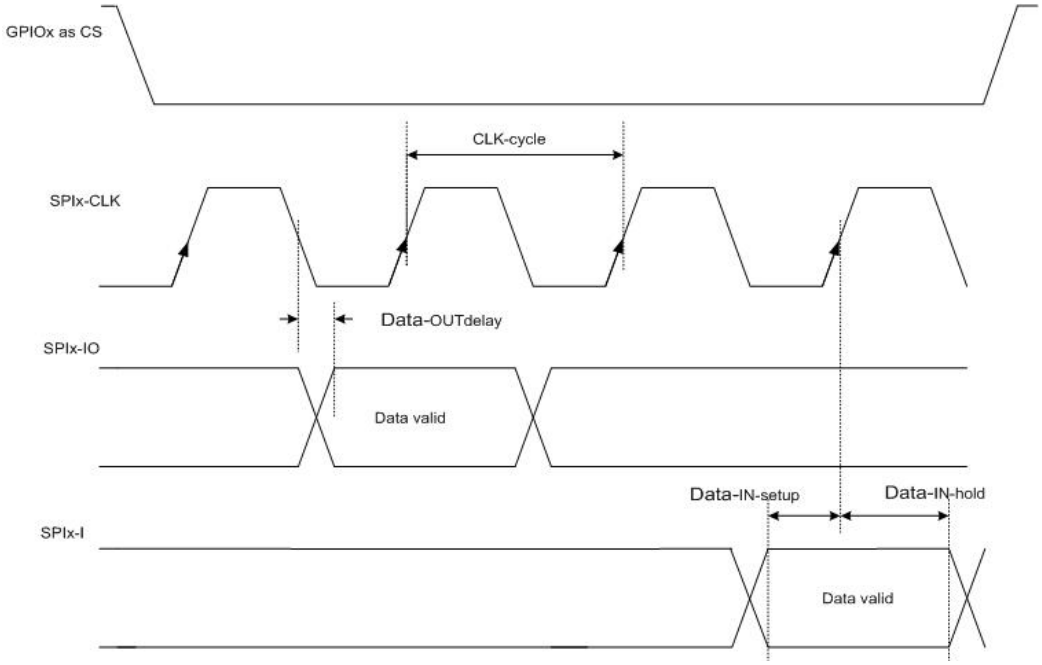


Figure 5. SPI Timing Diagram; Mode 0, Master, 4 wires

Table 12. AC Characteristics of the SPI Bus

Signal	Description	Minimum	Typ	Maximum	Unit
CLK-cycle	SPI clock frequency	0.05		26	MHz
Data-OUT delay	Data out ready delay time			10	ns
Data-IN-setup	Data in setup time	2			ns
Data-OUT-hold	Data out hold time	2			ns

The following figure shows the waveforms for SPI transfer with the LOAD (SPIx-LOAD) signal configuration in master mode 0 (chip select is not represented).

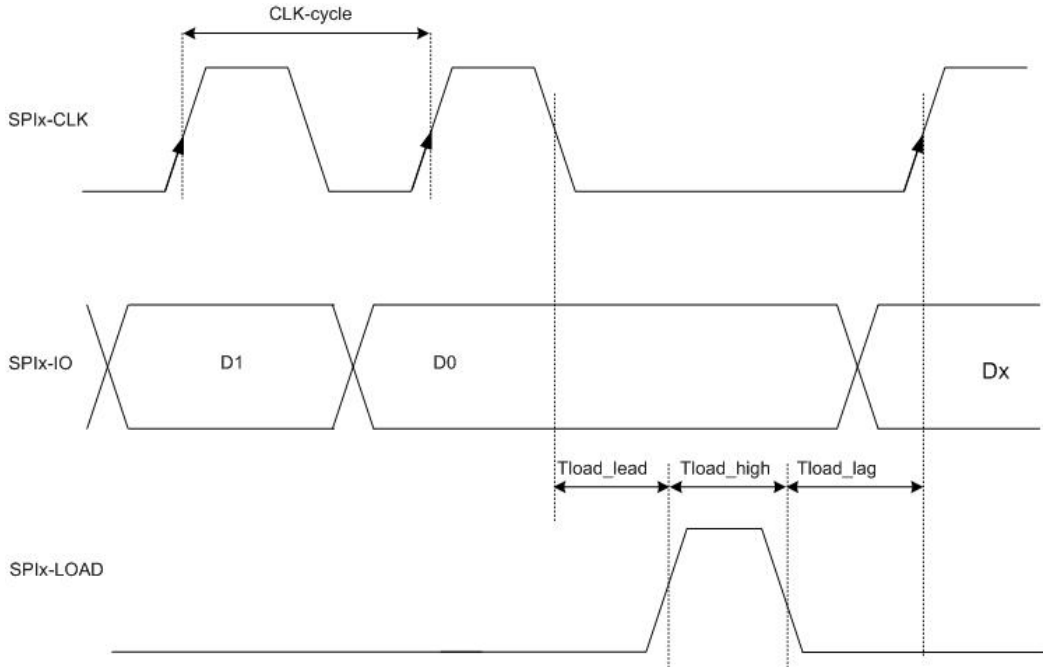


Figure 6. SPI Timing Diagrams with SPIx-LOAD Signal; Mode 0, Master, 4 wires

4.4.1.3. SPI1 Bus Pin Description

Table 13. SPI1 Pin Description

Pin Number	Signal	I/O	I/O Type	Reset State	Description	Multiplexed With
22	SPI1-LOAD	O	2V9	-	SPI load	GPIO31
23	SPI1-CLK	O	2V9	-	SPI Serial Clock	GPIO28
24	SPI1-I	I	2V9	-	SPI Serial input	GPIO30
25	SPI1-IO	O	2V9	-	SPI Serial input/output	GPIO29

Refer to section 4.2 Electrical Information for Digital I/O for open drain, 2V9 and 1V8 voltage characteristics and reset state definitions.

4.4.1.4. SPI2 Bus Pin Description

Table 14. SPI2 Pin Description

Pin Number	Signal	I/O	I/O Type	Reset State	Description	Multiplexed With
26	SPI2-CLK	O	2V9	-	SPI Serial Clock	GPIO32
27	SPI2-IO	I/O	2V9	-	SPI Serial input/output	GPIO33
28	SPI2-LOAD	O	2V9	-	SPI Load	GPIO35
29	SP2-I	I	2V9	-	SPI Serial input	GPIO34

Refer to section 4.2 Electrical Information for Digital I/O for open drain, 2V9 and 1V8 voltage characteristics and reset state definitions.

4.4.1.5. Application

Table 15. SPI Bus Configuration

Operation	Maximum Speed	SPI-Mode	Duplex	3-wire Type	4-wire Type	5-wire Type
Master	26 Mb/s	0, 1, 2, 3	Half	SPIx-CLK; SPIx-IO; GPIOx as CS	SPIx-CLK; SPIx-IO; SPIx-I; GPIOx as CS	SPIx-CLK; SPIx-IO; SPIx-I; GPIOx as CS; SPIx-LOAD (not muxed in GPIO);

4.4.1.5.1. 3-wire Application

For the 3-wire configuration, only SPIx-I/O is used as both input and output.

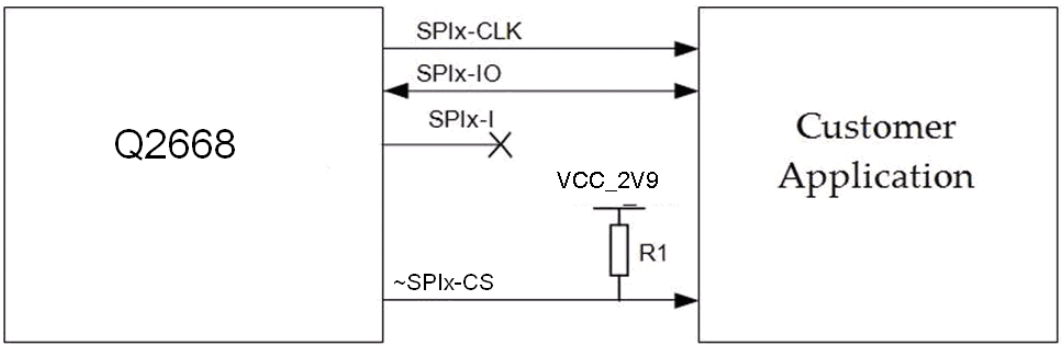


Figure 7. Example of a 3-wire SPI Bus Application

Input and output data lines are disassociated in a 3-wire (SPI bus) serial interface. The SPIx-IO signal is used for both output and input data.

One pull-up resistor, R1, is needed to set the SPIx-CS level for the reset state. The value of R1 depends on the peripheral plugged on the SPIx interface. The recommended value for R1 is 100kΩ.

Except for R1, no external components are needed if the electrical specification of the customer application complies with the Q2668 SPIx interface electrical specification.

The SPIx-I line is not used in a 4-wire configuration. This line can be left open or used as GPIO for other application functionality.

The SPIx interface voltage range is 2.9V. It can be powered either by VCC_2V9 (pin 10) of the Q2668 or by any other power supply.

4.4.1.5.2. 4-wire Application

For the 4-wire configuration, SPIx-I/O is used as output only, and SPIx-I is used as input only.

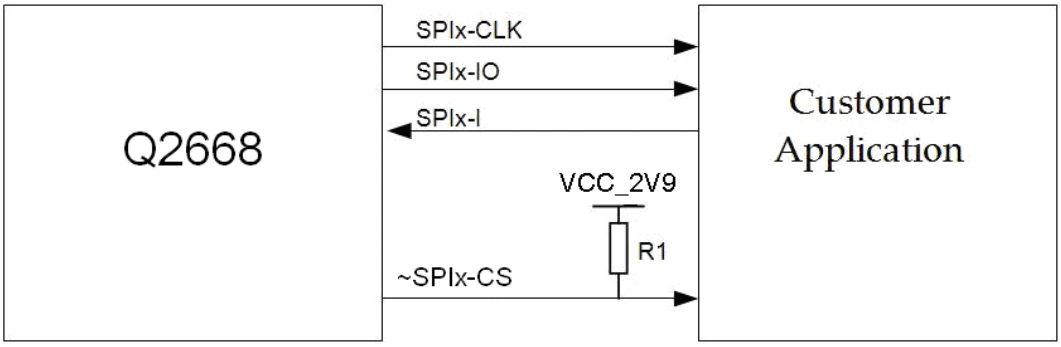


Figure 8. Example of a 4-wire SPI Bus Application

One pull-up resistor, R1, is needed to set the SPIx-CS level for the reset state. The recommended R1 value is 100kΩ.

Except for R1, no external components are needed if the electrical specification of the customer application complies with the Q2668 SPIx interface electrical specification.

4.4.1.5.3. 5-wire Application

For the 5-wire configuration, SPIx-I/O is used as output only and SPIx-I is used as input only. The dedicated SPIx-LOAD signal is also used. It is an additional signal in more than a Chip Select (any other GPIOx).

4.4.2. I^2C Bus

The I^2C interface includes:

- A clock signal **(SCL1)**
- A data signal **(SDA1)** that is compliant with max 100Kbit/s standard interface (standard mode: s-mode).

The I^2C bus is always master; and the maximum speed transfer range is 400Kbit/s (fast mode: f-mode).

For more information on the I^2C bus interface, refer to document [4] "I2C Bus Specification and User Guide", Version 3.0, NXP 2007.

4.4.2.1. I²C Waveforms

The figure below shows the I²C bus waveform in master mode configuration.

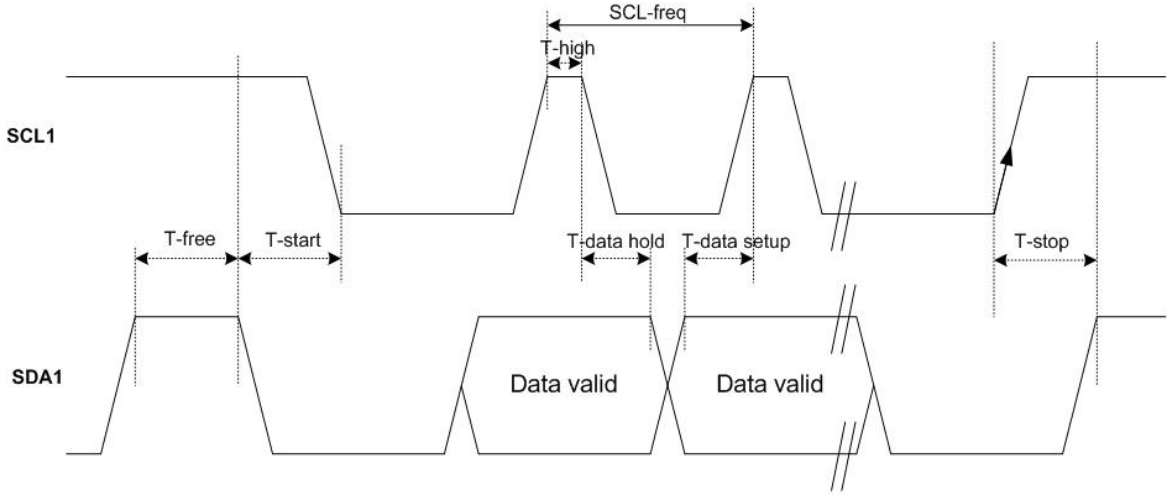


Figure 9. I²C Timing Diagram; Master

Table 16. AC Characteristics of the I²C

Signal	Description	Minimum	Typical	Maximum	Unit
SCL1-freq	I²C clock frequency	0		400	kHz
T-start	Hold time START condition	0.6			ms
T-stop	Setup time STOP condition	0.6			ms
T-free	Bus free time, STOP to START	1.3			ms
T-high	High period for clock	0.6			ms
T-data-hold	Data hold time	0.3			ms
T-data-setup	Data setup time	100			ns

4.4.2.2. I²C Bus Pin Description

Table 17. I²C Pin Description

Pin Number	Signal	I/O	I/O Type	Reset State	Description	Multiplexed With
44	SCL1	O	H	Z	Serial Clock	GPIO26
46	SDA1	I/O	H	Z	Serial Data	GPIO27

Refer to section 4.2 Electrical Information for Digital I/O for open drain, 2V9 and 1V8 voltage characteristics and reset state definitions.

4.4.2.3. Application

The two lines need to be pulled-up to the V_I²C voltage. The V_I²C voltage is dependent on the customer application component connected on the I²C bus. Nevertheless, the VI²C must comply with the Q2668 electrical specification.

The VCC_2V9 (pin 10) of the Q2668 may be used to connect the pull-up resistors, if the I²C bus voltage is 2.9V.

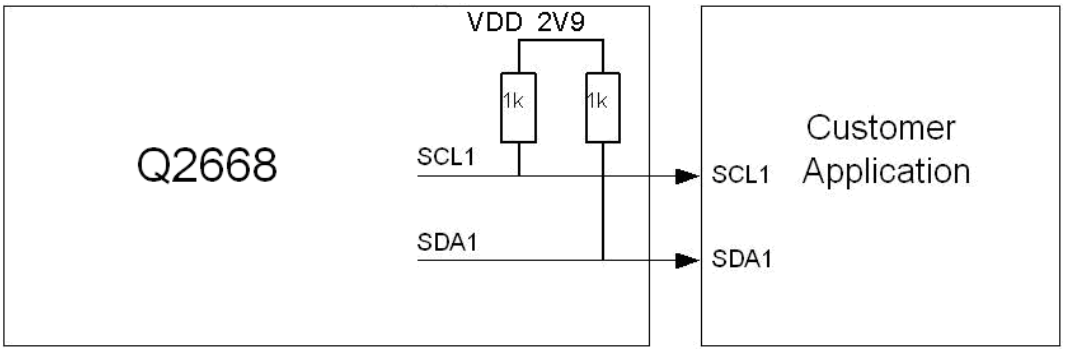


Figure 10. Example of I²C Bus Application

The pull-up resistor values are selected depending on the mode used. For Fast mode, it is recommended to use 1kΩ resistors in order to ensure compliance with I²C specification. For Standard mode, higher values of resistors may be used to save power consumption.

4.5. Keyboard Interface

This interface provides 10 connections:

- 5 rows (ROW0 to ROW4)

  and

- 5 columns (COL0 to COL4)

Scanning is digital and debouncing is performed in the Q2668. No discreet components like resistors or capacitors are needed when using this interface.

4.5.1. Pin Description

Refer to the following table for the pin description of the keyboard interface.

Table 18. Keyboard Interface Pin Description

Pin Number	Signal	I/O	I/O Type	Reset State	Description	Multiplexed With
59	COL0	I/O	1V8	L	Column scan	GPIO4
60	COL1	I/O	1V8	L	Column scan	GPIO5
61	COL2	I/O	1V8	L	Column scan	GPIO6
62	COL3	I/O	1V8	L	Column scan	GPIO7
63	COL4	I/O	1V8	L	Column scan	GPIO8
64	ROW4	I/O	1V8	H	Row scan	GPIO13
65	ROW3	I/O	1V8	H	Row scan	GPIO12

Pin Number	Signal	I/O	I/O Type	Reset State	Description	Multiplexed With
66	ROW2	I/O	1V8	H	Row scan	GPIO11
67	ROW1	I/O	1V8	H	Row scan	GPIO10
68	ROW0	I/O	1V8	H	Row scan	GPIO9

Refer to section 4.2 Electrical Information for Digital I/O for open drain, 2V9 and 1V8 voltage characteristics and reset state definitions.

If one or more GPIOs (of this table) are allocated the keyboard service becomes unavailable.

4.5.2. Application

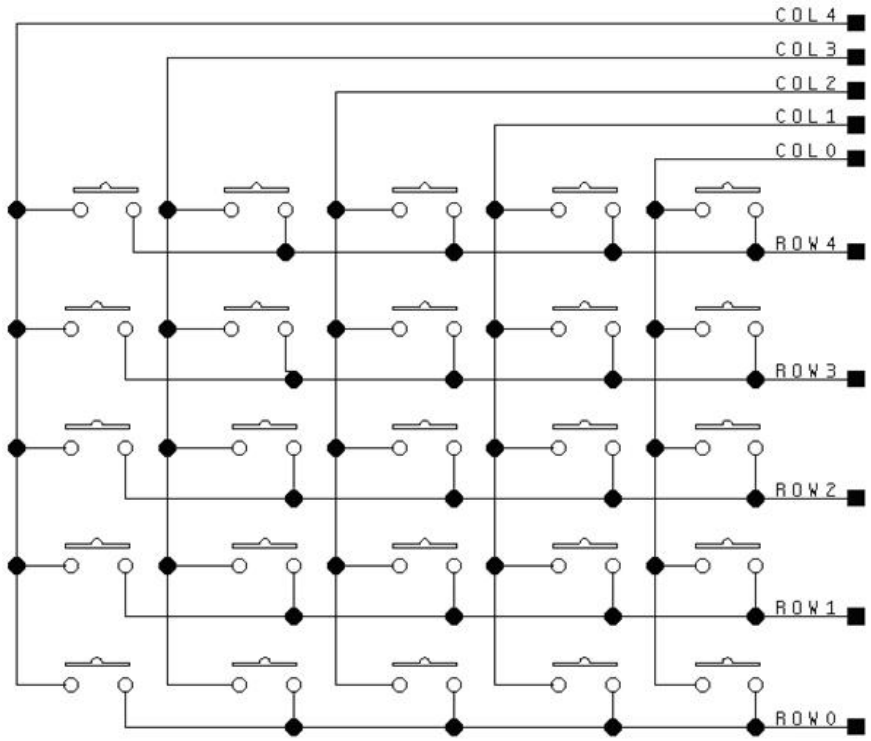


Figure 11. Example of a Keyboard Implementation

4.6. Main Serial Link (UART1)

The main serial link (UART1) is used for communication between the Q2668 and a PC or host processor. It consists of a flexible 6-wire serial interface.

The signals used by UART1 are as follows:

- TX data (CT103-TXD1)
- RX data (CT104-RXD1)
- Request To Send (~CT105-RTS1)
- Clear To Send (~CT106-CTS1)
- Data Terminal Ready (~CT108-2-DTR1)
- Data Set Ready (~CT107-DSR1)

4.6.1. Pin Description

Refer to the following table for the pin description of the UART1 interface.

Table 19. UART1 Pin Description

Pin Number	Signal	I/O	I/O Type	Reset State	Description	Multiplexed With
71	CT103-TXD1	I	2V9	L weak	Transmit serial data	GPIO36
72	~CT105-RTS1	I	2V9	-	Request To Send	GPIO38
73	CT104-RXD1	O	2V9	L weak	Receive serial data	GPIO37
74	~CT107-DSR1	O	2V9	-	Data Set Ready	GPIO40
75	~CT106-CTS1	O	2V9	-	Clear To Send	GPIO39
76	~CT108-2-DTR1	I	2V9	-	Data Terminal Ready	GPIO41
Shielding leads	CT102-GND		GND		Ground	

Refer to section 4.2 Electrical Information for Digital I/O for open drain, 2V9 and 1V8 voltage characteristics and reset state definitions.

The rise and fall time of the reception signals (mainly CT103) must be less than 300ns.

The maximum baud rate of UART1 is 921Kbit/s.

The UART1 interface is 2.9V type, but it is 3.3V tolerant.

Note: The Q2668 is designed to operate using all the serial interface signals. In particular, it is mandatory to use RTS and CTS for hardware flow control in order to avoid data loss/corruption during transmission.

4.6.2. Level Shifter Implementation

The level shifter must be 2.9V with V29 electrical signal compliance.

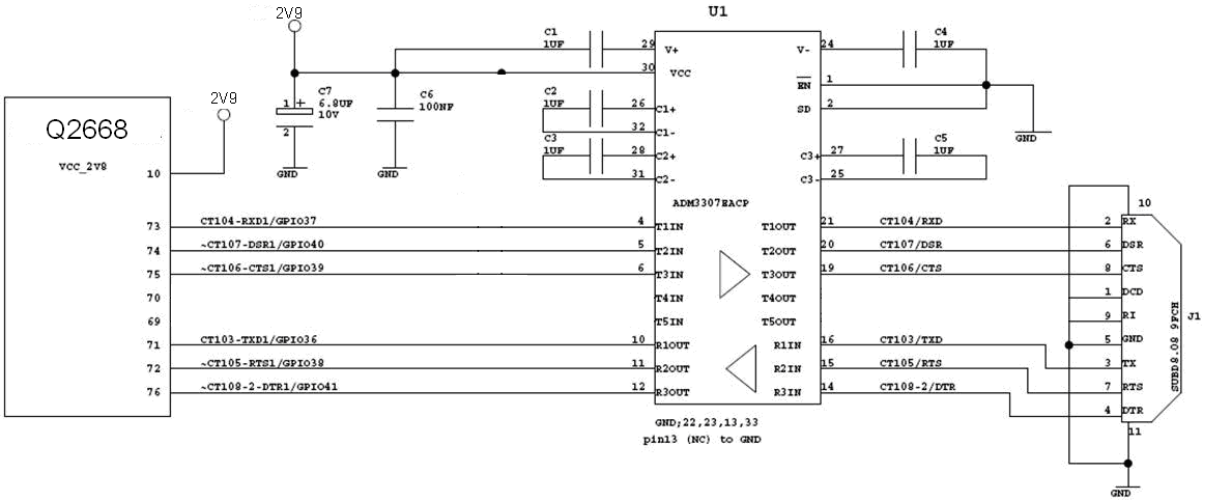


Figure 12. Example of an RS-232 Level Shifter Implementation for UART1

The U1 chip also protects the Q2668 against ESD at 15kV (air discharge).

4.6.2.1. Recommended Components

- C1, C2, C3, C4, C5 :1µF
- C6 :100nF
- C7 :6.8µF TANTAL 10V CP32136 AVX
- U1 :ADM3307AECP Analog devices
- J1 :SUB-D9 female

The ADM3307EACP chip is able to speed up to 921Kb/s. If other level shifters are used, ensure that their speeds are compliant with the UART1 speed.

The ADM3307EACP can be powered either by VCC_2V9 (pin 10) of the Q2668 or by an external regulator at 2.9 volts.

If the UART1 interface is connected directly to a host processor, it is not necessary to use level shifters. The interface can be connected as shown in the following figures.

4.6.3. V24/CMOS Possible Designs

The ~CT107-DSR1 must be configured from low level.

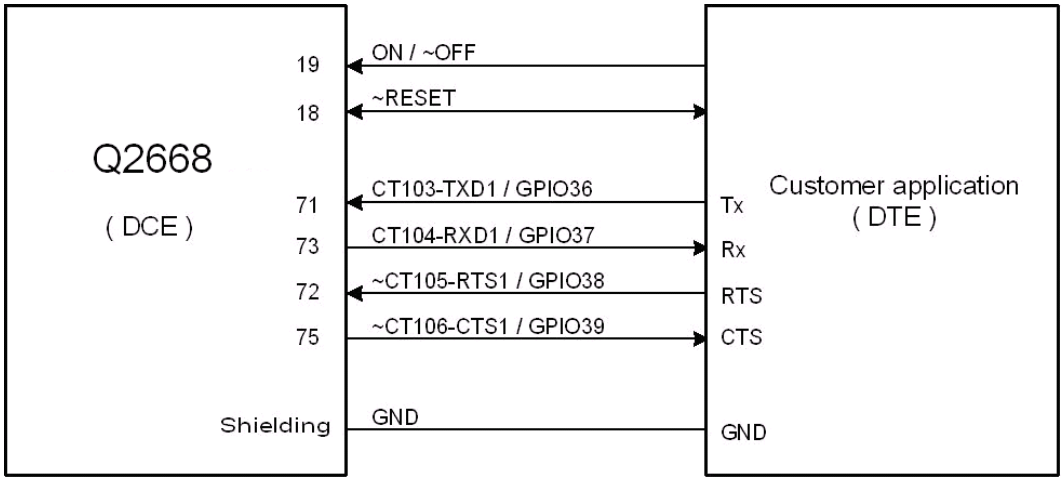


Figure 13. Example of V24/CMOS Serial Link Implementation for UART1

Note that the design presented above is a basic one and that a more flexible design to access the serial link with all modem signals is presented below.

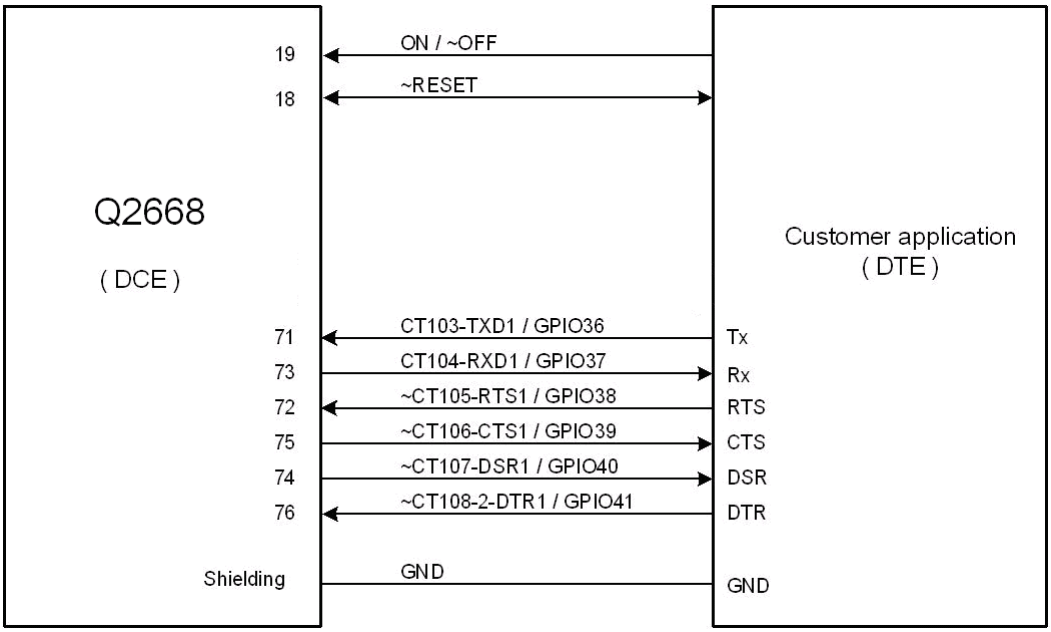


Figure 14. Example of a Full Modem V24/CMOS Serial Link Implementation for UART1

4.6.3.1. 4-wire Serial Interface

The signals used in this interface are as follows:

- CT103-TXD1
- CT104-RXD1
- ~CT105-RTS1
- ~CT106-CTS1

The signal ~CT108-2-DTR1 and ~CT107-DSR1 must be configured from low level. If idle mode is to be used, ~CT107-DTR1 must be configured at high level.

The other signals and their multiplexed GPIOs are not available.

4.6.3.2. 2-wire Serial Interface

Caution: *Although this case is possible for a connected external chip, it is not recommended (and forbidden for AT command or modem use).*

The flow control mechanism has to be managed from the customer side. The signals used in this interface are as follows:

- CT103-TXD1
- CT104-RXD1

Signals ~CT108-2-DTR1, ~CT107-DSR1 and ~CT105-RTS1 must be configured at low level.

If idle mode is to be used, ~CT107-DTR1 must be configured at high level.

The other signals and their multiplexed GPIOs are not available.

Refer to the technical appendixes of document [1] AirPrime Q2668 AT Command Set for more information.

4.7. USIM/SIM Interface

The Universal Subscriber Identification Module (USIM) may be directly connected to the Q2668 via this dedicated interface. The USIM interface controls either 1V8 or 3V USIM.

The four signals used by this interface are as follows:

- SIM-VCC: USIM power supply
- ~SIM-RST: reset
- SIM-CLK: clock
- SIM-IO: I/O port

4.7.1. Pin Description

Refer to the following table for the pin description of the USIM interface.

Table 20. USIM Pin Description

Pin Number	Signal	I/O	I/O Type	Reset State	Description	Multiplexed With
9	SIM-VCC	O	3V / 1V8		USIM Power Supply	Not mux
11	SIM-IO	I/O	3V / 1V8	Pull-up*	USIM Data	Not mux
13	~SIM-RST	O	3V / 1V8	L	USIM Reset	Not mux
14	SIM-CLK	O	3V / 1V8	L	USIM Clock	Not mux

* USIM-IO pull-up is about 10kΩ.

Refer to section 4.2 Electrical Information for Digital I/O for open drain, 2V9 and 1V8 voltage characteristics and reset state definitions.

4.7.2. Electrical Characteristics

Refer to the following table for the electrical characteristics of the USIM interface.

Table 21. Electrical Characteristics of the USIM Interface

Parameter	Conditions	Minimum	Typical	Maximum	Unit
SIM-IO V_{IH}	I_{IH} = ± 20µA	0.7xSIMVCC			V
SIM-IO V_{IL}	I_{IL} = 1mA			0.4	V
~SIM-RST, SIM-CLK V_{OH}	Source current = 20µA	0.9xSIMVCC			V
SIM-IO V_{OH}	Source current = 20µA	0.8xSIMVCC			
~SIM-RST, SIM-IO, SIM-CLK V_{OL}	Sink current = -200µA			0.4	V
SIM-VCC Output Voltage	SIMVCC = 2.9V IVCC= 1mA	2.84	2.9	2.96	V
	SIMVCC = 1.8V IVCC= 1mA	1.74	1.8	1.86	V
SIM-VCC current	VBATT = 3.8V			10	mA

Parameter	Conditions	Minimum	Typical	Maximum	Unit
SIM-CLK Rise/Fall Time	Loaded with 30pF		20		ns
~SIM-RST, Rise/Fall Time	Loaded with 30pF		20		ns
SIM-IO Rise/Fall Time	Loaded with 30pF		0.7	1	µs
SIM-CLK Frequency	Loaded with 30pF			3.25	MHz

4.7.3. SIM Socket Pin Description

The following table lists the SIM socket pin description.

Table 22. SIM Socket Pin Description

Pin Number	Signal	Description
1	VCC	SIM-VCC
2	RST	~SIM-RST
3	CLK	SIM-CLK
5	GND	GROUND
6	VPP	Not connected
7	I/O	SIM-IO with 10KΩ pull-up resistor
8	CC8	Not Connected

4.7.4. Typical Implementation without SIM Detection

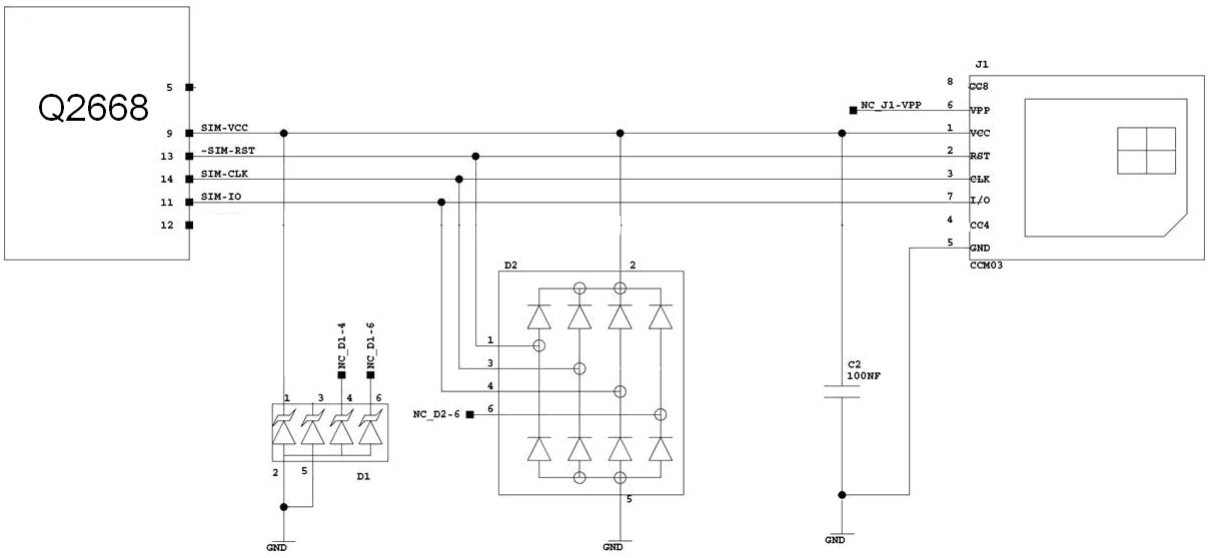


Figure 15. Example of SIM Socket Implementation

4.7.4.1. Recommended Components

- R1 :100 kΩ
- C1 :470 pF
- C2 :100 nF
- D1 :ESDA6V1SC6 from ST
- D2 :DALC208SC6 from SGS-THOMSON
- J1 :ITT CANNON CCM03 series

Note: The capacitor (C2) placed on the SIM-VCC line must not exceed 330nF.

4.8. USB 2.0 Interface

A 4-wire USB slave interface is available which complies with USB 2.0 protocol signaling. But it is not compliant with the electrical interface, due to the 5V interface of VPAD-USB.

The signals used by the USB interface are as follows:

- VPAD-USB
- USB-DP
- USB-DM
- GND

The USB 2.0 interface also features the following:

- 12Mbit/s full-speed transfer rate
- 3.3V type compatible
- USB Softconnect feature
- USB bus error detection and recovery
- Power management: Suspend mode, wake-up from suspend

4.8.1. Pin Description

Refer to the following table for the pin description of the USB interface.

Table 23. USB Pin Description

Pin Number	Signal	I/O	I/O Type	Description
52	VPAD-USB	I	VPAD_USB	USB Power Supply
54	USB-DP	I/O	VPAD_USB	Differential data interface positive
56	USB-DM	I/O	VPAD_USB	Differential data interface negative

4.8.2. Electrical Characteristics

Refer to the following table for the electrical characteristics of the USB interface.

Table 24. Electrical characteristics of the USB Interface

Parameter	Minimum	Typical	Maximum	Unit
VPAD-USB, USB-DP, USB-DM	4.9	5	5.1	V
VPAD-USB Input current consumption		10		mA

4.8.3. Application

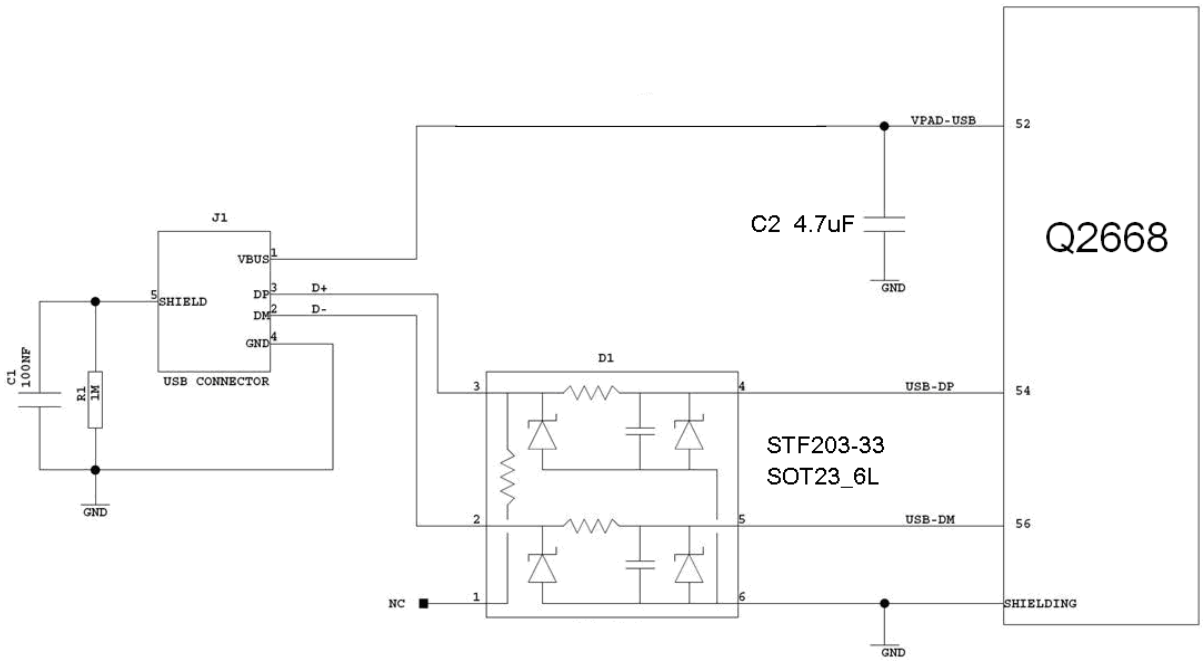


Figure 16. Example of a USB Implementation

D1 is an EMI/RFI filter with ESD protection. The internal pull-up resistor of D1 which is used to detect the interface's full speed is not connected because it is embedded into the Q2668.

R1 and C1 must be close to J1.

4.8.3.1. Recommended Components

- R1 :1MΩ
- C1 :100nF
- C2 :4.7µF
- D1 :STF203-33 from SEMTECH

4.9. RF Interface

The Q2668 supports one antenna. This interface has a nominal impedance of 50Ω and 0Ω DC impedance.

4.9.1. RF Connections

The antenna cable and connector should be selected in order to minimize loss in the frequency bands used for GSM 900MHz, 1800MHz and TD-SCDMA 1880 to 1920, 2010 to 2025 bands.

0.5dB may be considered as the maximum value of loss between the Q2668 and an external connector.

4.9.1.1. U.FL Connector for Main Antenna

A wide variety of cables fitted with U.FL connectors is offered by different suppliers. Refer to section 9.5 Antenna Cable for more information.

4.9.1.2. Soldered Solution for Main Antenna

The soldered solution will preferably be based on an RG178 coaxial cable. Refer to section 9.5 Antenna Cable for more information.

4.9.2. RF Performance

RF performance is compliant with the ETSI GSM 05.05 recommendation.

The main Receiver parameters are:

- E-GSM900 Reference Sensitivity = -108dBm typical (Static & TUHigh)
- DCS1800 Reference Sensitivity = -108 dBm typical (Static & TUHigh)
- 3G Band I 1880~1920 Reference Sensitivity = -110 dBm typical (Static & TUHigh)
- 3G Band II 2010~2025 Reference Sensitivity = -110 dBm typical (Static & TUHigh)
- Selectivity @ 200 kHz: > +9 dBc
- Selectivity @ 400 kHz: > +41 dBc
- Linear dynamic range: 63 dB
- Co-channel rejection: >= 9 dBc

The main Transmitter parameters are:

- TD-SCDMA: Power level 2 (24dBm)
- EGSM900: 33dBm/27dBm (EDGE)
- DCS1800: 30dBm/26dBm (EDGE)

4.9.3. Antenna Specifications

The antenna must meet the requirements specified in the table below.

The optimum operating frequency depends on the application. A dual-band, tri-band or quad-band antenna should operate in these frequency bands and have the following characteristics.

Table 25. Antenna Specifications

Characteristics		E-GSM 900	DCS 1800	TD-SCDMA 1880-1920	TD-SCDMA 2010-2025
TX Frequency		880 to 915 MHz	1710 to 1785 MHz	1880 to 1920 MHz	2010 to 2025 MHz
RX Frequency		925 to 960 MHz	1805 to 1880 MHz		
Impedance		50 Ω			
VSWR	Rx max	1.5:1			
	Tx max	1.5:1			
Max Power		TD-SCDMA: Power level 2 (24 dBm) EGSM900: 33dBm/27dBm (EDGE) DCS1800: 30dBm/26dBm (EDGE)			
Typical radiated gain		0dBi in one direction at least			

4.9.3.1. Application

The antenna should be isolated as much as possible from analog and digital circuitry (including interface signals).

On applications with an embedded antenna, poor shielding could dramatically affect the receiving sensitivity. Moreover, the power radiated by the antenna could affect the application (TDMA noise, for instance).

As a general recommendation, all components or chips operated at high frequencies (microprocessors, memories, DC/DC converter) or other active RF parts should not be placed too close to the Q2668 embedded module. In the event that this happens, the correct power supply layout and shielding should be designed and validated.

Components near RF connections or unshielded feed lines must be prohibited.

RF lines must be kept as short as possible to minimize loss.

4.10. Analog Audio Interface

The Q2668 supports two microphone inputs and two speaker outputs. It also includes an echo cancellation and a noise reduction feature which allows for an improved quality of hands-free functionality.

In some cases, ESD protection must be added on the audio interface lines.

4.10.1. Pin Description

The following table lists the pin description of the analog audio interface.

Table 26. Analog Audio Pin Description

Pin Number	Signal	I/O	I/O Type	Description
34	MIC2N	I	Analog	Microphone 2 negative input
35	SPK1P	O	Analog	Speaker 1 positive output
36	MIC2P	I	Analog	Microphone 2 positive input
37	SPK1N	O	Analog	Speaker 1 negative output
38	MIC1N	I	Analog	Microphone 1 negative input
39	SPK2P	O	Analog	Speaker 2 positive output
40	MIC1P	I	Analog	Microphone 1 positive input
41	SPK2N	O	Analog	Speaker 2 negative output

4.10.2. Microphone Features

The microphone can be connected in either differential or single-ended mode. However, it is strongly recommended to use a differential connection in order to reject common mode noise and TDMA noise. When using a single-ended connection, be sure to have a very good ground plane, very good filtering, as well as shielding in order to avoid any disturbance on the audio path. Also note that using a single-ended connection decreases the audio input signal by 6dB as compared to using a differential connection.

The gain of both MIC inputs are internally adjusted and can be tuned using AT commands. For more information on AT commands, refer to document [1] AirPrime Q2668 AT Command Set.

Refer to the following table for the electrical characteristics of MIC1 and MIC2.

Table 27. Electrical Characteristics of MIC1 & MIC2

Parameters			Minimum	Typical	Maximum	Unit
AC Characteristics 200 Hz < F < 4 kHz	Z1	Differential	140	200	320	kΩ
		Single ended	70	100	160	kΩ
MIC	Sensitivity Range		-43	-40	-37	dB
	Impedance				2,2	kΩ
	Consume				0.5	mA

Caution: *The voltage input value cannot exceed the maximum working voltage; otherwise, clipping will appear.*

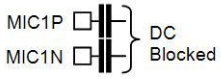
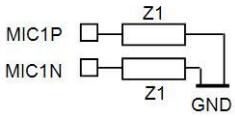
4.10.2.1. MIC1 Microphone Input

By default, the MIC1 input is single-ended, but can be configured in differential mode.

The MIC1 input include an internal bias making it the standard input for an external headset or a hands-free kit.

AC coupling is already embedded in the Q2668.

Table 28. Equivalent Circuits of MIC1

DC Equivalent Circuit	AC Equivalent Circuit
	

4.10.2.2. MIC1 Differential Connection Example

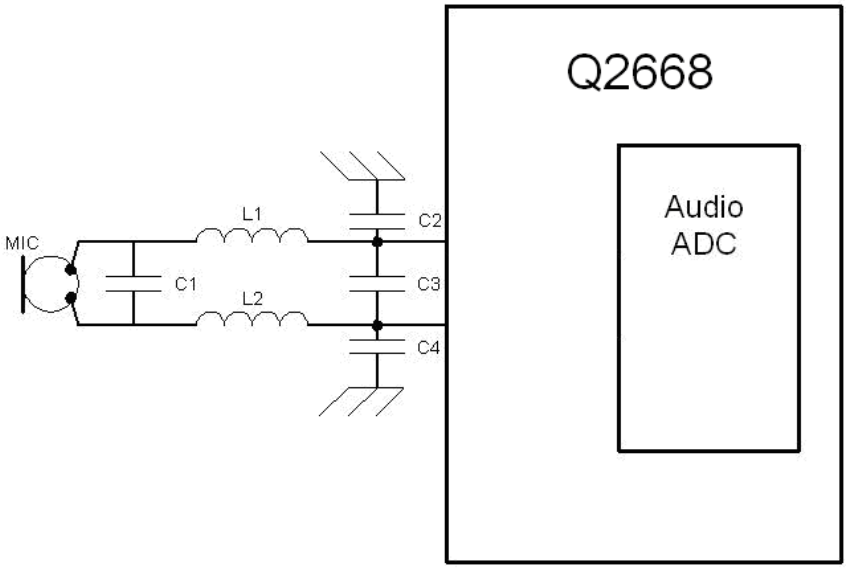


Figure 17. Example of MIC1 Input Differential Connection with LC Filter

Audio quality can be very good without a filter (L1, L2, C2, C3 and C4), depending on the design. But if there is EMI perturbation, this filter can reduce TDMA noise. Note though that this filter is not mandatory. If the filter is not to be used, the capacitors must be removed and the coil replaced by 0Ω resistors as shown in the following diagram.

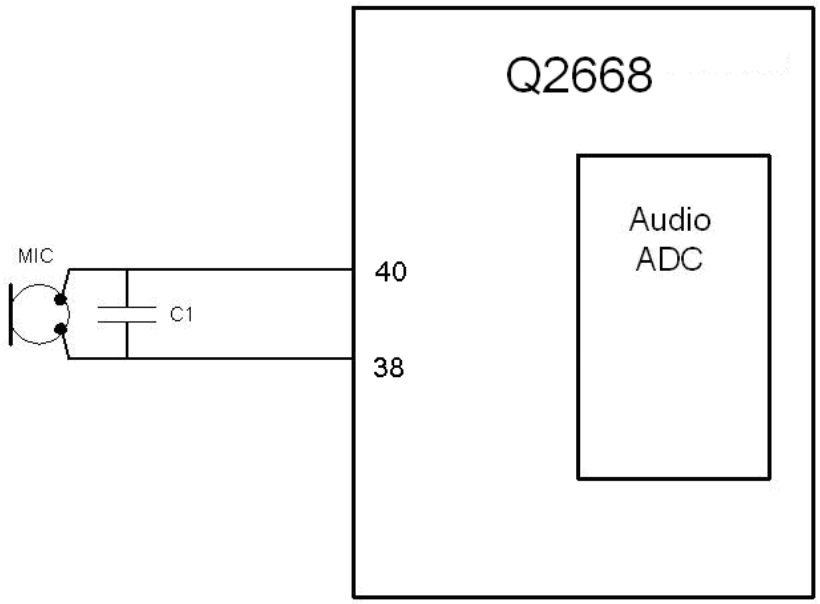


Figure 18. Example of MIC1 Input Differential Connection without LC Filter

The capacitor, C1, is highly recommended to eliminate TDMA noise and it must be connected close to the microphone.

The following table lists the recommended components to use in creating the LC filter.

Table 29. Recommended Components for MIC1 Input Differential Connection

Component	Value	Notes
C1	12pF to 33pF	Must be tuned depending on the design.

4.10.2.3. MIC1 Single-Ended Connection Example

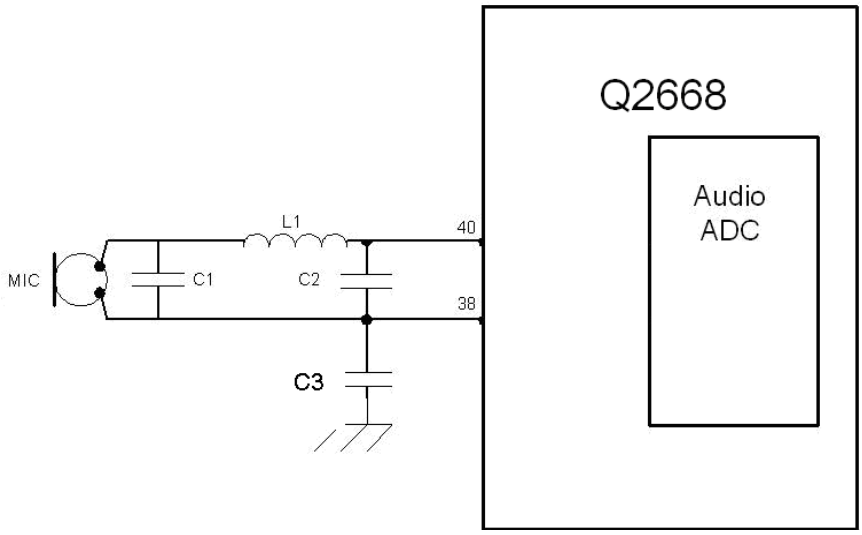


Figure 19. Example of MIC1 Input Single-Ended Connection with LC Filter

The single-ended design is not recommended for improving TDMA noise rejection as it is usually difficult to eliminate TDMA noise from a single-ended design.

It is recommended to use an LC filter (L1 and C2) to eliminate TDMA noise. Note though that this filter is not mandatory. If the filter is not to be used, the capacitor C2 must be removed and the coil replaced by 0Ω resistors as shown in the following diagram.

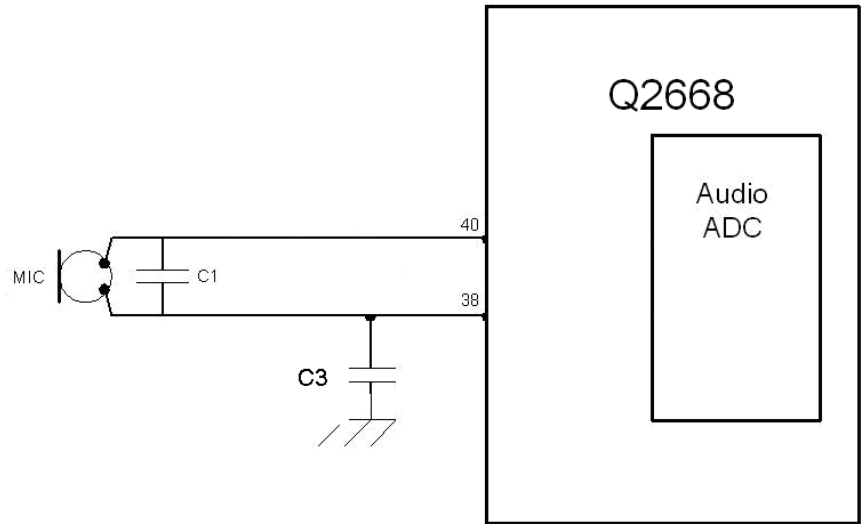


Figure 20. Example of MIC1 Input Single-Ended Connection without LC Filter

The capacitor, C1, is highly recommended to eliminate TDMA noise and it must be connected close to the microphone.

The following table lists the recommended components to use in creating the LC filter.

Table 30. Recommended Components for a MIC1 Input Single-Ended Connection

Component	Value	Notes
C1	12pF to 33pF	Must be tuned depending on the design.
C2		Must be tuned depending on the design.
C3	100nF	
L1		Must be tuned depending on the design.

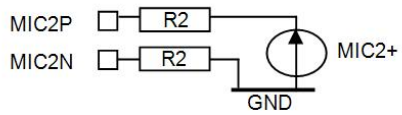
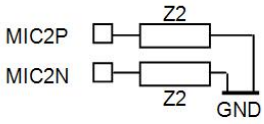
4.10.2.4. MIC2 Microphone Input

By default, the MIC2 input is differential, but can be configured in single-ended mode.

The MIC2 input already includes biasing for an electret microphone and the electret microphone may be directly connected to this input, allowing an easy connection to a headset/handset.

AC coupling is already embedded in the Q2668.

Table 31. Equivalent Circuits of MIC2

DC Equivalent Circuit	AC Equivalent Circuit
	

4.10.2.5. MIC2 Differential Connection Example

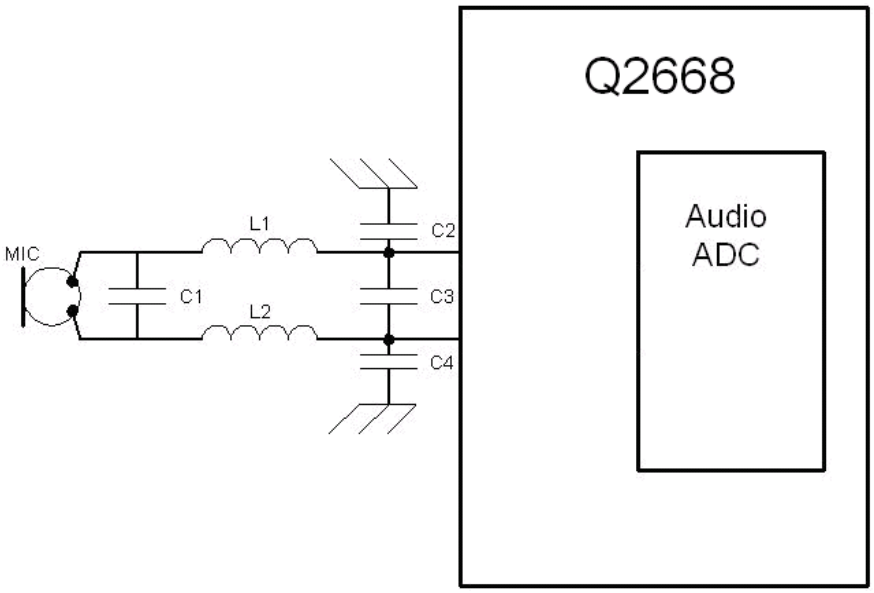


Figure 21. Example of MIC2 Input Differential Connection with LC Filter

Audio quality can be very good without a filter (L1, L2, C2, C3 and C4), depending on the design. But if there is EMI perturbation, this filter can reduce TDMA noise. Note though that this filter is not mandatory. If the filter is not to be used, the capacitors must be removed and the coil replaced by 0Ω resistors as shown in the following diagram.

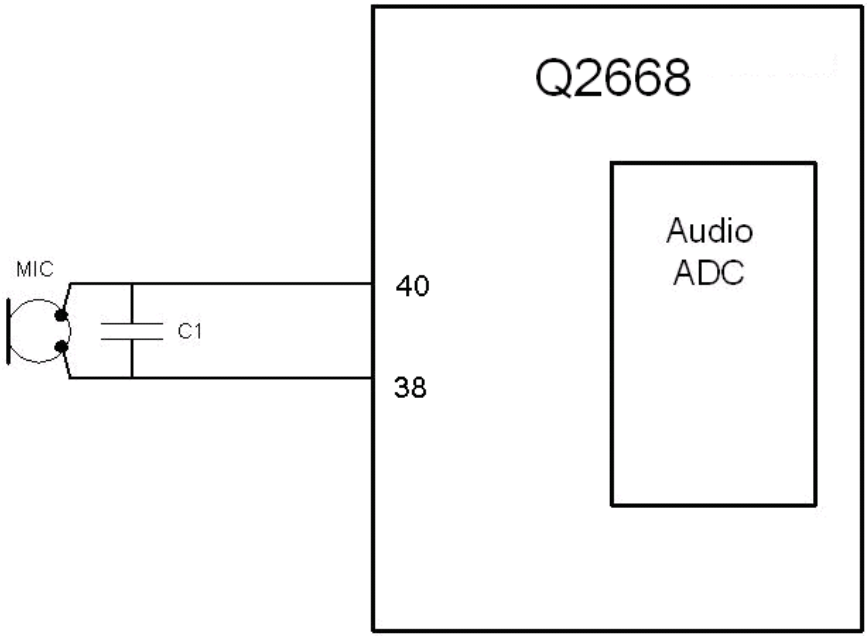


Figure 22. Example of MIC2 Input Differential Connection without LC Filter

The capacitor, C1, is highly recommended to eliminate TDMA noise and it must be connected close to the microphone.

The following table lists the recommended components to use in creating the LC filter.

Table 32. Recommended Components for a MIC2 Differential Connection

Component	Value	Notes
C1	12pF to 33pF	Must be tuned depending on the design.

4.10.2.6. MIC2 Single-Ended Connection Example

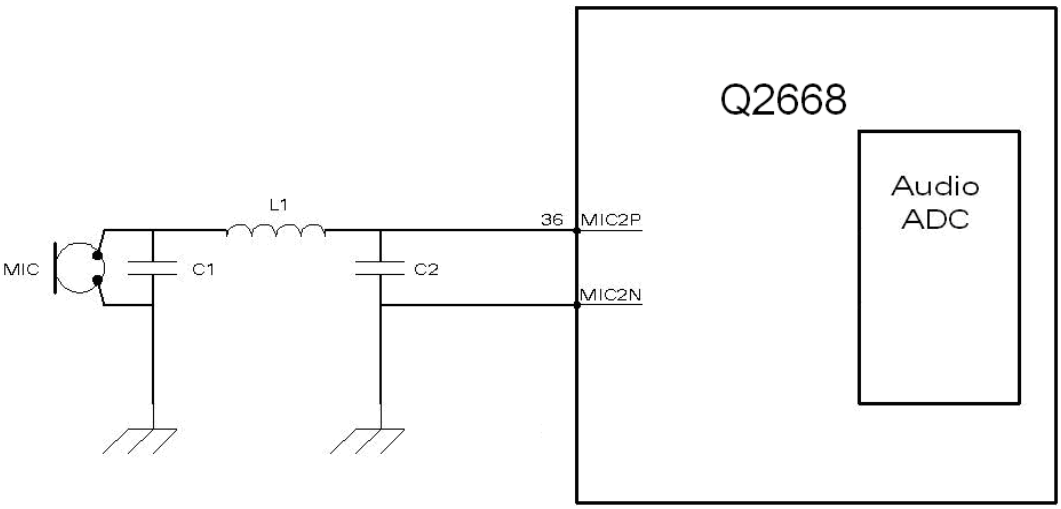


Figure 23. Example of MIC2 Input Single-Ended Connection with LC Filter

The single-ended design is not recommended for improving TDMA noise rejection as it is usually difficult to eliminate TDMA noise from a single-ended design.

It is recommended to use an LC filter (L1 and C2) to eliminate TDMA noise. Note though that this filter is not mandatory. If the filter is not to be used, the capacitor C2 must be removed and the coil replaced by 0Ω resistors as shown in the following diagram.

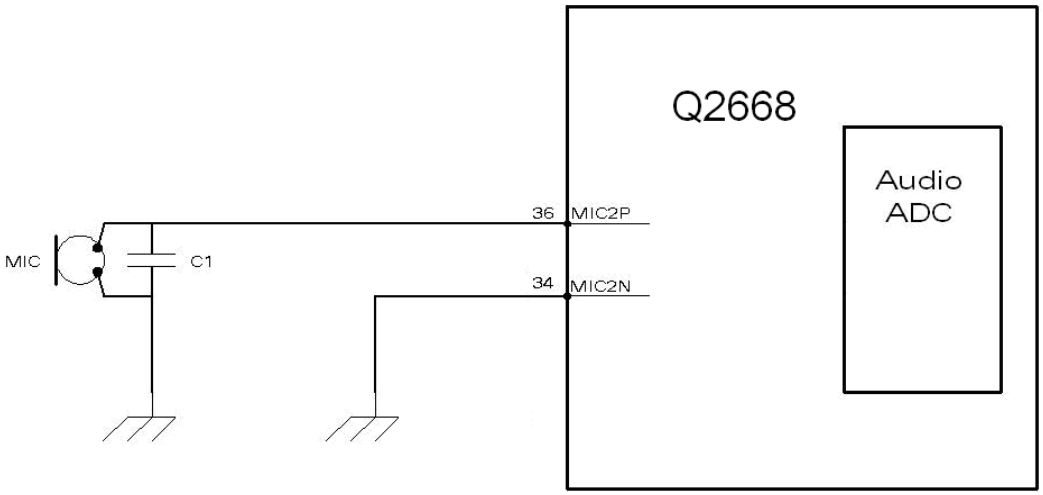


Figure 24. Example of MIC2 Input Single-Ended Connection without LC Filter

The capacitor, C1, is highly recommended to eliminate TDMA noise and it must be connected close to the microphone.

The following table lists the recommended components to use in creating the LC filter.

Table 33. Recommended Components for a MIC2 Single-Ended Connection

Component	Value	Notes
C1	12pF to 33pF	Must be tuned depending on the design.
C2		Must be tuned depending on the design.
L1		Must be tuned depending on the design.

4.10.3. Speaker Features

There are two different speaker channels, SPK1 and SPK2, available on the Q2668. The connection on SPK1 is fixed as single-ended, but SPK2 may be configured in either differential or single-ended mode.

However, as with the microphone connection, it is strongly recommended to use a differential connection in order to reject common mode noise and TDMA noise. Furthermore, using a single-ended connection entails losing power (the power is divided by 4 in a single-ended connection) as compared to using a differential connection.

Note that when using a single-ended connection, a very good ground plane, very good filtering, as well as shielding is needed in order to avoid any disturbance on the audio path.

The gain of each speaker output channel is internally adjusted and can be tuned using AT commands. For more information on AT commands, refer to document [1] AirPrime Q2668 AT Command Set.

No discreet components like resistors or capacitors are needed when using this interface.

The following table lists the typical values of both speaker outputs.

Table 34. Speaker Information

Parameter	Typical	Unit	Connection
Z (SPK1P, SPK1N)	16 or 32	Ω	Single-ended mode

Parameter	Typical	Unit	Connection
Z (SPK2P, SPK2N)	4	Ω	Single-ended mode
Z (SPK2P, SPK2N)	8	Ω	Differential mode

4.10.3.1. Speakers Output Power

The maximum power output of SPK1 and SPK2 are not similar because of the difference in their configuration. Because SPK2 can be connected in differential mode, it can provide more power compared to SPK1 which only allows single-ended connections. The maximal specifications given in the following sub-sections are available with the maximum power output configuration values set by AT command, and the typical values are recommended.

4.10.3.2. SPK1 Speaker Outputs

SPK1 only allows for a single-ended connection.

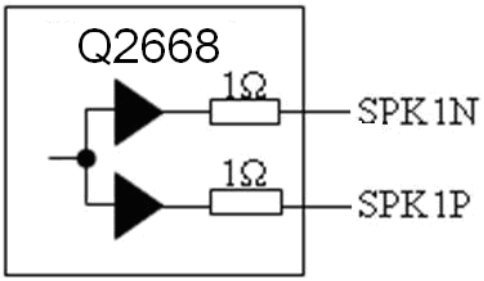


Figure 25. Equivalent Circuits of SPK1

Refer to the following table for the electrical characteristics of SPK1.

Table 35. Electrical Characteristics of SPK1

Parameters			Minimum	Typical	Maximum	Unit
Biasing voltage	-		2.5	2.5	2.75	V
Output swing voltage	RL=16Ω: AT+VGR=-1600**; single-ended		1.8	2.0	-	Vpp
	RL=32Ω; AT+VGR=-1600**; single-ended		2.0	2.2		Vpp
RL	Load resistance		14.5	32	-	Ω
IOUT	Output current; single-ended; peak value	RL=16Ω	40	44	85	mA
		RL=32Ω	22	24	-	mA
POUT	RL=16Ω; AT+VGR*=-1600**		25	31		mW
	RL=32Ω; AT+VGR*=-1600**		16	19	27	mW
RPD	Output pull-down resistance at power-down		28	40	52	kΩ

* The output voltage depends on the output speaker gain set by AT command.

** This value is given in dB, but it's possible to toggle to index value.

4.10.3.3. SPK2 Speaker Outputs

SPK2 can have either a single-ended or a differential connection.

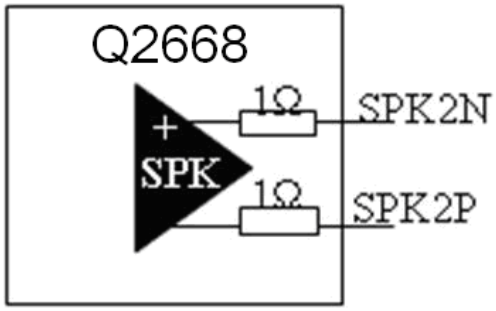


Figure 26. Equivalent Circuits of SPK2

Refer to the following table for the electrical characteristics of SPK2.

Table 36. Electrical Characteristics of SPK2

Parameters		Minimum	Typical	Maximum	Unit
Biasing voltage	SPK2P and SPK2N	2.5	2.5	2.75	V
RL	Load resistance	6	8	-	Ω
IOUT	Output current; peak value; RL=8Ω	-	-	275	mA
POUT	RL=8Ω; AT+VGR=-1000*;	-	-	300	mW
RPD	Output pull-down resistance at power-down	28	40	52	kΩ
VPD	Output DC voltage at power-down	-	100	-	mV

* The output voltage depends on the output speaker gain set by AT command. Refer to document [1] AirPrime Q2668 AT Command Set for more information.

If a single-ended connection is used with SPK2, only one of either SPK2 has to be chosen. The result is a maximal output power divided by 4.

4.10.3.4. Differential Connection Example

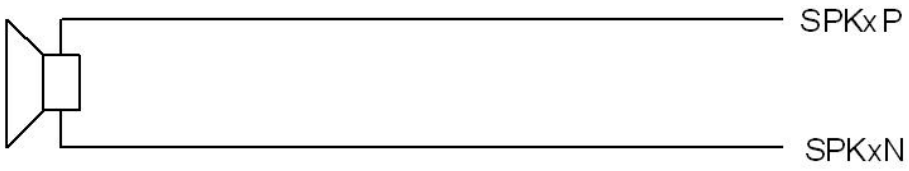


Figure 27. Example of Speaker Differential Connection

Impedance of the speaker amplifier output in differential mode is **R ≤ 1Ω +/-10 %**.

Note that the connection between the speaker and the Q2668 pins must be designed to keep the serial impedance lower than 3Ω when it is connected in differential mode.

4.10.3.5. Single-Ended Connection Example

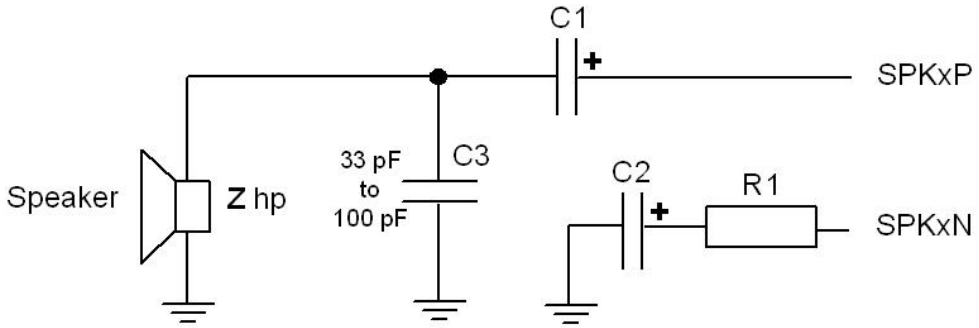


Figure 28. Example of Speaker Single-Ended Connection

Take note of the following when connecting the speaker in single-ended mode:

- 6.8μF < C1 < 47μF (depending on the characteristics of the speaker and the output power)
- C1 = C2
- R1 = Zhp
- Using a single-ended connection results in output power loss (-6dB) as compared to a differential connection

In the case of a 32Ω speaker, a cheaper and smaller solution can be implemented where R1 = 82Ω and C2 = 6.8μF (ceramic).

Note that the connection between the speaker and the Q2668 pins must be designed to keep the serial impedance lower than 1.5Ω when it is connected in single-ended mode.

Lastly, when the SPK1 channel is used, only SPK1P is useful in a single-ended connection and SPK1N can be left open.

4.10.3.6. Recommended Characteristics

- Type : 10mW, electro-magnetic.
- Impedance
  - Z = 8Ω for hands-free (SPK2)
  - Z = 32Ω for headset kit (SPK1)
- Sensitivity :110 dB SPL minimum (0 dB = 20μPa)
- Frequency response compatible with GSM specifications

4.11. Digital Audio Interface (PCM)

The Digital Audio Interface (PCM) interface allows connectivity with standard audio peripherals. It can be used, for example, to connect an external audio codec.

The programmability of this interface allows addressing a large range of audio peripherals.

The signals used by the Digital Audio Interface are as follows:

- **PCM-SYNC (output)**: The frame synchronization signal delivers an 8 kHz frequency pulse that synchronizes the frame data in and the frame data out.
- **PCM-CLK (output)**: The frame bit clock signal controls data transfer with the audio peripheral.
- **PCM-OUT (output)**: The frame “data out” relies on the selected configuration mode.
- **PCM-IN (input)**: The frame “data in” relies on the selected configuration mode.

The Digital Audio Interface also features the following:

- IOM-2 compatible device on physical level
- 16 bits data word MSB first only
- Linear Law only (no compression law)
- Push-pull configuration on PCM-OUT and PCM-IN

The digital audio interface configuration cannot differ from those specified above.

4.11.1. PCM Waveforms

The following figures describe the PCM Frame and Sampling waveforms.

The default configuration: The PCM data slot is the first slot and short Frame.

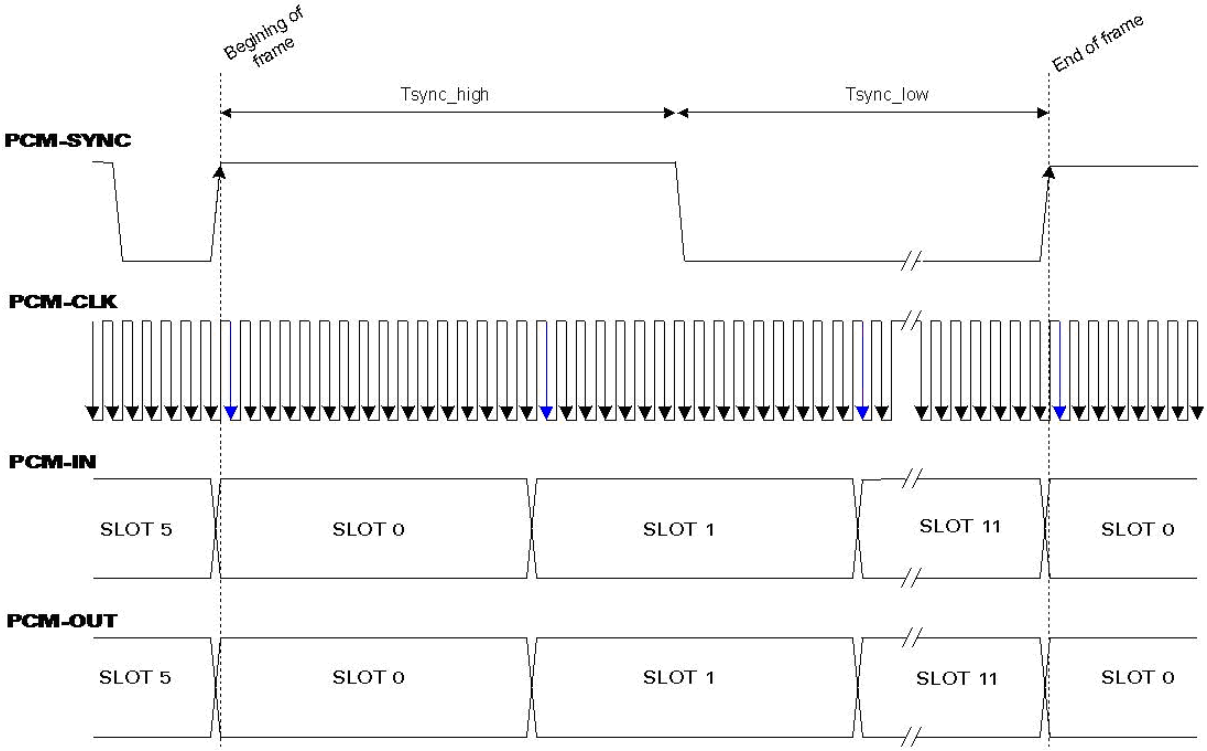


Figure 29. PCM Frame Waveform

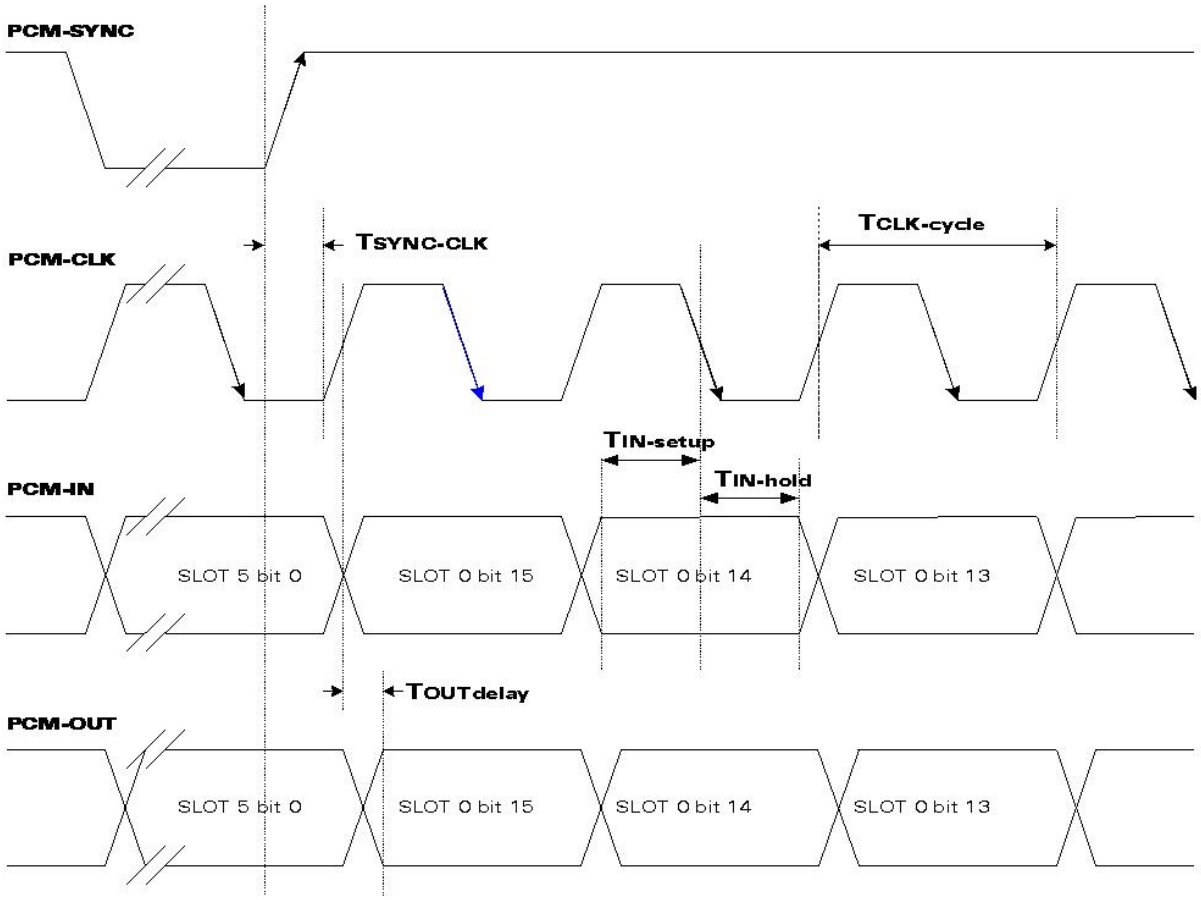


Figure 30. PCM Sampling Waveform

Refer to the following table for the AC characteristics of the digital audio interface.

Table 37. AC Characteristics of the Digital Audio Interface

Signal	Description	Minimum	Typical	Maximum	Unit
T_{sync_high}	PCM-SYNC high time	25			µs
$T_{SYNC-CLK}$	PCM-SYNC to PCM-CLK time	-	125	-	ns
$T_{CLK-cycle}$	PCM-CLK period	200		7800	ns
$T_{IN-setup}$	PCM-IN setup time	70			ns
$T_{IN-hold}$	PCM-IN hold time	40			ns
$T_{OUT-delay}$	PCM-OUT delay time			30	ns

4.11.2. Pin Description

Refer to the following table for the pin description of the digital audio (PCM) interface.

Table 38. Pin description of the PCM interface

Pin Number	Signal	I/O	I/O type	Reset state	Description
77	PCM-SYNC	O	1V8	L weak	Frame synchronization 8kHz
78	PCM-IN	I	1V8	H weak	Data input

Pin Number	Signal	I/O	I/O type	Reset state	Description
79	PCM-CLK	O	1V8	L weak	Data clock
80	PCM-OUT	O	1V8	H weak	Data output

Refer to section 4.2 Electrical Information for Digital I/O for open drain, 2V9 and 1V8 voltage characteristics and reset state definitions.

4.12. Battery Charging Interface

The Q2668 supports one battery charging circuit, two algorithms and one hardware charging mode (pre-charging) for the following battery types:

- Ni-Mh (Nickel-Metal Hydride) with algorithm 0
- Li-Ion (Lithium-Ion) with the embedded PCM (Protection Circuit Module) algorithm 1

The Q2668 charging circuit is composed of a transistor switch (between CHG-IN pin 6, 8 and VBATT pin 1, 2, 3, 4). Charging is controlled by 2 software algorithms.

The two algorithms control a switch, which connects the CHG-IN signal to the VBATT signal. The algorithm controls the frequency and the connected time of the switching. During the charging procedure, battery charging level is monitored and when Li-Ion (algorithm 0) is used, the battery temperature is monitored via the ADC1/BAT-TEMP input.

Note: If the Q2668 is not powered (VBATT pin 1, 2, 3, 4) by a rechargeable battery, it is mandatory to leave the CHG-IN input (pin 6, 8) open.

A dedicated ADC input, BAT-TEMP (pin 20), is available for temperature monitoring (only for Li-Ion battery technology).

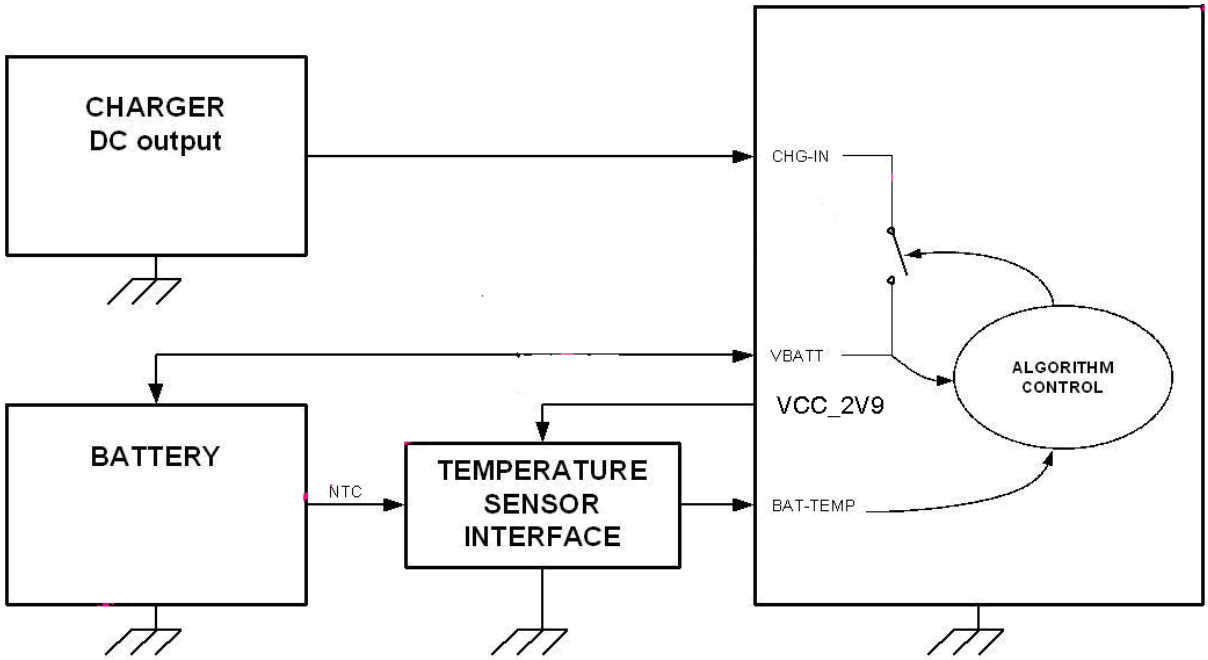


Figure 31. Synopsis of Battery Charging

One more charging procedure is provided by the Q2668. This is called “Pre-charging” mode. This is a special charging mode because it is activated only when the Q2668 is OFF. The purpose of this charging mode is to avoid battery damage by preventing the battery from being discharged to below the minimum battery level. Control of this mode is managed by hardware.

To use the charging functionality, 3 hardware items are required:

- Charger power supply – this provides a DC current power supply limited to 800mA and with voltage range, according to the battery choice and to the Q2668 specification.
- Battery – the charging functionality must only be used with rechargeable batteries. Two battery types are supported: Li-Ion, Ni-Mh.
- Analog temperature sensor – this is only used for Li-Ion batteries to monitor the battery temperature. This sensor is composed of an NTC sensor and several resistors.

4.12.1. Charger Recommendations

The following table defines and specifies the AC/DC adapter for a battery cell.

Table 39. Charger Recommendations

Parameter	Minimum	Typical	Maximum	Unit	Remark
Input voltage	90		265	Vac	
Input frequency	45		65	Hz	
Output voltage limit			5.5	V	No load
Output voltage limit	4.6			V	Io max
Output current		300		mA	
Output Voltage Ripple			150	mVpp	

We recommend that the output voltage (Vo) fall under 1.18V in less than 1 second when the adapter AC/DC is unplugged.

4.12.2. Charging Algorithms

The Sierra Wireless Software Suite provides the charging algorithms for Li-ion and Ni-Mh type batteries.

Algorithm 0 is used for Ni-Mh type batteries, while algorithm 1 is used for Li-Ion type batteries. Temperature monitoring is only performed when using algorithm 1.

Both charging algorithms are controlled by AT commands. Refer to document [1] AirPrime Q2668 AT Command Set for more information about AT commands.

Note: In the following sub-sections, the parameters in bold and italic type can be modified with AT commands.

4.12.2.1. Ni-Mh Charging Algorithm

This algorithm measures the battery voltage when the DC switch is open (T2). If the voltage is below ***BattLevelMax***, the switch is closed (T1) to charge the battery. The switch is then re-opened for a time specified by ***TPulseInCharge*** (typically 100ms) and then the switch is closed again.

When the battery voltage has reached ***BattLevelMax***, the software monitors the battery voltage (typically every 5seconds; defined by ***TPulseOutCharge***) and the switch state is left open for time T3.

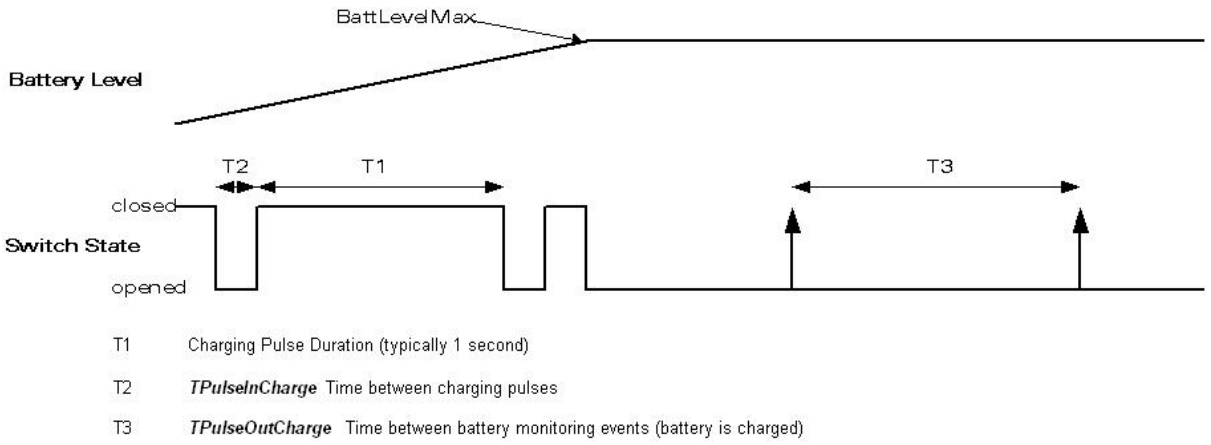


Figure 32. Ni-Mh Charging Waveform

Refer to the following table for the electrical characteristics of the Ni-Cd battery timing charge.

Table 40. Electrical Characteristics of Ni-Mh Battery Timing Charge

Parameter	Minimum	Typical	Maximum	Unit
T1		1		s
T2		0.1		s
T3		5		s

T1, T2, T3 and ***BattLevelMax*** may be configured using AT commands. For more information, refer to document [1] AirPrime Q2668 AT Command Set.

Note: Only the battery level, and not the temperature, is monitored by the software.

4.12.2.2. Li-Ion Charging Algorithm

The Li-Ion charger algorithm can be broken down into three phases:

1. Pre-charging
2. Constant current charging
3. Constant voltage charging

The three phases can be seen on the following waveform for full charging:

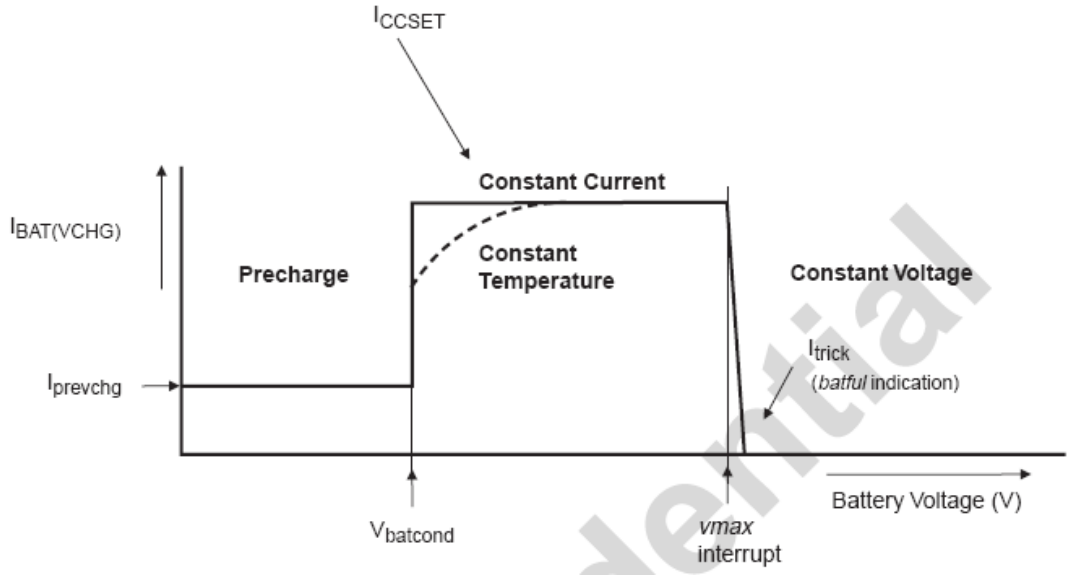


Figure 33. Li-Ion Full Charging Waveform

4.12.3. Pre-Charging

When a charger DC power supply is connected to the CHG-IN input and if the voltage battery is between 2.8V* and 3.2V, a constant current of 50mA is provided to the battery.

When the battery is able to supply the Q2668, it is automatically powered on and the software algorithm is activated to finish the charge.

* For the Lithium-ion battery, the minimum voltage must be higher than the PCM lock level.

Note:	*When pre-charging is launched, the LED0 output blinks automatically.*

Caution:	*The Q2668 can not release the PCM protection inside the Lithium battery pack. Voltage is forbidden on the CHG-IN signal if no battery is connected on the VBATT signals.*

4.12.4. Temperature Monitoring

Temperature monitoring is only available for the Li-Ion battery with algorithm 1. The ADC1/BAT-TEMP (pin 20) input must be used to sample the temperature analog signal provided by an NTC temperature sensor. The minimum and maximum temperature range may be set by AT command.

Table 41. Pin Description of Battery Charging Interface

Signal	Pin Number	I/O	I/O Type	Description
6, 8	CHG-IN	I	Analog	Current source input
20	BAT-TEMP	I	Analog	A/D converter

Table 42. Electrical Characteristics of Battery Charging Interface

Parameter		Minimum	Typical	Maximum	Unit
Charging operating temperature		0		50	°C
ADC1/BAT-TEMP (pin 20)	Maximum output code		1635		LSB
	Sampling rate frequency		216	7000	Hz

Parameter		Minimum	Typical	Maximum	Unit
	Input Impedance (R)		1		MΩ
	Input signal range	0		2	V
CHG-IN (pin 6, 8)	Voltage (for I=Imax)	4.8*			V
	Voltage (for I=0)			5.5	V
	DC Current	400**		800	mA

* To be configured as specified by the battery manufacturer.

** This value has to be selected in function of the power consumption mode used; please refer to the power consumption tables in section 6 Power Consumption.

4.12.5. Application

The VCC_2V9 (pin 10) voltage provided by the Q2668 may be used to polarize the NTC. However, the additional resistors R1 and R2 must be used to adjust the maximum voltage of the ADC input to 2volts.

If any other polarized voltage is used, the resistors must be adapted.

It is not recommended to used the VCC_1V8 (pin 5) voltage.

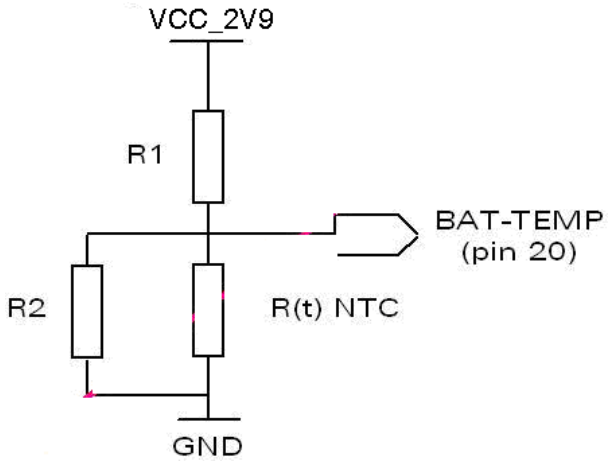


Figure 34. Example of ADC Application

The R(t) resistor is the NTC and must be close to the battery. Usually, it is integrated into the battery.

Note the following:

- The Charger DC power supply must have an output current limited to 800mA.
- The maximum Charger output current, provided to the battery, must be according to the battery electrical characteristics.
- Li-Ion batteries must be used with the embedded PCM (Protection Circuit Module).
- The maximum charging voltage is up to 4.3V (software drive).
- At the first plug, if the Li-ion battery is locked by its PCM, the charger function does not work.

5. Signals and Indicators

5.1. ON/~OFF Signal

This input is used to switch the Q2668 ON or OFF.

A Low-level signal must be provided on the ON/~OFF pin to switch ON the Q2668. The voltage of this signal has to be maintained lower than 0.2 x VBATT during 100ms (min80~max120ms).

The Q2668 module can be switched off by either software or hardware. When the module is ON, a Low-level signal provided on the ON/~OFF pin for a duration of more than 1s will switch the module OFF.

Table 43. ON/~OFF Signal Pin Description

Pin Number	Signal	I/O	I/O Type	Description
19	ON/~OFF	I	CMOS	Q2668 Power-ON

Table 44. Electrical Characteristics of the ON/~OFF Signal

Parameter		I/O Type	Minimum	Maximum	Unit
V_{IL}		CMOS	0	VBATT x 0.2	V
V_{IH}	VBATT	CMOS	VBATT x 0.7	VBATT	V
	CHG-IN/ Charging	CMOS	CHG-IN x 0.7	CHG-IN	V

Caution: *All external signals must be inactive when the Q2668 is OFF to avoid any damage when starting and to allow the Q2668 to start and stop correctly.*

5.1.1. Power-ON

Once the Q2668 is supplied through VBATT, the application must set the ON/OFF signal to low to start the Q2668 power-ON sequence. The ON/OFF signal must be held low for a delay of $\mathbf{T_{on/off\text{-}hold}}$ (hold delay on the ON/~OFF signal) to power-ON. After this delay, an internal mechanism maintains the Q2668 in power-ON condition.

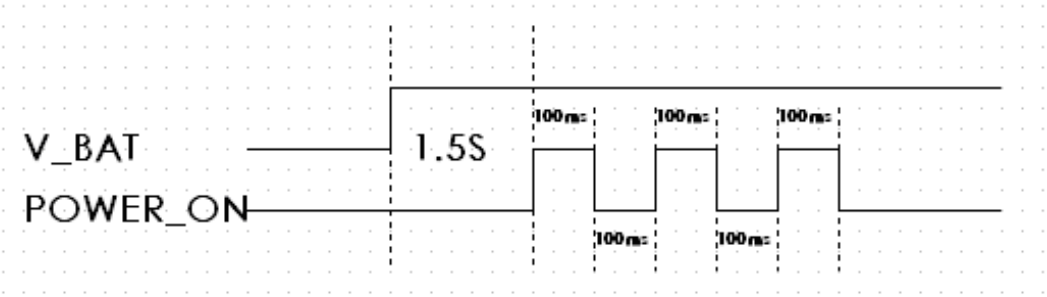


Figure 35. Power-ON Sequence (no PIN code activated)

The duration of the firmware power-up sequence depends on:

- the need to perform a recovery sequence if the power has been lost during a flash memory modification.

Other factors that have a minor influence include:

- the number of parameters stored in EEPROM by the AT commands received so far
- the ageing of the hardware components, especially the flash memory
- the temperature conditions

The table below gives the minimum values of $\mathbf{T_{on/off\text{-}hold}}$:

Table 45. $T_{on/off\text{-}hold}$ Minimum Values

$T_{on/off}$ (ms)	Minimum	Typical	Maximum
T_{on}	80	100	120
T_{off}	1000	1500	-

The figures above take the worst cases into account: power-loss recovery operations, slow flash memory operations in high temperature conditions, and so on. But, they are safe because they are large enough to ensure that ON/~OFF is not de-asserted too early.

The ON/~OFF signal can be left at high level until switched OFF. But this is not recommended as it will prevent the **AT+PSCPOF** command from performing a clean power-off. (Refer to the Note on Power-OFF for an alternate usage.)

When using a battery as power source, it is not recommended to let VBATT ON after switching off the Q2668.

5.1.2. Power-OFF

To power-OFF the Q2668 correctly, the application sends the **AT+PSCPOF** command to switch off the Q2668.

Once the "OK" response is issued by the Q2668, the power supply can be switched off.

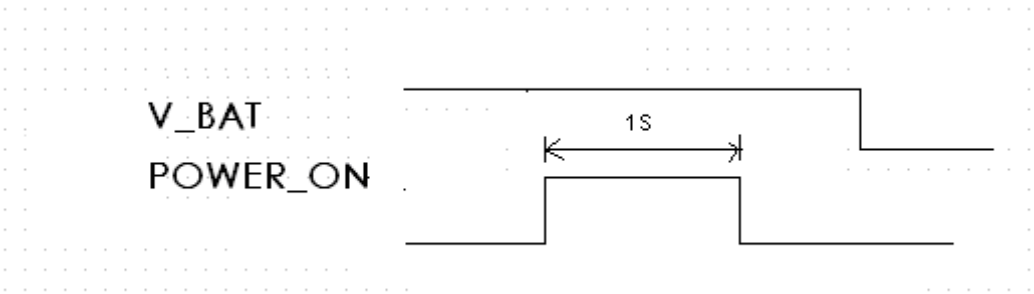


Figure 36. Power-OFF Sequence

Note: If the ON/~OFF pin is maintained to ON (High Level), then the Q2668 can't be switched OFF.

Connecting a charger on the Q2668 has exactly the same effect as setting the ON/~OFF signal. In particular, the Q2668 will not POWER-OFF after the **AT+PSCPOF** command, unless the Charger is disconnected.

5.1.3. Application

The ON/~OFF input (pin 19) is used to switch ON or OFF the Q2668 embedded module.

A high level signal has to be provided on the ON/~OFF pin to switch the embedded module ON.

The level of the voltage of this signal has to be maintained at 0.8 x VBATT for a minimum of 2000ms.

This signal can be left at HIGH level until switched OFF.

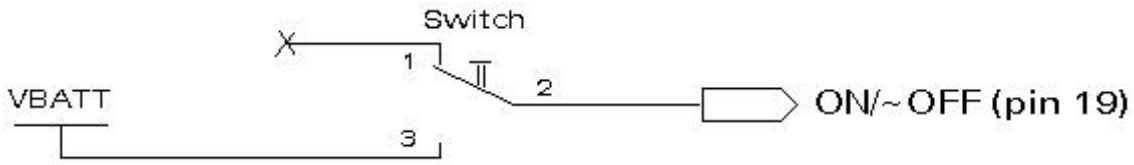


Figure 37. Example of ON/~OFF Pin Connection

5.2. Reset Signal (~RESET)

This signal is used to force a reset procedure by providing the embedded module with a low level for at least 200µs. This signal must be considered as an emergency reset only. A reset procedure is already driven by the internal hardware during the power-up sequence.

This signal may also be used to provide a reset to an external device (at power-up only). If no external reset is necessary, this input may be left open. If used (emergency reset), it must be driven by an open collector or an open drain.

The Q2668 remains in reset mode as long as the ~RESET signal is held low.

Caution: *This signal should only be used for "emergency" resets.*

An operating system reset is preferred to a hardware reset.

5.2.1. Reset Sequence

To activate the "emergency" reset sequence, the ~RESET signal must be set to low for a minimum of 200µs.

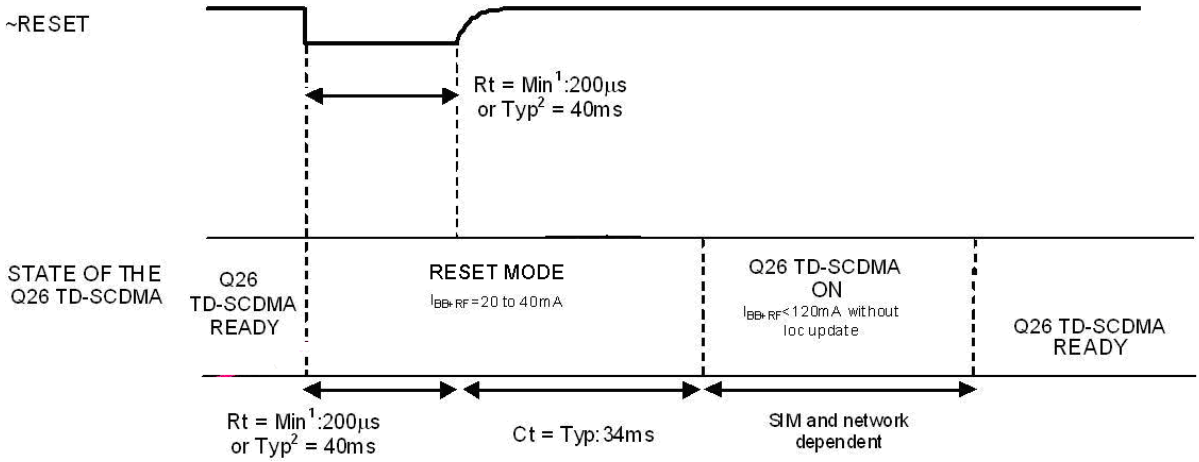


Figure 38. Reset Sequence Waveform

At power-up, the ~RESET time (Rt) is carried out after switching ON the Q2668. It is generated by the internal Q2668 voltage supervisor.

The ~RESET time is provided by the internal RC component. To keep the same time, it is not recommended to connect another R or C component on the ~RESET signal. Only a switch or an open drain gate is recommended.

Ct is the cancellation time required for the Q2668 initialization. Ct is automatically carried out by the Q2668 after a hardware reset.

5.2.2. Pin Description

Refer to the following table for the pin description of the reset signal.

Table 46. Reset Signal Pin Description

Pin Number	Signal	I/O	I/O Type	Description
18	~RESET	I/O Open Drain	1V8	Q2668 Reset

Refer to section 4.2 Electrical Information for Digital I/O for open drain, 2V9 and 1V8 voltage characteristics and reset state definitions.

5.2.3. Electrical Characteristics

Refer to the following table for the electrical characteristics of the reset signal.

Table 47. Electrical Characteristics of the Reset Signal

Parameter	Minimum	Typical	Maximum	Unit
V_{IL}	0	0	0.1	V
V_{IH}	-	1.8	-	V

5.2.4. Application

The ~RESET input (pin 18) is used to force a reset procedure by providing a LOW level for at least 200µs.

This signal has to be considered as an emergency reset only: a reset procedure is automatically driven by an internal hardware during the power-ON sequence.

Table 48. Reset Command

Reset command	~RESET (pin 18)	Operating mode
1	0	Reset activated
0	1	Reset inactive

5.3. BAT-RTC (Backup Battery)

The Q2668 provides an input/output to connect a Real Time Clock (RTC) power supply.

5.3.1. Interface Description

This pin is used as a back-up power supply for the internal Real Time Clock. The RTC is supported by the Q2668 when VBATT is available, but a back-up power supply is needed to save date and time when VBATT is switched off (VBATT = 0V).

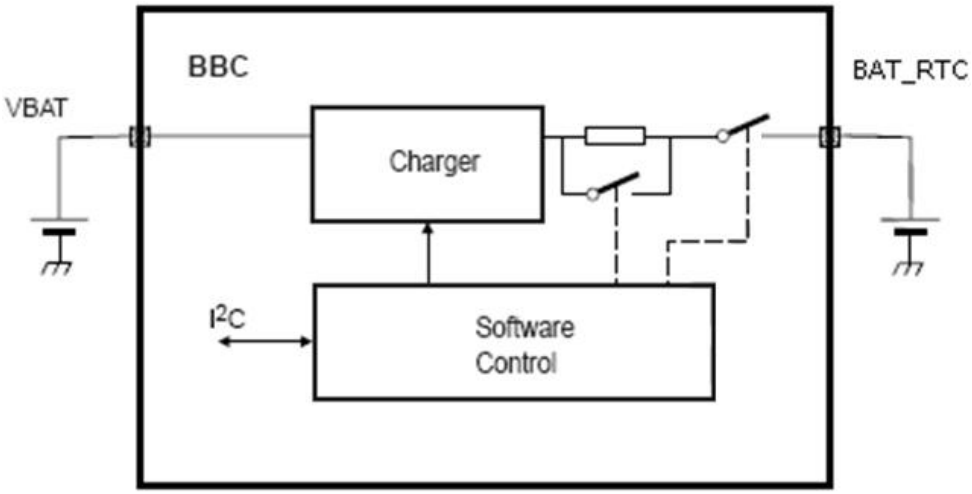


Figure 39. Real Time Clock Power Supply

If the RTC is not used, this pin can be left open.

If VBATT is available, the back-up battery can be charged by the internal 2.5V power supply regulator.

Table 49. Pin Description

Pin Number	Signal	I/O	I/O Type	Description
7	BAT-RTC	I/O	Supply	RTC Back-up supply

Table 50. Electrical Characteristics of the Signals

Parameter	Minimum	Typical	Maximum	Unit
Input voltage	2.37		2.63	V
Input current consumption*		2.5		µA
Input current consumption**			1	µA

* Provided by an RTC back-up battery when the Q2668 power supply is off (VBATT = 0V).

** When a valid BAT power is connected to the Q2668.

5.3.2. Typical Application Electrical Diagram

5.3.2.1. Super Capacitor

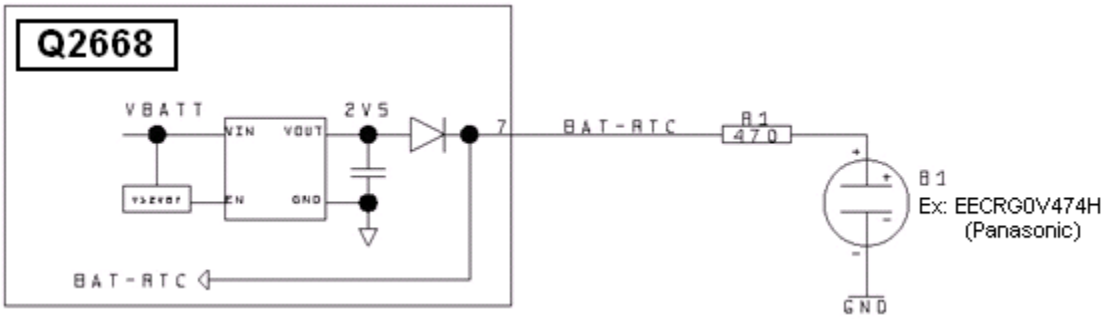


Figure 40. RTC Supplied by a Gold Capacitor

The estimated range with a 0.47 Farad gold capacitor is 25 hours for 3µA.

Note: The gold capacitor maximum voltage is 2.5V.

5.3.2.2. Non-Rechargeable Battery

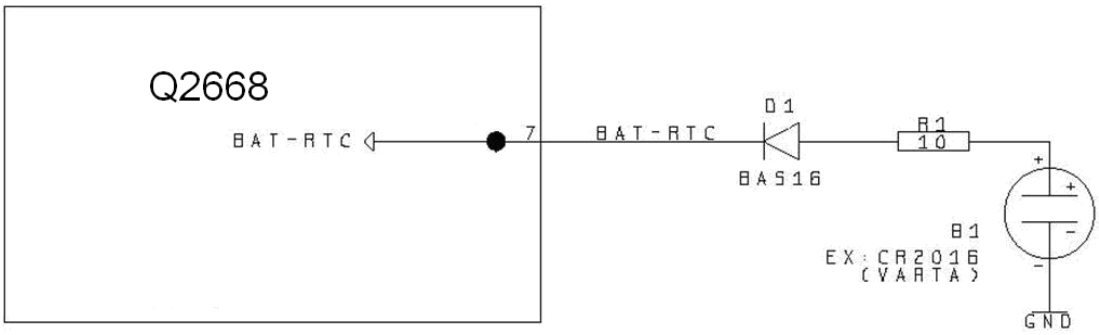


Figure 41. RTC Supplied by a Non-Rechargeable Battery

The diode D1 is mandatory, in order to protect the non-rechargeable battery.

Estimated range with 85mAh battery: 800 h minimum.

5.3.2.3. Rechargeable Battery Cell

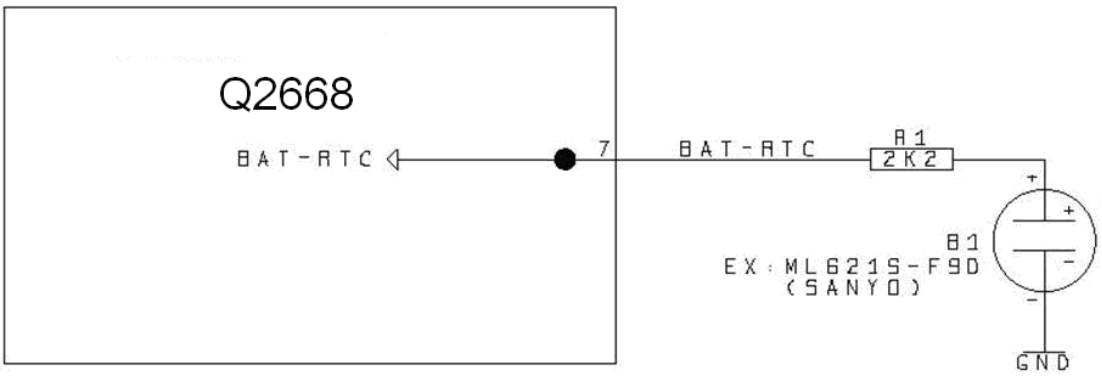


Figure 42. RTC Supplied by a Rechargeable Battery Cell

Estimated range with 2mAh rechargeable battery: ~15 hours.

Caution: *Ensure that cell voltage is lower than 2.63V before battery cell assembly to avoid any damage to the Q2668.*

5.4. Buzzer Output

This output is controlled by a pulse width modulation controller and may be used only as buzzer.

BUZZER0 is an open drain output. A buzzer can be directly connected between this output and VBATT. The maximum current is 100mA (PEAK).

5.4.1. Pin Description

Refer to the following table for the pin description of the buzzer output.

Table 51. PWM/Buzzer Output Pin Description

Pin Number	Signal	I/O	I/O Type	Reset State	Description
15	BUZZER0	O	Open drain	Z	Buzzer output

Refer to section 4.2 Electrical Information for Digital I/O for open drain, 2V9 and 1V8 voltage characteristics and reset state definitions.

5.4.2. Electrical Characteristics

Refer to the following table for the electrical characteristics of the buzzer output.

Table 52. Electrical Characteristics of the Buzzer Output

Parameter	Condition	Minimum	Maximum	Unit
V_{OL} on	Iol = 100mA		0.4	V
I_{PEAK}	VBATT = VBATTmax		100	mA
Frequency		100	8000	Hz

5.4.3. Application

The maximum peak current is 80mA and the maximum average current is 40mA. A diode against transient peak voltage must be added as described below.

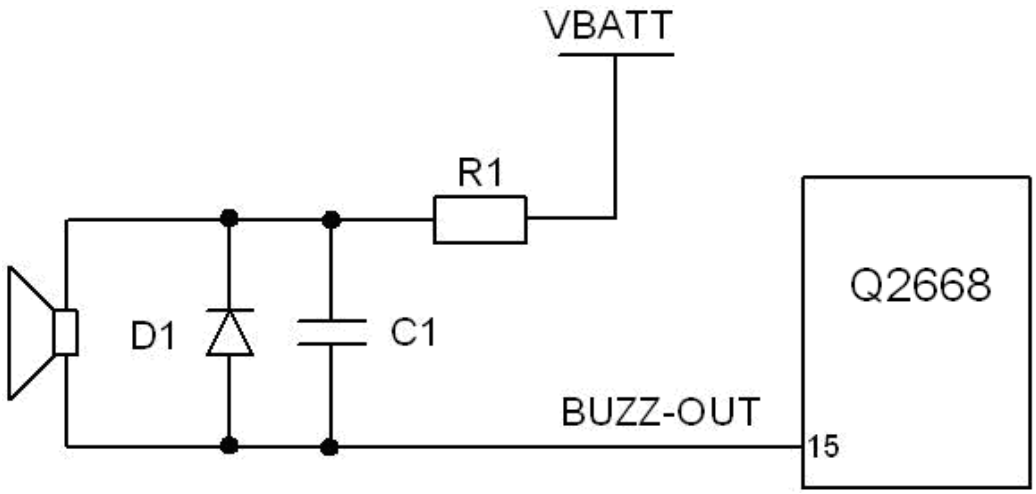


Figure 43. Example of Buzzer Implementation

Where:

- R1 must be selected in order to limit the current at I_{PEAK} max
- C1 = 0 to 100nF (depends on the buzzer type)
- D1 = BAS16 (for example)

Recommended characteristics for the buzzer:

- Electro-magnetic type
- Impedance: 7 to 30Ω
- Sensitivity: 90dB SPL min @ 10cm
- Current: 60 to 90mA

BUZZ-OUT output may also be used to drive a LED as shown in the following figure.

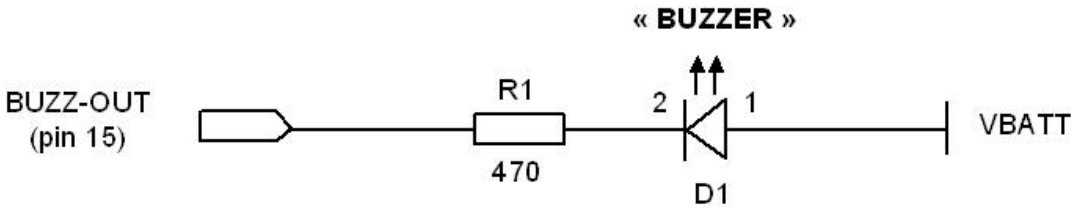


Figure 44. Example of LED driven by the BUZZ-OUT output

R1 value depends on the LED (D1) characteristics.

5.4.3.1. Recommended Characteristics

- Type :electro-magnetic
- Impedance :7Ω to 30Ω
- Sensitivity :90dB SPL minimum @ 10cm
- Current :60mA to 90mA

5.5. External Interrupt

The Q2668 provides three external interrupt inputs. These interrupt inputs can be activated on:

- High to low edge
- Low to high edge
- Low to high and high to low edge

When used, the interrupt inputs must not be left open.

If not used, they must be configured as GPIOs.

5.5.1. Pin Description

Refer to the following table for the pin description of the external interrupt.

Table 53. External Interrupt Pin Description

Pin Number	Signal	I/O	I/O Type	Reset State	Description	Multiplexed With
49	INT1	I	2V9	-	External Interrupt 1	GPIO25
50	INT0	I	1V8	-	External Interrupt 0	GPIO3
51	INT2	I	1V8	-	External Interrupt 2	~CS2 / GPIO1

Refer to section 4.2 Electrical Information for Digital I/O for open drain, 2V9 and 1V8 voltage characteristics and reset state definitions.

5.5.2. Electrical Characteristics

Refer to the following table for the electrical characteristics of the external interrupt.

Table 54. Electrical Characteristics of the External Interrupt

Parameter		Minimum	Maximum	Unit
INT1	V_{IL}		0.3	V
	V_{IH}	2.7		V
INT0 , INT2	V_{IL}		0.3	V
	V_{IH}	1.6		V

5.5.3. Application

The external interrupts are high impedance input types so it is important to set the interrupt input signals with pull-up or pull-down resistors if they are driven by an open drain, an open collector or by a switch. If the interrupt signals are driven by a push-pull transistor, then no pull-up or pull-down resistors are necessary.

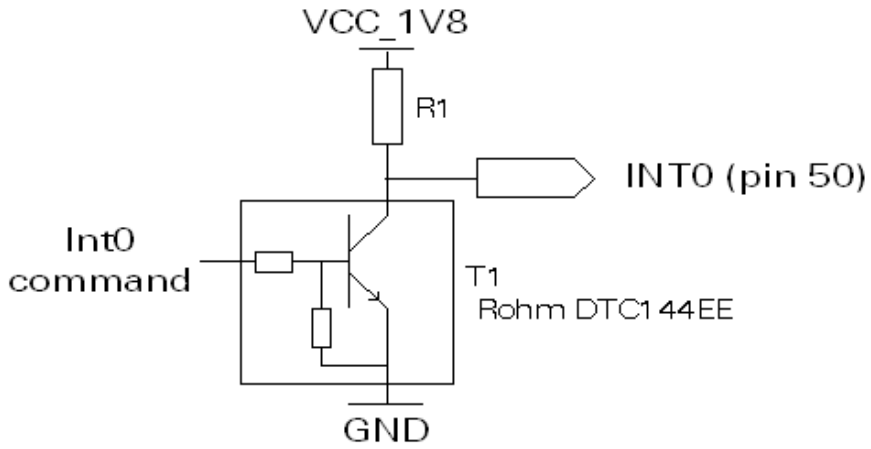


Figure 45. Example of INT0 Driven by an Open Collector

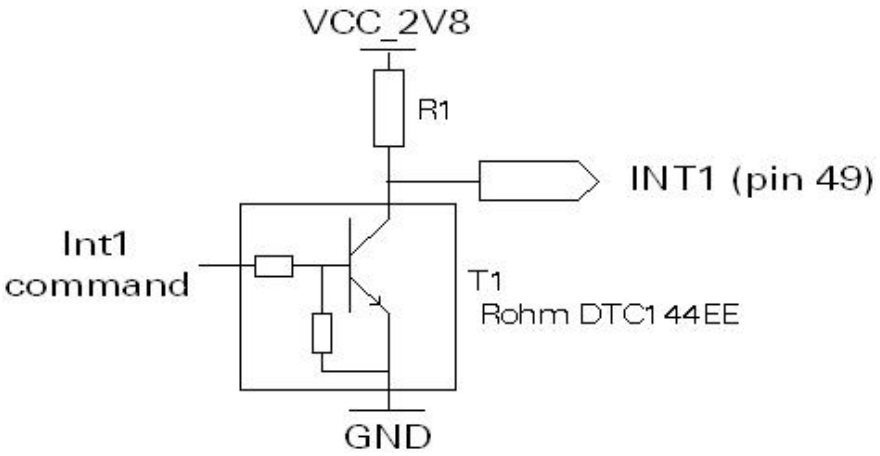


Figure 46. Example of INT1 Driven by an Open Collector

where:

- The value of R1 can be 47kΩ
- T1 can be a ROHM DTC144EE open collector transistor

5.6. VCC_2V9 and VCC_1V8 Output

These outputs may be used to power some external functions and only available when the Q2668 is ON.

These digital power supplies are mainly used to:

- Pull-up signals such as I/O
- Supply the digital transistors driving the LEDs
- Supply the SIMPRES signal
- Act as a voltage reference for ADC interface AUX-ADC (only for VCC_2V9)

The maximum current to be provided by each output is 15mA.

Note: This output is only available when the embedded module is ON.

5.6.1. Pin Description

Refer to the following table for the pin description of the VCC_2V9 and VCC_1V8 output.

Table 55. VCC_2V9 and VCC_1V8 Pin Description

Pin Number	Signal	I/O	I/O Type	Description
5	VCC_1V8	O	Supply	Digital supply
10	VCC_2V9	O	Supply	Digital supply

Refer to section 4.2 Electrical Information for Digital I/O for open drain, 2V9 and 1V8 voltage characteristics and reset state definitions.

5.6.2. Electrical Characteristics

Refer to the following table for the electrical characteristics of the VCC_2V9 and VCC_1V8 output signals.

Table 56. Electrical Characteristics of the VCC_2V9 and VCC_1V8 Signals

Parameter		Minimum	Typical	Maximum	Unit
VCC_2V9	Output voltage	2.7	2.8	2.95	V
	Output Current			15	mA
VCC_1V8	Output voltage	1.7	1.8	1.9	V
	Output Current			15	mA

5.7. LED0 Signal

LED0 is an open drain output. An LED and a resistor can be directly connected between this output and VBATT.

When the Q2668 is OFF, if 2.8V < VBATT < 3.2V and a charger is connected on the CHG-IN inputs, this output flashes (100ms ON, 900ms OFF) to indicate the pre-charging phase of the battery.

When the Q2668 is ON, this output is used to indicate network status.

Table 57. LED0 Status

Q2668 State	VBATT Status	LED0 Status	Q2668 Status
OFF	VBATT< 2.8V or VBATT> 3.2V	OFF	Q2668 is OFF
	2.8V < VBATT < 3.2V	Pre-charge flash LED ON for 100ms, OFF for 900ms	Q2668 is OFF, Pre-charging mode (charger must be connected on CHG-IN to activate this mode)
ON	VBATT > 3.2V	Permanent	Q2668 switched ON, not registered on the network
		Slow flash LED ON for 200ms, OFF for 2s	Q2668 switched ON, registered on the network
		Quick flash LED ON for 200ms, OFF for 600ms	Q2668 switched ON, registered on the network, communication in progress
		Very quick flash LED ON for 100ms, OFF for 200ms	Q2668 switched on, software downloaded is either corrupted or non-compatible ("BAD SOFTWARE")

5.7.1. Pin Description

Refer to the following table for the pin description of LED0.

Table 58. LED0 Pin Description

Pin Number	Signal	I/O	I/O Type	Reset State	Description
17	LED0	O	Open Drain Output	1 and Undefined	LED driving

Refer to section 4.2 Electrical Information for Digital I/O for open drain, 2V9 and 1V8 voltage characteristics and reset state definitions.

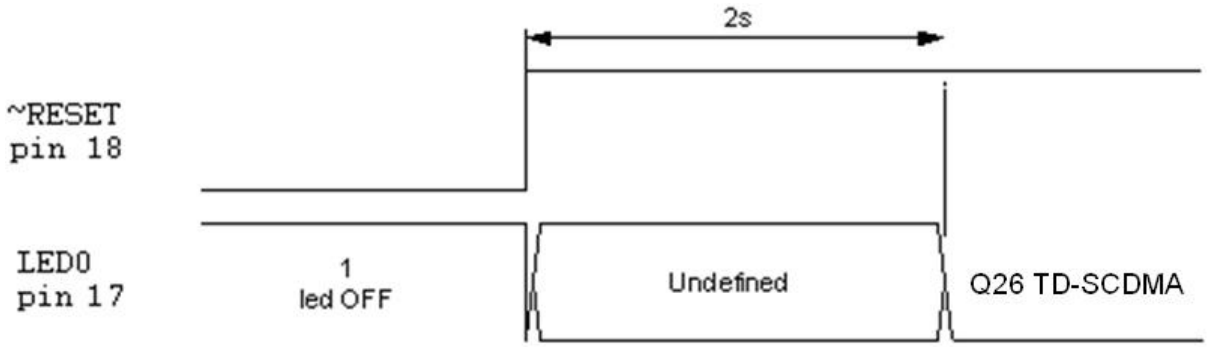


Figure 47. LED0 State During RESET and Initialization Time

LED0 state is high during the RESET time and undefined during the software initialization time. During software initialization time, for 2 seconds max after RESET cancellation, the LED0 signal is toggling and does not provide Q2668 status. After the 2s period, the LED0 provides the true status of the Q2668.

5.7.2. Electrical Characteristics

Refer to the following table for the electrical characteristics of the LED0 signal.

Table 59. Electrical Characteristics of the LED0 Signal

Parameter	Condition	Minimum	Typical	Maximum	Unit
V_{OL}				0.4	V
I_{OUT}				10	mA

5.7.3. Application

The GSM activity status indication signals LED0 (pin 17) may be used to drive a LED. This signal is an open-drain digital transistor in accordance to the Q2668 activity status.

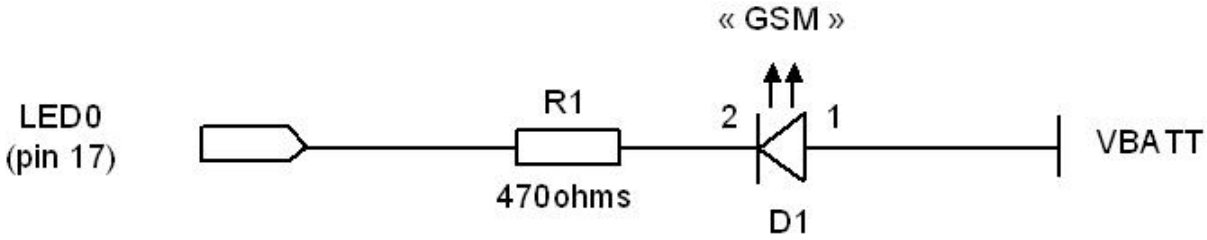


Figure 48. Example of GSM Activity Status Implementation

R1 value may be harmonized depending on the LED (D1) characteristics.

5.8. Analog to Digital Converter

Two Analog to Digital Converter inputs are provided by the Q2668. These converters are 10-bit resolution ADCs ranging from 0V to 2V.

Typically, the BAT-TEMP/ADC1 input is used to monitor external temperature. This is very useful for monitoring the application temperature and can be used as an indicator to safely power OFF the application in case of overheating (for Li-Ion batteries). For more information, refer to section 4.12 Battery Charging Interface.

The ADC2 input can be used for customer specific applications.

5.8.1. Pin Description

Refer to the following table for the pin description of the ADC.

Table 60. ADC Pin Description

Pin Number	Signal	I/O	I/O Type	Description
20	ADC1/ BAT-TEMP*	I	Analog	A/D converter
21	ADC2	I	Analog	A/D converter

* This input can be used for a battery charging temperature sensor. For more information, refer to section 4.12 Battery Charging Interface.

5.8.2. Electrical Characteristics

Refer to the following table for the electrical characteristics of the ADC.

Table 61. ADC Electrical Characteristics

Parameter		Minimum	Typical	Maximum	Unit
Maximum output code			1635		LSB
Sampling period				3*	s
Input signal range		0		2	V
Input impedance	ADC1/BAT-TEMP		1M		Ω
	ADC2		1M		Ω

* Sampling rate for ADC2 only

6. Power Consumption

6.1.1. Power Consumption

Power consumption is dependent on the configuration used. It is for this reason that the following consumption values are given for each mode, RF band and type of software used.

All the following information is given assuming a 50Ω RF output.

The following consumption values were obtained by performing measurements on the Q2668 samples at a temperature of 25°C.

Three VBATT values are used to measure the consumption, VBATTmin (3.7V), VBATTmax (4.5V) and VBATTtyp (4.0V).

The average current is given for the three VBATT values and the peak current given is the maximum current peak measured with the three VBATT voltages.

First let's define start-up current in view to avoid start issues.

6.1.1.1. Power Consumption Processing

Table 62. Power Consumption Processing; Typical Values

Note: TX means that the current peak is the RF transmission burst (Tx burst)

RX means that the current peak is the RF reception burst (Rx burst)

Operating Mode VBATT=4V	Parameters	I_{NOM} average			Unit
		Min	Typ	Max	
SLEEP Mode			2		mA
ACTIVE Mode			60		mA
SLEEP mode with telecom stack in Idle Mode[1]	Case 2G (Paging 9/Rx burst occurrence ~2s)		6		mA
	Case 2G (Paging 2/Rx burst occurrence ~0,5s)		8		mA
	Case TD (5.12S)		4		mA
ACTIVE mode with telecom stack in Idle Mode[1]	Case 2G (Paging 9/Rx burst occurrence ~2s)		58		mA
	Case 2G (Paging 2/Rx burst occurrence ~0,5s)		60		mA
	Case TD (5.12S)		58		mA
Peak current in GSM/GPRS Mode	900 MHz - PCL5/gam.3 (TX power 33dBm)		0.25	1.5	A
	1800 MHz - PCL0/gam.3 (TX power 30dBm)		0.16	1.0	A
GSM Connected Mode (Voice)	900 MHz - PCL5 (TX power 33dBm)		282	1579	mA
	900 MHz - PCL19 (TX power 5dBm)		118	358	mA
	1800 MHz - PCL0 (TX power 30dBm)		246	1080	mA
	1800 MHz - PCL15 (TX power 0dBm)		117	354	mA
GPRS Transfer Mode class 8 (4Rx/1Tx)	900 MHz - gam. 3(TX power 33dBm)		264	1559	mA
	1800 MHz - gam.3(TX power 30dBm)		204	1048	mA
GPRS Transfer	900 MHz - gam.3 (TX power 30dBm)		421	1475	mA

Operating Mode VBATT=4V		Parameters	I_{NOM} average			Unit
			Min	Typ	Max	
Mode class 10 (3Rx/2Tx)		1800 MHz - gam.3 (TX power 27dBm)		301	953	mA
EGPRS Transfer Mode class 8 (4Rx/1Tx)		900 MHz - gam.6 (TX power 27dBm)		209	1527	mA
		1800 MHz - gam.5 (TX power 26dBm)		194	895	mA
EGPRS Transfer Mode class 10 (3Rx/2Tx)		900 MHz - gam.6 (TX power 24dBm)		326	1430	mA
		1800 MHz - gam.5 (TX power 23dBm)		300	950	mA
TD-SCDMA	Voice	BAND F@ +23 dBm 1880~1920MHZ		200		mA
		BAND F @ +10 dBm 1880~1920MHZ		160		mA
		BAND A @ +23dBm 2010~2025MHZ		200		mA
		BAND A @ +10 dBm 2010~2025MHZ		160		mA
	Data Transfer	BAND F @ +23 dBm 1880~1920MHZ		180		mA
		BAND F @ +10 dBm 1880~1920MHZ		140		mA
		BAND A @ +23 dBm 2010~2025MHZ		180		mA
		BAND A @ +10 dBm 2010~2025MHZ		140		mA

1 This Mode consumption is dependent on the USIM card used. Some USIM cards respond faster than others, the longer the response time, the higher the consumption. The measurements were performed with a large number of 3V USIM cards, the results in brackets are the minimum and maximum currents measured from among all the USIMs used.

7. Consumption Measurement Procedure

This chapter describes the consumption measurement procedure used to obtain the Q2668 Embedded Module consumption specification.

7.1. Hardware Configuration

Consumption results are highly dependent on the hardware configuration used during measurement and this section describes the hardware configuration settings that must be used to obtain optimum consumption measurements.

The following hardware configuration includes both the measurement equipment used and the Q2668 embedded module on the Q26 Series Development Kit board v3.

7.1.1. Equipments Used

Four devices were used to perform consumption measurement:

- Network Analyzer
- Current Measuring Power Supply
- Standalone Power Supply
- Computer, to control the embedded module and to save measurement data
- MT8820B from Anritsu

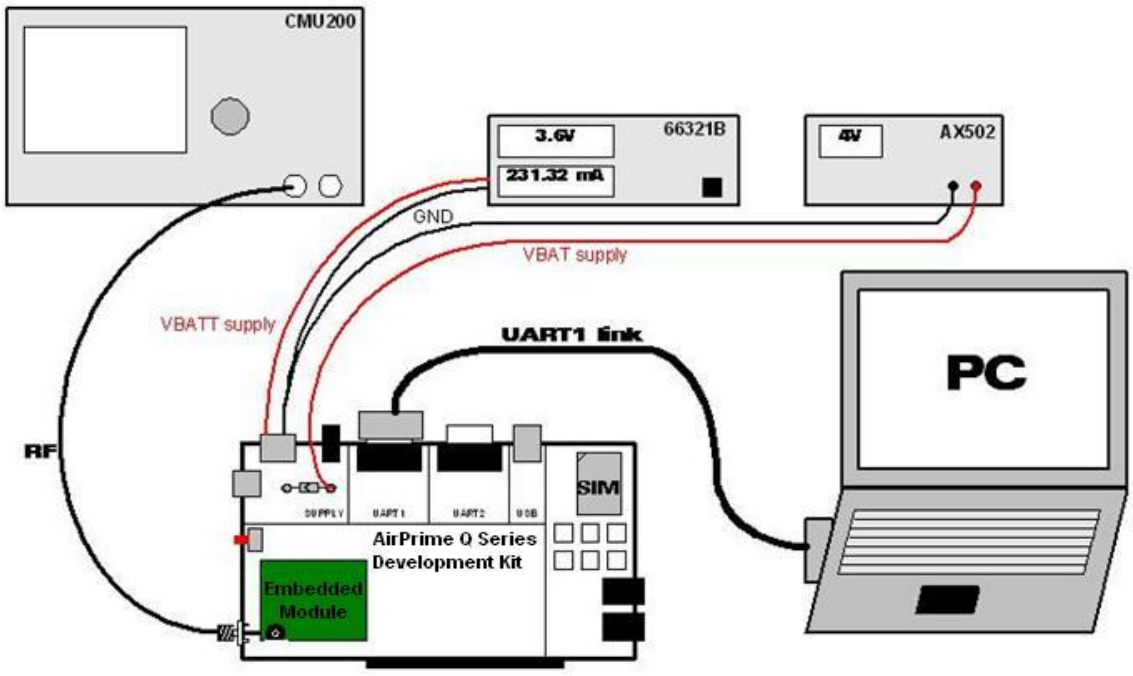


Figure 49. Typical Hardware Configuration

The **network analyzer** is a **CMU 200** from **Rhode & Schwartz**, or an **MT8820B** from **Anritsu**. This analyzer offers all GSM/GPRS/EGPRS network configurations required and allows a wide range of network configurations to be set.

The **AX502** standalone power supply is used to supply all development kit board components except the embedded module. The goal is to separate the development kit board consumption from the embedded module consumption which is measured by the other power supply, the **66321B** "current measuring power supply".

The "current measuring power supply" is also connected and controlled by the computer (GPIB control not shown in the previous figure).

A SIM must be inserted in the Q26 Series Development Kit during all consumption measurements.

The following table lists the recommended equipments to use for the consumption measurement.

Table 63. Recommended Equipments

Device	Manufacturer	Reference	Notes
Network analyzer	Rhode & Schwartz	CMU 200	Quad Band GSM/DCS/GPRS/EGPRS
Current measuring power supply	Agilent	66321B	Used for VBATT
Standalone power supply	Metrix	AX502	Used for VBAT

7.1.2. Q26 Series Development Kit Board v3

The Q26 Series Development Kit Board v3 is used as a basis for the Q2668 embedded module measurements using several settings. For more information about these settings, refer to document [3] AirPrime Q26 Series Development Kit User Guide.

The Q26 Series Development Kit board is powered by the standalone power supply VBAT; while the Q2668 embedded module is powered by the current measuring power supply, VBATT. Because of this, the link between VBATT and VBAT (J103) must be opened (by removing the solder at the top of the board in the SUPPLY area).

- VBATT is powered by the current measuring power supply **66321B**
- VBAT is powered by the standalone power supply **AX502**

Also take note of the following additional configuration/settings:

- The R100 resistor (around the BAT-TEMP connector) must be removed.
- The UART2 link is not used; therefore, J501, J502, J503 and J504 must be opened (by removing the solder).
- UART2 R502 must be removed; R507 must be soldered with a 0Ω resistor.
- The USB link is not used; therefore, J801, J802 and J803 must be opened (by removing the solder).
- UART1 R408 must be removed; R406 must be soldered with a 0Ω resistor.
- The standalone power supply, VBAT, may be set to 4V.

The goal of the settings listed above is to eliminate all bias current from VBATT and to supply the entire board (except the embedded module) using only VBAT.

Note: When measuring the current consumption in alarm mode, it is necessary to remove D100, D103 and R103 from the Q26 Series Development Kit in order to have accurate results.

7.1.3. SIM Cards

Consumption measurement may be performed with either 3-Volt or 1.8-Volt SIM cards. However, all specified consumption values are for a 3-Volt SIM card.

Note: The SIM card's voltage is supplied by the embedded module's power supply. Consumption measurement results may vary depending on the SIM card used.

7.2. Software Configuration

The software configuration for the equipment(s) used and the Q2668 embedded module settings are presented in the following sub-sections.

7.2.1. Embedded Module Configuration

The software configuration for the embedded module is done by selecting the operating mode to use in performing the measurement.

A description of the operating modes and the procedures used to change the operating mode are given in document [1] AirPrime Q2668 AT Command Set.

The available operating modes in the Q2668 embedded module are as follows:

- Active Idle Mode
- Sleep Idle Mode
- Active Mode
- Sleep Mode
- Connected Mode
- Transfer Mode class 8 (4Rx/1Tx)
- Transfer Mode class 10 (3Rx/2Tx)

7.2.2. Equipment Configuration

The network analyzer is set according to the embedded module's operating mode.

Paging during Idle modes, TX burst power, RF band and GSM/DCS/GPRS/EGPRS may be selected on the network analyzer.

Refer to the following table for the network analyzer configuration according to operating mode.

Table 64. Operating Mode Configuration

Operating Mode	Network Analyzer Configuration
SLEEP Mode	N/A
ACTIVE Mode	N/A
SLEEP mode with telecom stack in Idle Mode	Paging 9/Rx burst occurrence ~2s
	Paging 2/Rx burst occurrence ~0,5s
ACTIVE mode with telecom stack in Idle Mode	Paging 9/Rx burst occurrence ~2s
	Paging 2/Rx burst occurrence ~0,5s
Peak current in GSM/GPRS Mode	850/900 MHz - PCL5/gam.3 (TX power 33dBm)

Operating Mode	Network Analyzer Configuration
	1800/1900 MHz - PCL0/gam.3 (TX power 30dBm)
GSM Connected Mode (Voice)	850/900 MHz - PCL5 (TX power 33dBm)
	850/900 MHz - PCL19 (TX power 5dBm)
	1800/1900 MHz - PCL0 (TX power 30dBm)
	1800/1900 MHz - PCL15 (TX power 0dBm)
GPRS Transfer Mode class 10 (3Rx/2Tx)	850/900 MHz - gam.3 (TX power 30dBm)
EGPRS Transfer Mode class 10 (3Rx/2Tx)	850/900 MHz - gam.6 (TX power 24dBm)
	1800/1900 MHz - gam.5 (TX power 23dBm)

The standalone power supply, VBAT, may be set from 3.2V to 4.8V.

The current measuring power supply, VBATT, may be set from 3.2V to 4.8V according to the Q2668 embedded module VBATT specifications.

8. Reliability Compliance and Recommended Standards

8.1. Reliability Compliance

The AirPrime Q2668 embedded module connected on a development kit board application is compliant with the following requirements.

Table 65. Standards Conformity for the Q2668 Embedded Module

Abbreviation	Definition
IEC	International Electro technical Commission
ISO	International Organization for Standardization

8.2. Applicable Standards Listing

The table hereafter gives the basic list of standards applicable to the Q2668 embedded module.

Note: References to any features can be found from these standards.

Table 66. Applicable Standards and Requirements

Document	Current Version	Title
IEC6006826	7.0	Environmental testing - Part 2.6: Test FC: Sinusoidal Vibration.
IEC60068234	73	Basic environmental testing procedures part 2: Test FD: random vibration wide band - general requirements Cancelled and replaced by **IEC60068-2-64**. For reference only.
IEC60068264	2.0	Environmental testing - part 2-64: Test FH: vibration, broadband random and guidance.
IEC60068232	2.0	Basic environmental testing procedures - part 2: Test ED: (procedure 1) (withdrawn & replaced by IEC60068-2-31).
IEC60068231	2.0	Environmental testing part 2-31: Test EC: rough handling shocks, primarily for equipment-type specimens.
IEC60068229	2.0	Basic environmental testing procedures - part 2: Test EB and guidance: bump Withdrawn and replaced by **IEC60068-2-27**. For reference only.
IEC60068227	4.0	Environmental testing - part 2-27: Test EA and guidance: shock.
IEC60068214	6.0	Environmental testing - part 2-14: Test N: change of temperature.
IEC6006822	5.0	Environmental testing - part 2-2: Test B: dry heat.
IEC6006821	6.0	Environmental testing - part 2-1: Test A: cold.
IEC60068230	3.0	Environmental testing - part 2-30: Test DB: damp heat, cyclic (12 h + 12 h cycle).
IEC6006823	69 w/A1	Basic environmental testing procedures part 2: Test CA: damp heat, steady State Withdrawn and replaced by **IEC60068-2-78**. For reference only.
IEC60068278	1.0	Environmental testing part 2-78: Test CAB: damp heat, steady state.

Document	Current Version	Title
IEC60068238	2.0	Environmental testing - part 2-38: Test Z/AD: composite temperature/humidity cyclic test.
IEC60068240	1.0 w/A1	Basic environmental testing procedures - part 2: Test Z/AM combined cold/low air pressure tests.
ISO167501	2ND	Road vehicles - environmental conditions and testing for electrical and electronic equipment - part 1: general.
ISO167502	2ND	Road vehicles - environmental conditions and testing for electrical and electronic equipment - part 2: electrical loads.
ISO167503	2ND	Road vehicles - environmental conditions and testing for electrical and electronic equipment - part 3: mechanical loads.
ISO167504	2ND	Road vehicles - environmental conditions and testing for electrical and electronic equipment - part 4: climatic loads.
IEC60529	2.1 w/COR2	Degrees of protection provided by enclosures (IP code).
IEC60068217	4.0	Basic environmental testing procedures - part 2: Test Q: sealing.
IEC60068218	2.0	Environmental testing - part 2-18: Tests - R and guidance: water.
IEC60068270	1.0	Environmental testing - part 2: tests - test XB: abrasion of markings and letterings caused by rubbing of fingers and hands.
IEC60068268	1.0	Environmental testing - part 2: tests - test l: dust and sand.
IEC60068211	3.0	Basic environmental testing procedures, part 2: test KA: salt mist.
IEC60068260	2.0	Environmental testing - part 2: Test KE: flowing mixed gas corrosion test.
IEC60068252	2.0 w/COR	Environmental testing - part 2: Test KB: salt mist, cyclic (sodium chloride solution).

8.3. Environmental Specifications

The Q2668 embedded module is compliant with the operating classes listed in the table below. The ideal temperature range of the environment for each operating class is also specified.

Table 67. Operating Class Temperature Range

Conditions	Temperature Range
Operating / Class A	-20 °C to +55°C
Operating / Class B	-30 °C to +75°C
Storage	-40 °C to +80°C

8.3.1. Function Status Classification

The classes reported below comply with the Annex "ISO Failure Mode Severity Classification", ISO Standard 7637, and Section 1.

Note: The word "function" as used here concerns only the function performed by the Q2668 embedded module.

Table 68. ISO Failure Mode Severity Classification

Class	Definition
CLASS A	The Q2668 embedded module remains fully functional during and after environmental exposure; and shall meet the minimum requirements of 3GPP or appropriate wireless standards.
CLASS B	The Q2668 embedded module remains fully functional during and after environmental exposure; and shall exhibit the ability to establish a voice, SMS or DATA call at all times even when one or more environmental constraint exceeds the specified tolerance. Unless otherwise stated, full performance should return to normal after the excessive constraint(s) have been removed.

8.4. Reliability Prediction Model

8.4.1. Life Stress Test

The following tests the Q2668 embedded module's product performance.

Table 69. Life Stress Test

Designation	Condition
Performance Test PT3T° & PT 	Standard: N/A
	Special conditions: • Temperature: ▪ Class A: -20°C to +55°C ▪ Class B: -30°C to +75°C ▪ Rate of temperature change: ± 3°C/min • Recovery time: 3 hours
	Operating conditions: Powered
	Duration: 14 days

8.4.2. Environmental Resistance Stress Test

The following tests the Q2668 embedded module's resistance to extreme temperature.

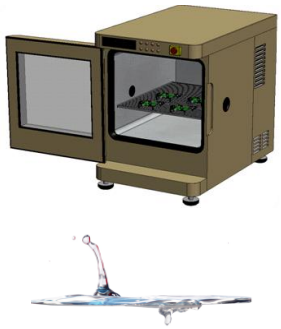
Table 70. Environmental Resistance Stress Test

Designation	Condition
Cold Test **COT** 	Standard: IEC 680068-2-1, Test Ab
	Special conditions: • Temperature: -40°C • Rate of temperature change: dT/dt >= ± 3°C/min • Recovery time: 3 hours
	Operating conditions: Un-powered
	Duration: 72 hours

8.4.3. Corrosive Resistance Stress Test

The following tests the Q2668 embedded module's resistance to corrosive atmosphere.

Table 71. Corrosive Resistance Stress Test

Designation	Condition
Moist Heat Cyclic Test **MHCT** 	Standard: IEC 60068-2-30, Test Db
	Special conditions: • Upper temperature: +55 ± 2°C • Lower temperature: +25 ± 2°C • RH: ▪ Upper temperature: 93% ▪ Lower temperature: 95% • Number of cycles: 21 (1 cycle/24 hours) • Rate of temperature change: dT/dt >= ± 3°C/min • Recovery time: 3 hours
	Operating conditions: Un-powered
	Duration: 21 days

8.4.4. Thermal Resistance Cycle Stress Test

The following tests the Q2668 embedded module's resistance to extreme temperature cycling.

Table 72. Thermal Resistance Cycle Stress Test

Designation	Condition
Thermal Shock Test TSKT 	Standard: IEC 60068-2-14
	Special conditions: • Upper temperature: +90°C • Lower temperature: -40°C • Rate of temperature change: 30s • Number of cycles: 200 • Duration of exposure: 30 minutes • Recovery time: 3 hours
	Operating conditions: Un-powered
	Duration: 72 hours

8.4.5. Mechanical Resistance Stress Tests

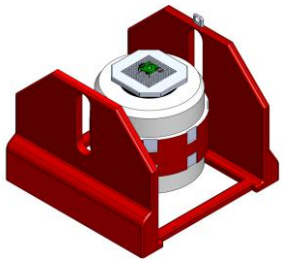
The following tests the Q2668 embedded module's resistance to vibrations and mechanical shocks.

Table 73. Mechanical Resistance Stress Tests

Designation	Condition
Sinusoidal Vibration Test SVT 	Standard: IEC 60068-2-6, Test Fc

	Special conditions:
	• Frequency range: 10Hz to 1000Hz
	  ▪ Displacement: ±5mm (peak)
	• Frequency range: 16Hz to 62Hz
	  ▪ Acceleration: 5G
	• Frequency range: 62Hz to 200Hz
	  ▪ Acceleration: 3G
	• Frequency range: 200Hz to 1000Hz
	  ▪ Acceleration: 1G
	• Sweep rate: 1 oct/min.
	• Test duration: 20 cycles
	• Sweep directions: X, Y and Z

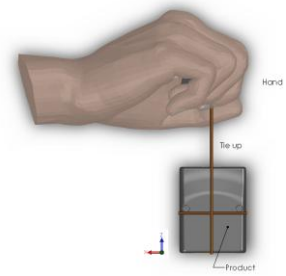
	Operating conditions: Un-powered
	Duration: 72 hours
Random Vibration Test	Standard: IEC 60068-2-64

Designation	Condition
RVT 	Special conditions: • Density spectrum: 0.96m²/s3 • Frequency range: ▪ 0.1 g^2/Hz at 10Hz ▪ 0.01 g^2/Hz at 250Hz ▪ 0.0005 g^2/Hz at 1000Hz ▪ 0.0005 g^2/Hz at 2000Hz • Slope: -3dB/octave • Acceleration: 0.9gRMS • Number of axis: 3
	Operating conditions: Un-powered
	Duration: 16 hours
Mechanical Shock Test MST 	Standard: IEC 60068-2-27, Test Ea
	Special conditions: • Shock Test 1: ▪ Wave form: Half sine ▪ Peak acceleration: 30G ▪ Duration: 11ms ▪ Number of shocks: 8 per direction ▪ Number of directions: 6 (±X, ±Y, ±Z) • Shock Test 2: ▪ Wave form: Half sine ▪ Peak acceleration: 200G ▪ Duration: 3ms ▪ Number of shocks: 3 per direction ▪ Number of directions: 6 (±X, ±Y, ±Z) • Shock Test 3: ▪ Wave form: Half sine ▪ Peak acceleration: 100G ▪ Duration: 6ms ▪ Number of shocks: 3 per direction ▪ Number of directions: 6 (±X, ±Y, ±Z)
	Operating conditions: Un-powered
	Duration: 72 hours

8.4.6. Handling Resistance Stress Tests

The following tests the Q2668 embedded module's resistance to handling malfunctions and damage.

Table 74. Handling Resistance Stress Tests

Designation	Condition
ESD Test 	Standard: IEC 1000-4-2
	Special conditions: • Contact discharges: 10 positive and 10 negative applied • Voltage: ±2kV, ±4kV, ±6kV
	Operating conditions: Powered
	Duration: 24 hours
Free Fall Test **FFT** 	Standard : IEC 60068-2-32, Test Ed
	Special conditions: • Drop: 2 samples for each direction • Equivalent drop height: 1m • Number of directions: 6 (±X, ±Y, ±Z) • Number of drops/face: 2
	Operating conditions: Un-powered
	Duration: 24 hours

9. Connector and Peripheral Device References

9.1. General Purpose Connector

The GPC is a 100-pin connector with 0.5mm pitch from the from PANASONIC Group's P5K series, with the following reference:

AXK600347BN1

The mating connector has the following reference:

AXK500147BN1J

The stacking height is 3.0 mm.

Sierra Wireless recommends that the **AXK500147BN1J** connector be used for applications to benefit from Sierra Wireless prices. For more information, contact Panasonic and quote the Sierra Wireless connector reference: **WM18868**.

For more information about the recommended GPC, refer to the GPC data sheets available from Panasonic (see http://panasonic-denko.co.jp/ac/e/control/connector/base-base/p5k/index.jsp).

9.2. USIM Card Reader

- AMPHENOL C707 series (see http://www.amphenol.com)
- JAE (see http://www.jae.co.jp)
- MOLEX (see http://www.molex.com)
  - Connector reference: 99228-0002
  - Holder reference: 91236-0002

9.3. Microphone

Possible suppliers:

- HOSIDEN (see http://www.hosiden.co.jp/)
- PANASONIC (see http://www.panasonic/com/industrial/components/)
- PEIKER

9.4. Speaker

Possible suppliers:

- SANYO (see http://www.sanyo.com/industrial/components/)
- HOSIDEN (see http://www.hosiden.co.jp/)
- PRIMO (see http://www.primo.com.sg/)
- PHILIPS (see http://www.semiconductors.philips.com/)

9.5. Antenna Cable

There is a main connection for 2G and 3G and a diversity connection only for 3G.

For the main connection we have two possibilities:

- UF-L pigtails connection on the bottom side
- Coaxial cable soldered to the RF pad (opposite side of the UF-L connector) on the top side

For the diversity connection the only possibility is to solder a coaxial cable to the second RF pad (no UF-L connector on the opposite side) on the top side.

A wide variety of cables fitted with UF-L connectors is offered by Murata:

- UF-L pigtails, Ex: Ref = **MXYH75-TYPE**
- UF-L Ref = **MM9329-2700B**
- UF-L cable assemblies,
- Between series cable assemblies.

More information is also available from www.murata.com.cn/products/microwave/index.html.

For the coaxial cable soldered on the RF pad the following references have been certified for mounting on the Q2668:

- RG178
- RG316

9.6. RF Antenna

RF antennas and support for antenna adaptation can be obtained from manufacturers such as:

- TAOGLAS (http://www.taoglas.com)
- HIRSCHMANN (http://www.hirschmann.com/)
- IPEX (http://www.i-pex.com/)
- Murata (http://www.murata.com.cn/)

9.7. Buzzer

One possible Buzzer supplier is:

- SAMBU (see http://www.sambuco.co.kr)

10. Design Guidelines

The purpose of the following paragraphs is to present design guidelines.

10.1. Hardware and RF

10.1.1. EMC Recommendations

The EMC tests must be performed on the application as soon as possible to detect any potential problems.

When designing, special attention should be paid to:

- Possible spurious emission radiated by the application to the RF receiver in the receiver band.
- ESD protection **is mandatory** on all signals which have external accessibility (typically human accessibility).

  Typically, ESD protection is mandatory for the:

  - USIM (if accessible from outside)
  - Serial link
- EMC protection on audio input/output (filters against 900MHz emissions).
- Biasing of the microphone inputs.
- Length of the USIM interface lines (preferably <10cm).
- Ground plane: Sierra Wireless recommends a common ground plane for analog/digital/RF grounds.
- A metallic case or plastic casing with conductive paint are recommended.

Note: *The Q2668 does not include any protection against over-voltage.*

10.1.2. Power Supply

The power supply is one of the key issues in the design of a terminal.

A weak power supply design could, in particular, affect:

- EMC performance
- The emission spectrum
- The phase error and frequency error

Warning: *Careful attention should be paid to the quality of the power supply: low ripple, PFM or PSM systems should be avoided (PWM converter preferred), and the capacity to deliver high current peaks in a short time (pulsed radio emission).*

10.1.3. Layout Requirements

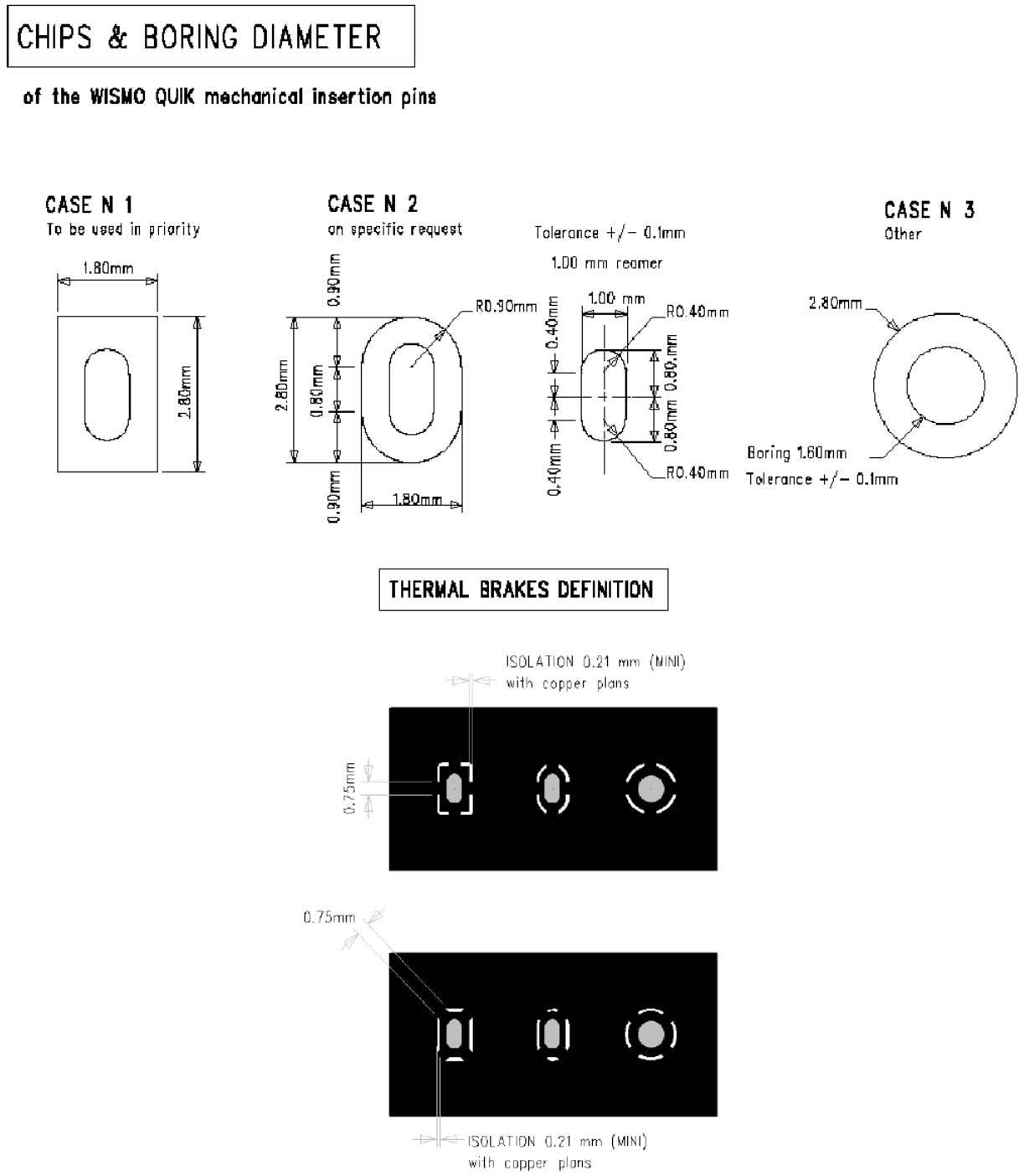


Figure 50. Layout Requirement

10.1.4. Antenna

Caution: *Sierra Wireless strongly recommends working with an antenna manufacturer either to develop an antenna adapted to the application or to adapt an existing solution to the application.*

Both the mechanical and electrical antenna adaptation is one of the key issues in the design of the GSM/UMTS terminal.

10.2. Mechanical Integration

Attention should be paid to:

- Antenna cable integration (bending, length, position, etc.)
- Leads of the Q2668 to be soldered to the Ground plane

11. References

11.1. Web Site Support

Table 75. Web Site Support Links

Subject Matter	Web Site
General information about Sierra Wireless and its range of products	www.sierrawireless.com
General information about the Q Series Intelligent Embedded Modules	http://www.sierrawireless.com/productsandservices/AirPrime/Embedded_Modules/Q_Series.aspx
Specific support about the Q2668 Embedded Module	http://www.sierrawireless.com/productsandservices/AirPrime/Embedded_Modules/Q_Series/Q2668.aspx
Carrier/Operator approvals	TBC
Developer support for software and hardware	http://forum.sierrawireless.com/

11.2. Reference Documents

For more details, several reference documents can be consulted. The Sierra Wireless documents referenced herein are provided in the Sierra Wireless documentation package; however, the general reference documents which are not Sierra Wireless owned are not provided in the documentation package.

Please check the Sierra Wireless web site at www.sierrawireless.com for the latest documentation available.

11.2.1. AT Software Documentation

[1] AirPrime Q2668 AT Command Set

Reference: WA_DEV_Q2668_UGD_003

[2] AirPrime Q2668 WMMP AT Command Manual

Reference: WA_DEV_Q2668_UGD_005

[3] AirPrime Q26 Series Development Kit User Guide

Reference: WM_BBD_Q26_UGD_001

11.2.2. General Reference Documents

[4] "I^2C Bus Specification and User Guide", Version 3.0, NXP 2007

[5] ISO 7816-3 Standard

12. List of Abbreviations

Abbreviation	Definition
AC	Alternating Current
ADC	Analog to Digital Converter
A/D	Analog to Digital conversion
AF	Audio-Frequency
AT	ATtention (prefix for modem commands)
AUX	AUXiliary
CAN	Controller Area Network
CB	Cell Broadcast
CEP	Circular Error Probable
CLK	CLocK
CMOS	Complementary Metal Oxide Semiconductor
CS	Coding Scheme
CTS	Clear To Send
DAC	Digital to Analog Converter
dB	Decibel
DC	Direct Current
DCD	Data Carrier Detect
DCE	Data Communication Equipment
DCS	Digital Cellular System
DR	Dynamic Range
DSR	Data Set Ready
DTE	Data Terminal Equipment
DTR	Data Terminal Ready
EDGE	Enhanced Data rates for GSM Evolution
EFR	Enhanced Full Rate
EGPRS	Enhanced General Packet Radio Service
E-GSM	Extended GSM
EMC	ElectroMagnetic Compatibility
EMI	ElectroMagnetic Interference
EMS	Enhanced Message Service
EN	ENable
ESD	ElectroStatic Discharges
FIFO	First In First Out
FR	Full Rate
FTA	Full Type Approval
GND	GrouND
GPI	General Purpose Input
GPC	General Purpose Connector
GPIO	General Purpose Input Output
GPO	General Purpose Output
GPRS	General Packet Radio Service

Abbreviation	Definition
GPS	Global Positioning System
GSM	Global System for Mobile communications
HR	Half Rate
HSDPA	High Speed Downlink Packet Access
HSUPA	High Speed Uplink Packet Access
HSxPA	High Speed x(downlink/uplink) Packet Access
I/O	Input / Output
LED	Light Emitting Diode
LNA	Low Noise Amplifier
MAX	MAXimum
MIC	MICrophone
MIN	MINimum
MMS	Multimedia Message Service
MO	Mobile Originated
MT	Mobile Terminated
na	Not Applicable
NF	Noise Factor
NMEA	National Marine Electronics Association
NOM	NOMinal
NTC	Negative Temperature Coefficient
PA	Power Amplifier
Pa	Pascal (for speaker sound pressure measurements)
PBCCH	Packet Broadcast Control CHannel
PC	Personal Computer
PCB	Printed Circuit Board
PCM	Pulse Code Modulation (audio) or Protection Circuit Module (battery)
PDA	Personal Digital Assistant
PFM	Power Frequency Modulation
PSM	Phase Shift Modulation
PWM	Pulse Width Modulation
RAM	Random Access Memory
RF	Radio Frequency
RFI	Radio Frequency Interference
RHCP	Right Hand Circular Polarization
RI	Ring Indicator
RST	ReSeT
RTC	Real Time Clock
RTCM	Radio Technical Commission for Maritime services
RTS	Request To Send
RX	Receive
SCL	Serial CLock
SDA	Serial DAta
SMS	Short Message Service
SPI	Serial Peripheral Interface

Abbreviation	Definition
SPL	Sound Pressure Level
SPK	SPeaKer
SRAM	Static Random Access Memory
TBC	To Be Confirmed
TDMA	Time Division Multiple Access
TP	Test Point
TVS	Transient Voltage Suppressor
TX	Transmit
TYP	TYPical
UART	Universal Asynchronous Receiver-Transmitter
UMTS	Universal Mobile Telecommunications System
USB	Universal Serial Bus
USIM	Universal Subscriber Identification Module
USSD	Unstructured Supplementary Services Data
VSWR	Voltage Standing Wave Ratio

13. Safety Recommendations (for Information Only)

For the efficient and safe operation of your GSM application based on the Q2668 Embedded Module, please read this information carefully.

13.1. RF Safety

13.1.1. General

Your GSM terminal is based on the GSM standard for cellular technology. The GSM standard is spread all over the world. It covers Europe, Asia and some parts of America and Africa. This is the most used telecommunication standard.

Your GSM terminal is actually a low power radio transmitter and receiver. It sends out as well as receives radio frequency energy. When you use your GSM application, the cellular system which handles your calls controls both the radio frequency and the power level of your cellular modem.

13.1.2. Exposure to RF Energy

There has been some public concern on possible health effects of using GSM terminals. Although research on health effects from RF energy has focused on the current RF technology for many years, scientists have begun research regarding newer radio technologies, such as GSM. After existing research had been reviewed, and after compliance to all applicable safety standards had been tested, it has been concluded that the product was fitted for use.

If you are concerned about exposure to RF energy there are things you can do to minimize exposure. Obviously, limiting the duration of your calls will reduce your exposure to RF energy. In addition, you can reduce RF exposure by operating your cellular terminal efficiently by following the guidelines below.

13.1.3. Efficient Terminal Operation

For your GSM terminal to operate at the lowest power level, consistent with satisfactory call quality:

If your terminal has an extendable antenna, extend it fully. Some models allow you to place a call with the antenna retracted. However your GSM terminal operates more efficiently with the antenna when it is fully extended.

Do not hold the antenna when the terminal is "IN USE". Holding the antenna affects call quality and may cause the modem to operate at a higher power level than needed.

13.1.4. Antenna Care and Replacement

Do not use the GSM terminal with a damaged antenna. If a damaged antenna comes into contact with the skin, a minor burn may result. Replace a damaged antenna immediately. You may repair antenna to yourself by following the instructions provided to you. If so, use only a manufacturer-approved antenna. Otherwise, have your antenna repaired by a qualified technician.

Buy or replace the antenna only from the approved suppliers list. Using of unauthorized antennas, modifications or attachments could damage the terminal and may violate local RF emission regulations or invalidate type approval.

13.2. General Safety

13.2.1. Driving

Check the laws and the regulations regarding the use of cellular devices in the area where you have to drive as you always have to comply with them. When using your GSM terminal while driving, please:

- give full attention to driving,
- pull-off from the road and park before making or answering a call if driving conditions so require.

13.2.2. Electronic Devices

Most electronic equipment, for example in hospitals and motor vehicles is shielded from RF energy. However, RF energy may affect some improperly shielded electronic equipment.

13.2.3. Vehicle Electronic Equipment

Check your vehicle manufacturer representative to determine if any on-board electronic equipment is adequately shielded from RF energy.

13.2.4. Medical Electronic Equipment

Consult the manufacturer of any personal medical devices (such as pacemakers, hearing aids, etc) to determine if they are adequately shielded from external RF energy.

Turn your terminal **OFF** in health care facilities when any regulations posted in the area instruct you to do so. Hospitals or health care facilities may be using RF monitoring equipment.

13.2.5. Aircraft

Turn your terminal OFF before boarding any aircraft.

- Use it on the ground only with crew permission.
- Do not use it in the air.

To prevent possible interference with aircraft systems, Federal Aviation Administration (FAA) regulations require you should have prior permission from a crew member to use your terminal while the aircraft is on the ground. In order to prevent interference with cellular systems, local RF regulations prohibit using your modem while airborne.

13.2.6. Children

Do not allow children to play with your GSM terminal. It is not a toy. Children could hurt themselves or others (by poking themselves or others in the eye with the antenna, for example). Children could damage the modem, or make calls that increase your modem bills.

13.2.7. Blasting Areas

To avoid interfering with blasting operations, turn your unit OFF when you are in a "blasting area" or in areas posted: "turn off two-way radio". Construction crew often uses remote control RF devices to set off explosives.

13.2.8. Potentially Explosive Atmospheres

Turn your terminal **OFF** when in any area with a potentially explosive atmosphere. Though it is rare, but your modem or its accessories could generate sparks. Sparks in such areas could cause an explosion or fire resulting in bodily injuries or even death.

Areas with a potentially explosive atmosphere are often, but not always, clearly marked. They include fuelling areas such as petrol stations; below decks on boats; fuel or chemical transfer or storage facilities; and areas where the air contains chemicals or particles, such as grain, dust, or metal powders.

Do not transport or store flammable gas, liquid, or explosives, in the compartment of your vehicle which contains your terminal or accessories.

Before using your terminal in a vehicle powered by liquefied petroleum gas (such as propane or butane) ensure that the vehicle complies with the relevant fire and safety regulations of the country in which the vehicle is used.

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