AirPrime HL7528

Product Technical Specification

SIERRA WIRELESS®

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Document History

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1.1	September 11, 2015	Updated: • Table 2 General Features • Table 5 Pad Definition • Table 7 Current Consumption • Table 32 Ordering Information
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13.0	July 20, 2018	Added **Error! Reference source not found. Error! Reference source not found.**
		Updated Table 5 Pad Definition
14.0	July 30, 2018	Deleted section 6 X-Ray Exposure
15.0	January 30, 2019	Updated 3.15 Debug Interfaces
16.0	June 11, 2019	Updated 3.15.2 JTAG
17.0	May 13, 2021	Added new note under Introduction

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1. Introduction

This document is the Product Technical Specification for the AirPrime HL7528 Embedded Module. It defines the high-level product features and illustrates the interfaces for these features. This document is intended to cover the hardware aspects of the product, including electrical and mechanical.

Note: *Sierra Wireless modules are shipped factory-programmed, with industry or mobile operator approved firmware, according to the specific SKU ordered. Periodically, newer firmware versions become available and can include new features, bug fixes, or critical security updates. Sierra Wireless strongly recommends that customers establish their own production capability for updating module firmware on their assembled end platform, in the event that a newer firmware must be installed before deployment. Sierra Wireless also recommends customers design their products to support post-deployment FOTA upgrades using the AirVantage cloud platform.*

The AirPrime HL7528 belongs to the AirPrime HL Series from Essential Connectivity Module family. These are industrial grade Embedded Wireless Modules that provide data connectivity on wireless networks (as listed in Table 1 Supported Bands/Connectivity).

The HL7528 supports a large variety of interfaces such as USB 2.0, UART and GPIOs to provide customers with the highest level of flexibility in implementing high-end solutions.

Table 1. Supported Bands/Connectivity

RF Band	Transmit Band (Tx)	Receive Band (Rx)	Maximum Output Power
LTE B1	1920 to 1980 MHz	2110 to 2170 MHz	Class 3 (+23 dBm ± 2 dBm)
LTE B3	1710 to 1785 MHz	1805 to 1880 MHz	Class 3 (+23 dBm ± 2 dBm)
LTE B5	824 to 849 MHz	869 to 894 MHz	Class 3 (+23 dBm ± 2 dBm)
LTE B7	2500 to 2570 MHz	2620 to 2690 MHz	Class 3 (+23 dBm ± 2 dBm)

1.1. Common Flexible Form Factor (CF^3)

The AirPrime HL7528 belongs to the Common Flexible Form Factor (CF^3) family of modules. This family consists of a series of WWAN modules that share the same mechanical dimensions (same width and length with varying thicknesses) and footprint. The CF^3 form factor provides a unique solution to a series of problems faced commonly in the WWAN module space as it:

- Accommodates multiple radio technologies (from 2G to LTE advanced) and band groupings
- Supports bit-pipe (Essential Module Series) and value add (Smart Module Series) solutions
- Offers electrical and functional compatibility
- Provides Direct Mount as well as Socketability depending on customer needs

1.2. Physical Dimensions

AirPrime HL7528 modules are compact, robust, fully shielded modules with the following dimensions:

- Length: 23 mm
- Width: 22 mm
- Thickness: 2.5 mm
- Weight: 3.5 g

Note: Dimensions specified above are typical values.

1.3. General Features

The table below summarizes the AirPrime HL7528 features.

Table 2. General Features

Feature	Description
Physical	• Small form factor (146-pad solderable LGA pad) – 23mm x 22mm x 2.5mm (nominal) • Complete body shielding • RF connection pads (RF main interface) • Baseband signals connection
Electrical	Single or double supply voltage (VBATT and VBATT_PA) – 3.2V – 4.5V
RF	Quad-band LTE: • LTE B1: 2100 MHz • LTE B3: 1800 MHz • LTE B5: 850 MHz • LTE B7: 2600 MHz
SIM interface	• 1.8V/3V support • SIM extraction / hot plug detection • SIM/USIM support • Conforms with ETSI UICC Specifications • Supports SIM application tool kit with proactive SIM commands
Application interface	• Multiple non-multiplexed USB channel support • Dial-up networking • USB selective suspend to maximize power savings • AT command interface – 3GPP 27.007 standard, plus proprietary extended AT commands
Protocol Stack	Single mode LTE operation: • LTE FDD, bandwidth 1.4-20 MHz • System Release: 3GPP Rel. 9 • Category 4 (up to 150 MBit/s in downlink, 50 MBit/s in uplink) • MIMO 2x2 • Max modulation 64 QAM DL, 16 QAM UL • Intra-frequency and inter-frequency mobility
SMS	• SMS over SGs • SMS MO and MT • SMS Status Report • SMS storing rules (support of AT+CNMI)
Connectivity	• Multiple (up to 20) cellular packet data profiles • Sleep mode for minimum idle power draw • Mobile-originated PDP context activation / deactivation • Static and Dynamic IP address. The network may assign a fixed IP address or dynamically assign one using DHCP (Dynamic Host Configuration Protocol). • Supports PAP and CHAP authentication protocols • PDP context type (IPv4, IPv6, IPv4v6). IP Packet Data Protocol context • RFC1144 TCP/IP header compression

Feature	Description
Environmental	Operating temperature ranges (industrial grade): • Class A: -30°C to +70°C • Class B: -40°C to +85°C
RTC	Real Time Clock (RTC) with calendar

1.4. Architecture

The figure below presents an overview of the AirPrime HL7528's internal architecture and external interfaces.

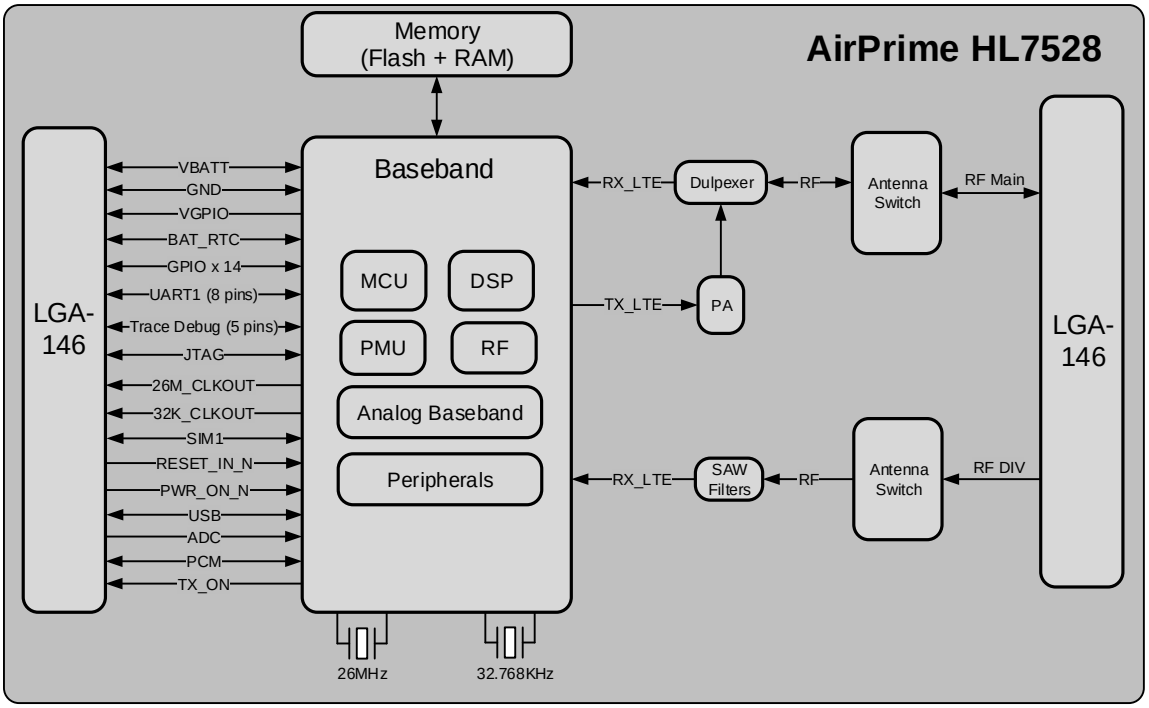

Figure 1. Architecture Overview

1.5. Interfaces

The AirPrime HL7528 module provides the following interfaces and peripheral connectivity:

- 1x – 8-wire UART
- 1x – Active Low RESET
- 1x – USB 2.0
- 1x – Backup Battery Interface
- 2x – System Clock Out
- 1x – Active Low POWER ON
- 1x – 1.8V/3V SIM
- 1x – JTAG Interface
- 14x – GPIOs (3 of which have multiplexes)

- 1x – Main Antenna
- 1x – RX Diversity Antenna
- 1x – VGPIO
- 1x – TX ON
- 1x – ADC
- 1x – PCM

1.6. Connection Interface

The AirPrime HL7528 module is an LGA form factor device. All electrical and mechanical connections are made through the 146 Land Grid Array (LGA) pads on the bottom side of the PCB.

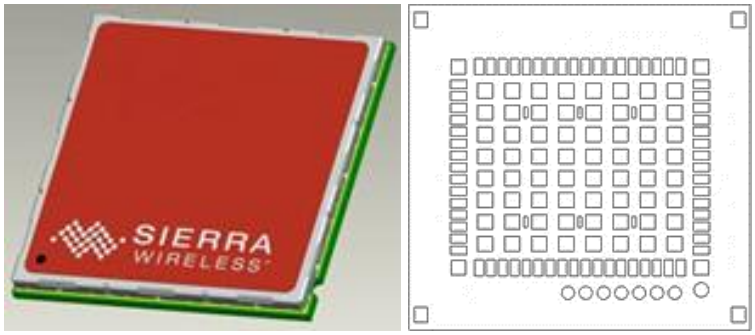

Figure 2. Mechanical Overview

The 146 pads have the following distribution:

- 66 inner signal pads, 1x0.5mm, pitch 0.8mm
- 1 reserved test point (do not connect), 1.0mm diameter
- 7 test point (JTAG), 0.8mm diameter, 1.20mm pitch
- 64 inner ground pads, 1.0x1.0mm, pitch 1.825mm/1.475mm
- 4 inner corner ground pads, 1x1mm
- 4 outer corner ground pads, 1x0.9mm

1.7. ESD

Refer to the following table for ESD Specifications.

Table 3. ESD Specifications

Category	Connection	Specification
Operational	RF ports	IEC-61000-4-2 — Level (Electrostatic Discharge Immunity Test)
Non-operational	Host connector interface	Unless otherwise specified: • JESD22-A114 ± 2kV Human Body Model • JESD22-A115 ± 200V Machine Model • JESD22-C101C ± 500V Charged Device Model
Signals	SIM connector	

Category	Connection	Specification
	Other host signals	Adding ESD protection is highly recommended at the point where the USIM contacts are exposed, and for any other signals that would be subjected to ESD by the user.

1.8. Environmental and Certifications

1.8.1. Environmental Specifications

The environmental specification for both operating and storage conditions are defined in the table below.

Table 4. Environmental Specifications

Conditions	Range
Operating Class A	-30°C to +70°C
Operating Class B	-40°C to +85°C
Storage	-40°C to +85°C

Class A is defined as the operating temperature ranges that the device:

- Shall exhibit normal function during and after environmental exposure.
- Shall meet the minimum requirements of 3GPP or appropriate wireless standards.

Class B is defined as the operating temperature ranges that the device:

- Shall remain fully functional during and after environmental exposure
- Shall exhibit the ability to establish an SMS or DATA call (emergency call) at all times even when one or more environmental constraint exceeds the specified tolerance.
- Unless otherwise stated, full performance should return to normal after the excessive constraint(s) have been removed.

1.8.2. RoHS Directive Compliance

AirPrime HL7528 modules are compliant with RoHS Directive 2011/65/EU, including directive 2015/863 amending annex II, which sets limits for the use of certain restricted hazardous substances. This directive states that electrical and electronic equipment put on the market does not contain lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB), polybrominated diphenyl ethers (PBDE), Bis (2-ethylhexyl) phthalate (DEHP), Butyl benzyl phthalate (BBP), Dibutyl phthalate (DBP) or Diisobutyl phthalate (DIBP) above threshold limits.

1.8.3. Disposing of the Product

This electronic product is subject to the EU Directive 2012/19/EU for Waste Electrical and Electronic Equipment (WEEE). As such, this product must not be disposed of at a municipal waste collection point. Please refer to local regulations for directions on how to dispose of this product in an environmentally friendly manner.

1.9. References

[1] AirPrime HL Series Customer Process Guidelines
Reference Number: 4114330

[2] AirPrime HL7528 AT Commands Interface Guide
Reference Number: 4116843

2. Pad Definition

AirPrime HL7528 pads are divided into 2 functional categories.

- Core functions and associated pads cover all the mandatory features for M2M connectivity and will be available by default across all CF^3 family of modules. These Core functions are always available and always at the same physical pad locations. A customer platform using only these functions and associated pads is guaranteed to be forward and/or backward compatible with the next generation of CF^3 modules.
- Extension functions and associated pads bring additional capabilities to the customer. Whenever an Extension function is available on a module, it is always at the same pad location.

Other pads marked as “not connected” or “reserved” should not be used.

Table 5. Pad Definition

Pad #	Signal Name	Function	I/O	Active Low/High	Reset State*	Power Supply Domain	Recommendation for Unused Pads	Type
1	GPIO1	General purpose input/output	I/O		T	1.8V	Left Open	Extension
2	UART1_RI / TRACE_DATA3	UART1 Ring indicator / Trace data 3	O		L	1.8V	Connect to test point	Core
3	UART1_RTS	UART1 Request to send	I	L	T/PU	1.8V	Connect to test point	Core
4	UART1_CTS	UART1 Clear to send	O	L	T/PU	1.8V	Connect to test point	Core
5	UART1_TX	UART1 Transmit data	I		T/PD	1.8V	Connect to test point	Core
6	UART1_RX	UART1 Receive data	O		T/PU	1.8V	Connect to test point	Core
7	UART1_DTR	UART1 Data terminal ready	I	L	T/PD	1.8V	Connect to test point	Core
8	UART1_DCD / TRACE_DATA1	UART1 Data carrier detect / Trace data 1	O	L	L	1.8V	Connect to test point	Core
9	UART1_DSR / TRACE_DATA0	UART1 Data set ready / Trace data 0	O	L	H	1.8V	Connect to test point	Core

Pad #	Signal Name	Function	I/O	Active Low/High	Reset State*	Power Supply Domain	Recommendation for Unused Pads	Type
10	GPIO2 / TRACE_DATA2	General purpose input/output / Trace data 2	I/O		L	1.8V	Connect to test point	Core
11	RESET_IN_N	Input reset signal	I	L	N/A	1.8V	Left Open	Core
12	USB_D-	USB Data Negative (Low / Full Speed)	I/O		T	3.3V	Connect to test point	Extension
		USB Data Negative (High Speed)				0.38V		
13	USB_D+	USB Data Positive (Low / Full Speed)	I/O		T	3.3V	Connect to test point	Extension
		USB Data Positive (High Speed)				0.38V		
14	NC	Not Connected						Not connected
15	NC	Not Connected						Not connected
16	USB_VBUS	USB VBUS	I		N/A	3.3V – 5.5V	Connect to test point	Extension
17	NC	Not Connected (Reserved for future use)					Left Open	Not connected
18	NC	Not Connected (Reserved for future use)					Left Open	Not connected
19	NC	Not Connected (Reserved for future use)					Left Open	Not connected
20	NC	Not Connected (Reserved for future use)					Left Open	Not connected
21	BAT_RTC	Power supply for RTC backup	I/O		N/A	1.8V	Left Open	Extension
22	26M_CLKOUT	26MHz System Clock Output	O		T/PD	1.8V	Left Open	Extension
23	32K_CLKOUT	32.768kHz System Clock Output	O		T/PD	1.8V	Left Open	Extension
24	ADC1	Analog to digital converter	I		N/A	1.2V	Left Open	Extension
25	NC	Not Connected (Reserved for future use)					Left Open	Not connected
26	UIM1_VCC	1.8V/3V SIM1 Power supply	O		N/A	1.8V/3V	Mandatory connection	Core
27	UIM1_CLK	1.8V/3V SIM1 Clock	O		L	1.8V/3V	Mandatory connection	Core
28	UIM1_DATA	1.8V/3V SIM1 Data	I/O		L	1.8V/3V	Mandatory connection	Core
29	UIM1_RESET	1.8V/3V SIM1 Reset	O	L	L	1.8V/3V	Mandatory connection	Core
30	GND	Ground	0V		N/A	0V	Mandatory connection	Extension
31	RF_DIV	RF Input - Diversity			N/A		Mandatory connection	Extension

Pad #	Signal Name	Function	I/O	Active Low/High	Reset State*	Power Supply Domain	Recommendation for Unused Pads	Type
32	GND	Ground	0V		N/A	0V	Mandatory connection	Extension
33	PCM_OUT	PCM data out	O		T/PD	1.8V	Left Open	Extension
34	PCM_IN	PCM data in	I		T/PD	1.8V	Left Open	Extension
35	PCM_SYNC	PCM sync out	I/O		T/PD	1.8V	Left Open	Extension
36	PCM_CLK	PCM clock	I/O		T/PD	1.8V	Left Open	Extension
37	GND	Ground	0V		N/A	0V	Mandatory connection	Core
38	NC	Not Connected (Reserved for future use)					Left Open	Not connected
39	GND	Ground	0V		N/A	0V	Mandatory connection	Core
40	GPIO7	General purpose input/output	I/O		T/PD	1.8V	Left Open	Core
41	GPIO8 / MIPI2_TRACE_CLK	General purpose input/output / Trace clock	I/O		L	1.8V	Connect to test point	Core
42	NC	Not Connected (Reserved for future use)					Left Open	Not connected
43	NC	Not Connected (Reserved for future use)					Left Open	Not connected
44	GPIO13	General purpose input/output	O		T/PU	1.8V	Left Open	Extension
45	VGPIO	GPIO voltage output	O		N/A	1.8V	Left Open	Core
46	GPIO6	General purpose input/output	I/O		T/PD	1.8V	Left Open	Core
47	NC	Not Connected (Reserved for future use)					Left Open	Not connected
48	GND	Ground	0V		N/A	0V	Mandatory connection	Core
49	RF_MAIN	RF Input/output			N/A		Mandatory connection	Core
50	GND	Ground	0V		N/A	0V	Mandatory connection	Core
51	GPIO14	General purpose input/output	I		T/PU	1.8V	Left Open	Extension
52	GPIO10	General purpose input/output	I/O		T/PD	1.8V	Left Open	Extension
53	GPIO11	General purpose input/output	I/O		T/PD	1.8V	Left Open	Extension
54	GPIO15	General purpose input/output	I/O		T/PU	1.8V	Left Open	Extension

Pad #	Signal Name	Function	I/O	Active Low/High	Reset State*	Power Supply Domain	Recommendation for Unused Pads	Type
55	NC	Not Connected					Left Open	Not connected
56	NC	Not Connected					Left Open	Not connected
57	NC	Not Connected					Left Open	Not connected
58	GPIO12	General purpose input/output	I/O		L	1.8V	Left Open	Extension
59	PWR_ON_N	Active Low Power On control signal	I	L	N/A	1.8V	Mandatory connection	Core
60	TX_ON	TX indicator	O			2.3V	Left Open	Core
61	VBATT_PA	Power supply (refer to section 3.1 Power Supply for more information)	I		N/A	3.2V (min) 3.7V (typ) 4.5V (max)	Mandatory connection	Core
62	VBATT_PA	Power supply (refer to section 3.1 Power Supply for more information)	I		N/A	3.2V (min) 3.7V (typ) 4.5V (max)	Mandatory connection	Core
63	VBATT	Power supply	I		N/A	3.2V (min) 3.7V (typ) 4.5V (max)	Mandatory connection	Core
64	UIM1_DET / GPIO3	UIM1 Detection / General purpose input/output	I/O	H	T/PD	1.8V	Left Open	Core
65	GPIO4	General purpose input/output	I/O	H	T/PD	1.8V	Left Open	Extension
66	GPIO5	General purpose input/output	I/O		T	1.8V	Left Open	Extension
67-70	GND	Ground	GND		N/A	0V		Core
71 - 166	*Note: These pads are not available on the AirPrime HL7528 module.*							
167 - 234	GND	Ground	GND		N/A	0V		Core
236	JTAG_RESET	JTAG RESET	I	L	N/A	1.8V	Left Open	Extension
237	JTAG_TCK	JTAG Test Clock	I		PD	1.8V	Left Open	Extension
238	JTAG_TDO	JTAG Test Data Output	O		T	1.8V	Left Open	Extension

Pad #	Signal Name	Function	I/O	Active Low/High	Reset State*	Power Supply Domain	Recommendation for Unused Pads	Type
239	JTAG_TMS	JTAG Test Mode Select	I		PU	1.8V	Left Open	Extension
240	JTAG_TRST	JTAG Test Reset	I	L	PD	1.8V	Left Open	Extension
241	JTAG_TDI	JTAG Test Data Input	I		PU	1.8V	Left Open	Extension
242	JTAG_RTCK	JTAG Returned Test Clock	O		PD	1.8V	Left Open	Extension

* PU = Pull up, PD = Pull down, H = High, L = Low, T = High impedance, N/A = Not applicable.

2.1. Pad Configuration (Top View, Through Module)

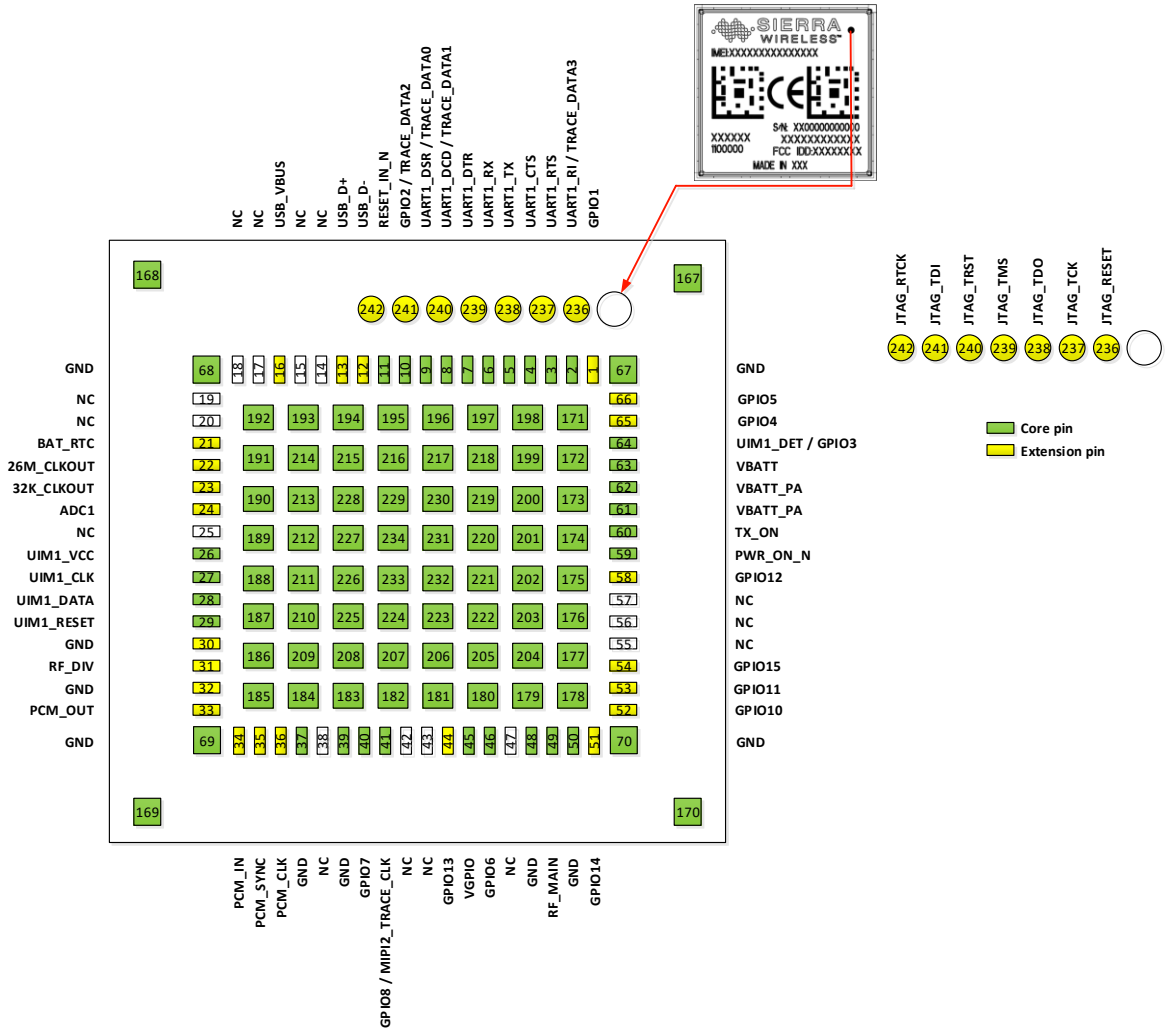

Figure 3. Pad Configuration

3. Detailed Interface Specifications

Note: If not specified, all electrical values are given for VBATT=3.7V and an operating temperature of 25°C.

For standard applications, VBATT and VBATT_PA must be tied externally to the same power supply. For some specific applications, AirPrime HL7528 module supports separate VBATT and VBATT_PA connection if requirements below are fulfilled.

3.1. Power Supply

The AirPrime HL7528 module is supplied through the VBATT signal with the following characteristics.

Table 6. Power Supply

Supply	Minimum	Typical	Maximum
VBATT voltage (V)	3.2*	3.7	4.5
VBATT_PA voltage (V) Full Specification	3.2*	3.7	4.5

* This value should be guaranteed during the burst.

Note: Load capacitance for VBATT is around 32µF ± 20% embedded inside the module.
Load capacitance for VBATT_PA is around 10µF ± 20% embedded inside the module.

3.2. Current Consumption

The following table lists the current consumption of the AirPrime HL7528 at different conditions.

Table 7. Current Consumption

Parameter		Minimum	Typical	Maximum	Unit
Off mode		95.0	110	202.0	µA
Sleep mode – LTE DRX = 1.28s USB = suspended	Band 1	1.2	1.4	6.2	mA
	Band 3	1.2	1.4	6.2	mA
	Band 5	1.2	1.4	6.2	mA
	Band 7	1.2	1.4	6.2	mA
LTE in communication mode (TX Max)	Band 1	596.0	610.0	633.0	mA
	Band 3	541.0	562.0	586.0	mA
	Band 5	632.0	678.0	749.0	mA
	Band 7	636.0	665.0	709.0	mA

3.3. VGPIO

The VGPIO output can be used to:

- Pull-up signals such as I/Os
- Supply the digital transistors driving LEDs

The VGPIO output is available when the AirPrime HL7528 module is switched ON.

Table 8. VGPIO Electrical Characteristics

Parameter	Minimum	Typical	Maximum	Remarks
Voltage level (V)	1.7	1.8	1.9	Both active mode and sleep mode
Current capability (mA)	-	-	50	
Rise Time (ms)	-	-	1.5	Start-Up time from 0V

3.4. BAT_RTC

The AirPrime HL7528 module provides an input/output to connect a Real Time Clock power supply.

This pad is used as a back-up power supply for the internal Real Time Clock. The RTC is supported when VBATT is available but a back-up power supply is needed to save date and hour when VBATT is switched off.

If VBATT is available, the back-up battery can be charged by the internal 1.8V power supply regulator.

Table 9. BAT_RTC Electrical Characteristics

Parameter	Minimum	Typical	Maximum	Unit
Input voltage	-	1.8	-	V
Input current consumption	-	2.5	-	µA
Output voltage	-5%	1.8	+5%	V
Maximum charging current (@VBATT=3.7V)	-	25	-	mA

3.5. SIM Interface

The AirPrime HL7528 has one physical SIM interface, UIM1.

UIM1 allows control of a 1.8V/3V SIM and are fully compliant with GSM 11.11 recommendations concerning SIM functions.

The five signals used by UIM1 are as follows:

- UIM1_VCC: power supply
- UIM1_CLK: clock
- UIM1_DATA: I/O port
- UIM1_RESET: reset
- UIM1_DET: SIM detection

Table 10. UIM1 Pad Description

Pad #	Signal Name	Description	Multiplex
26	UIM1_VCC	1.8V/3V SIM1 Power supply	
27	UIM1_CLK	1.8V/3V SIM1 Clock	
28	UIM1_DATA	1.8V/3V SIM1 Data	
29	UIM1_RESET	1.8V/3V SIM1 Reset	
64	UIM1_DET	UIM1 Detection	GPIO3

Table 11. Electrical Characteristics of UIM1

Parameter	Minimum	Typical	Maximum	Remarks
UIM1 Interface Voltage (V) (VCC, CLK, IO, RST)	-	2.9	-	The appropriate output voltage is auto detected and selected by software.
	-	1.80	-	
UIM1 Detect	-	1.80	-	High active
UIM1_VCC Current (mA)	-	-	10	Maximum output current in sleep mode = 3 mA
UIM1_VCC Line Regulation (mV/V)	-	-	50	At Iout_Max
UIM1_VCC Power-up Setting Time (µs) from power down	-	10	-	

3.5.1. UIM1_DET

UIM1_DET is used to detect and notify the application about the insertion and removal of a SIM device in the SIM socket connected to the SIM interface. When a SIM is inserted, the state of UIM1_DET transitions from logic 0 to logic 1. Inversely, when a SIM is removed, the state of UIM1_DET transitions from logic 1 to logic 0.

Enabling or disabling either SIM detect feature can be done using the **AT+KSIMDET** command. For more information about this command, refer to document [2] AirPrime HL7528 AT Commands Interface Guide.

3.6. USB

The AirPrime HL7528 has one USB interface.

Table 12. USB Pad Description

Pad Number	Signal Name	I/O	Function
12	USB_D-	I/O	USB Data Negative
13	USB_D+	I/O	USB Data Positive
16	USB_VBUS	I	USB VBUS

Note: When a USB supply is not available, connect USB_VBUS to VBATT to supply the USB interface. USB_VBUS will have a voltage range of 3.3V to 4.5V when connected to VBATT.

3.7. Electrical Information for Digital I/O

The table below enumerates the electrical characteristics of the following digital interfaces:

- UART
- GPIOs
- JTAG
- RESET

Table 13. Digital I/O Electrical Characteristics

Parameter	Symbol	Minimum	Maximum
Input Current-High (µA)	I_{IH}	-	-240
Input Current-Low (µA)	I_{IL}	-	240
DC Output Current-High (mA)	I_{OH}	-	6
DC Output Current-Low (mA)	I_{OL}	-6	-
Input Voltage-High (V)	V_{IH}	1.33	1.90
Input Voltage-Low (V)	V_{IL}	-0.20	0.34
Output Voltage-High (V)	V_{OH}	1.45	-
Output Voltage-Low (V)	V_{OL}	-	0.35

3.8. General Purpose Input/Output (GPIO)

The AirPrime HL7528 module provides 14 GPIOs, 3 of which have multiplexes.

Table 14. GPIO Pad Description

Pad Number	Signal Name	Multiplex	I/O	Power Supply Domain
1	GPIO1		I/O	1.8V
10	GPIO2	TRACE_DATA2	I/O	1.8V
40	GPIO7		I/O	1.8V
41	GPIO8	MIPI2_TRACE_CLK	I/O	1.8V
44	GPIO13		I/O	1.8V
46	GPIO6		I/O	1.8V
51	GPIO14		I/O	1.8V
52	GPIO10		I/O	1.8V
53	GPIO11		I/O	1.8V
54	GPIO15		I/O	1.8V
58	GPIO12		I/O	1.8V
64	GPIO3	UIM1_DET	I/O	1.8V
65	GPIO4		I/O	1.8V
66	GPIO5		I/O	1.8V

3.9. Main Serial Link (UART1)

The main serial link (UART1) is used for communication between the AirPrime HL7528 module and a PC or host processor. It consists of a flexible 8-wire serial interface that complies with RS-232 interface.

The supported baud rates of the UART1 are 300, 1200, 2400, 4800, 9600, 19200, 38400, 57600, 115200, 230400, 460800, 500000, 750000, 921600, 1843200, 3000000 and 3250000 bit/s.

The signals used by UART1 are as follows:

- TX data (UART1_TX)
- RX data (UART1_RX)
- Request To Send (UART1_RTS)
- Clear To Send (UART1_CTS)
- Data Terminal Ready (UART1_DTR)
- Data Set Ready (UART1_DSR)
- Data Carrier Detect (UART1_DCD)
- Ring Indicator (UART1_RI)

Note: Signal names are according to PC view.

UART1 pad description is summarized in the table below.

Table 15. UART1 Pad Description

Pad #	Signal Name*	I/O*	Description
2	UART1_RI	O	Signal incoming calls (data only), SMS, etc.
3	UART1_RTS	I	Request to send
4	UART1_CTS	O	AirPrime HL7528 is ready to receive AT commands
5	UART1_TX	I	Transmit data
6	UART1_RX	O	Receive data
7	UART1_DTR	I (active low)	Prevents the AirPrime HL7528 from entering sleep mode, switches between data mode and command mode, and wakes the module up.
8	UART1_DCD	O	Signal data connection in progress
9	UART1_DSR	O	Signal UART interface is ON

* According to PC view.

Note: UART1 input signal pins (UART1_RTS, UART1_TX and UART1_DTR) are internally pulled up by an 8kΩ resistor when the module is ON.

3.10. POWER-ON Signal (PWR_ON_N)

A low-level signal must be provided to switch the AirPrime HL7528 module ON.

It is internally connected to the permanent 1.8V supply regulator inside the HL7528 via a pull-up resistor. Once VBAT is supplied to the HL7528 module, this 1.8V supply regulator will be enabled and so the PWR_ON_N signal is by default at high level.

The PWR_ON_N signal's characteristics are listed in the table below.

Table 16. PWR_ON_N Electrical Characteristics

Parameter	Minimum	Typical	Maximum
Input Voltage-Low (V)		-	0.51
Input Voltage-High (V)	1.33	-	2.2
Power-up period (ms) from PWR_ON_N falling edge	2000	-	-
PWR_ON_N assertion time (ms)	25		

Note: As PWR_ON_N is internally pulled up with 100kΩ, an open collector or open drain transistor must be used for ignition.

VGPIO is an output from the module that can be used to check if the module is active.

- When VGPIO = 0V, the module is OFF
- When VGPIO = 1.8V, the module is ON (it can be in idle, communication or sleep mode)

*Note: PWR_ON_N signal cannot be used to power the module off. To power the module off, use AT command **AT+CFUN=0**.*

3.11. Reset Signal (RESET_IN_N)

To reset the module, a low-level pulse must be sent on the RESET_IN_N pad for 20ms. This action will immediately restart the AirPrime HL7528 module with the PWR_ON_N signal at low level. (If the PWR_ON_N signal is at high level, the module will be powered off.) As RESET_IN_N is internally pulled up, an open collector or open drain transistor should be used to control this signal.

The RESET_IN_N signal will reset the registers of the CPU and reset the RAM memory as well, for the next power on.

Note: As RESET_IN_N is referenced to the VRTC (200kΩ pull-up resistor to VRTC 1.8V) an open collector or open drain transistor should be used to control this signal.

Table 17. RESET_IN_N Electrical Characteristics

Parameter	Minimum	Typical	Maximum
Input Voltage-Low (V)		-	0.51
Input Voltage-High (V)	1.33	-	2.2
Reset assertion time (ms)	20	-	-
Power-up period (ms) from RESET_IN_N falling edge*	2000	-	-

* With the PWR_ON_N Signal at low level

3.12. Analog to Digital Converter (ADC1)

One Analog to Digital Converter input, ADC1, is provided by the AirPrime HL7528 module. This converter is a 10-bit resolution ADC ranging from 0 to 1.2V.

The following table describes the pad description of the ADC interface.

Table 18. ADC Interface Pad Description

Pad Number	Signal Name	I/O	Description
24	ADC1	I	Analog to digital converter

Typical ADC1 use is for monitoring external voltage; such as in an application to safely power OFF an external supply in case of overvoltage.

ADC1's electrical characteristics are listed in the table below.

Table 19. ADC Electrical Characteristics

Parameter	Minimum	Typical	Maximum	Remarks
ADC1 Resolution (bits)	-	10	-	
Input Voltage Range (V)	0	-	1.2	General purpose input
Update rate per channel (kHz)	-	-	125	
Integral Nonlinearity (bits)	-	-	± 2	LSB
Offset Error (bits)	-	-	± 1	LSB
Gain	849	853	858	
Input Resistance (MΩ)	1	-	-	
Input Capacitance (pF)	-	1	-	

3.13. Clock Interface

The AirPrime HL7528 module supports two digital clock interfaces.

The following table describes the pad description of the clock out interfaces.

Table 20. Clock Interface Pad Description

Pad Number	Signal Name	I/O	I/O Type	Description
22	26M_CLKOUT	O	1.8V	26MHz Digital Clock output
23	32K_CLKOUT	O	1.8V	32.768kHz Digital Clock output

Enabling or disabling the clock out feature can be done using AT commands. For more information about AT commands, refer to document [2] AirPrime HL7528 AT Commands Interface Guide.

3.14. PCM

The Digital Audio (PCM) Interface allows connectivity with standard audio peripherals. It can be used, for example, to connect an external audio codec.

The programmability of this interface allows addressing a large range of audio peripherals.

The signals used by the Digital Audio Interface are as follows:

- PCM_SYNC: The frame synchronization signal delivers an 8 kHz frequency pulse that synchronizes the frame data in and the frame data out.
- PCM_CLK: The frame bit clock signal controls data transfer with the audio peripheral.
- PCM_OUT: The frame “data out” relies on the selected configuration mode.
- PCM_IN: The frame “data in” relies on the selected configuration mode.

The following table describes the pad description of the PCM interface.

Table 21. PCM Interface Pad Description

Pad Number	Signal Name	I/O	Description
33	PCM_OUT	O	PCM data out
34	PCM_IN	I	PCM data in
35	PCM_SYNC	I/O	PCM sync out
36	PCM_CLK	I/O	PCM clock

Refer to the following table for the electrical characteristics of the digital audio interface in master mode.

Table 22. PCM Master Mode Parameters

Signal	Symbol	Minimum	Typical	Maximum	Unit
PCM_CLK period	t_1	T - 4	T	-	ns
PCM_CLK low time	t_2	T/2 - 20	T/2	-	ns
PCM_CLK high time	t_3	T/2 - 20	T/2	-	ns
PCM_SYNC high begin after PCM_CLK high begin	t_4	-24	-	2 x t_{cp} + 12	ns
PCM_SYNC high end after PCM_CLK low end	t_5	-24	-	2 x t_{cp} + 12	ns
PCM_OUT invalid before PCM_CLK low end	t_6	-	-	24	ns
PCM_OUT valid after PCM_CLK high begin	t_7	-	-	t_{cp} + 12	ns
PCM_IN setup time before PCM_CLK high end	t_8	t_{cp} + 50	-	-	ns
PCM_IN hold time after PCM_CLK low begin	t_9	12	-	-	ns

T = corresponds to the audio sampling rate (48KHz, 44.1KHz, 32KHz, 24KHz, 22.05KHz, 16KHz, 12KHz, 11.025KHz and 8KHz) and to the frame rate length (17 bit, 18 bit, 32 bit, 48 bit or 64 bit).

t_{CP} = 9.6ns (clock period test condition)

The following figure shows the PCM timing waveform.

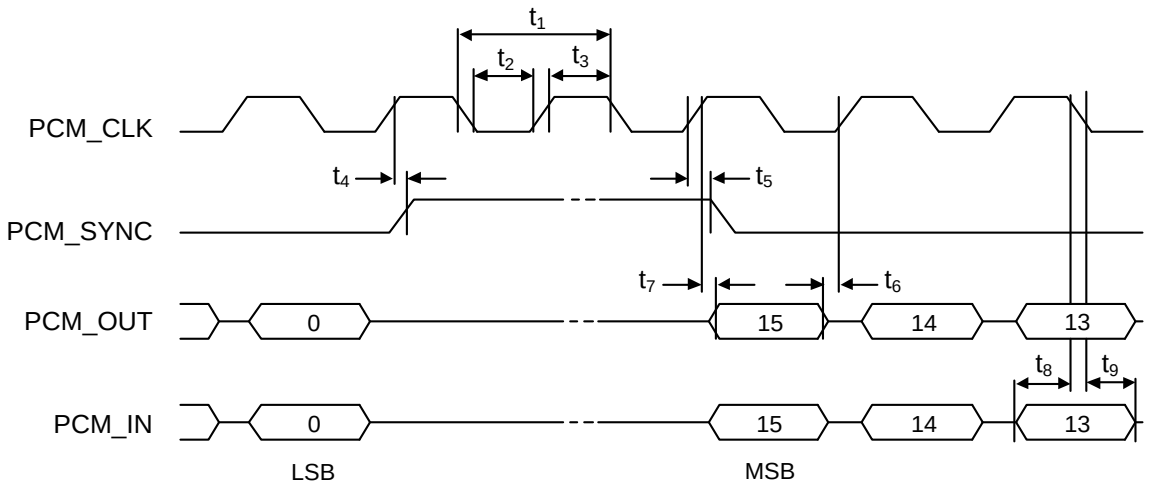

Figure 4. PCM Master Mode Timing Waveform

Refer to the following table for the electrical characteristics of the digital audio interface in slave mode.

Table 23. PCM Slave Mode Parameters

Signal	Symbol	Minimum	Typical	Maximum	Unit
PCM_CLK period	t_1	T	--	--	ns
PCM_CLK low time	t_2	120	--	--	ns
PCM_CLK high time	t_3	120	--	--	ns
PCM_SYNC high begins before PCM_CLK low begin (latching edge of PCM_CLK)	t_4	2 x t_{cp} + 17	---	---	ns
PCM_SYNC low begins before PCM_CLK low begin (latching edge of PCM_CLK)	t_5	2 x t_{cp} + 17	---	---	ns
PCM_OUT invalid before PCM_CLK rising edge (shifting edge of PCM_CLK)	t_6	---	---	12	ns
PCM_OUT valid after PCM_CLK rising edge (shifting edge of PCM_CLK)	t_7	---	---	3 x t_{cp} + 50	ns
PCM_IN setup time before PCM_CLK falling edge	t_8	t_{cp} + 12	---	---	ns
PCM_IN hold time after PCM_CLK falling edge	t_9	24	---	---	ns

T = corresponds to the audio sampling rate (48KHz, 44.1KHz, 32KHz, 24KHz, 22.05KHz, 16KHz, 12KHz, 11.025KHz and 8KHz) and to the frame rate length (17 bit, 18 bit, 32 bit, 48 bit or 64 bit).

t_{CP} = 9.6ns (clock period test condition)

The following figure shows the PCM slave mode timing waveform.

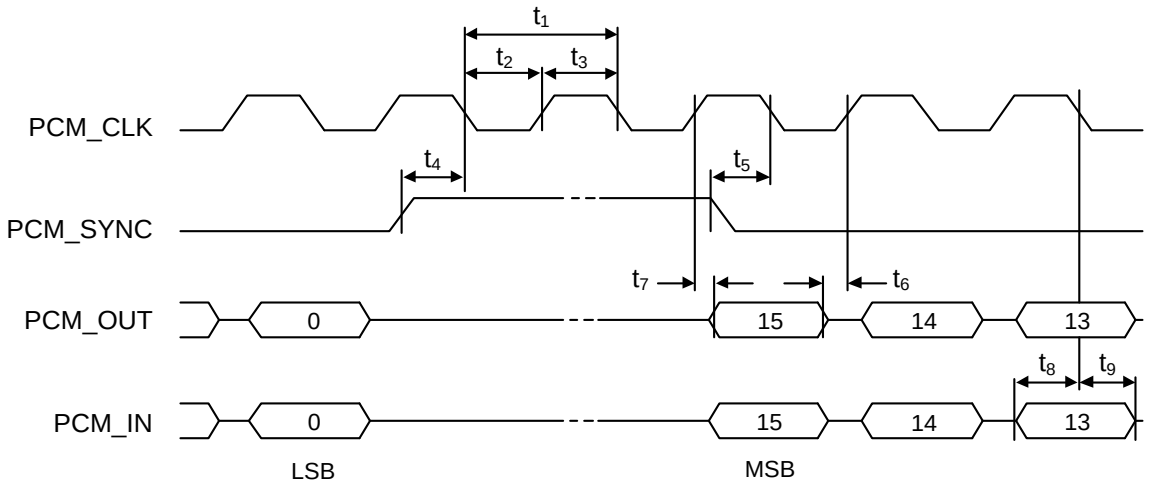

Figure 5. PCM Slave Mode Timing Waveform

3.15. Debug Interfaces

The AirPrime HL7528 module provides 3 interfaces for a powerful debug system.

3.15.1. USB

The USB interface is the primary debug interface for customers to collect traces.

Table 24. USB Pad Description

Pad Number	Signal Name	I/O	Function
12	USB_D-	I/O	USB Data Negative
13	USB_D+	I/O	USB Data Positive
16	USB_VBUS	I	USB VBUS

Note: It is strongly recommended to reserve test points to collect traces in case USB is not used.

3.15.2. JTAG

Note: This interface is reserved for Sierra Wireless' internal debug use (for customer support).

The JTAG interface provides debug access to the core of the HL7528. These JTAG signals are accessible through solder-able test points.

Table 25. JTAG Pad Description

Pad Number	Signal Name	Function
236	JTAG_RESET	JTAG RESET
237	JTAG_TCK	JTAG Test Clock
238	JTAG_TDO	JTAG Test Data Output
239	JTAG_TMS	JTAG Test Mode Select

Pad Number	Signal Name	Function
240	JTAG_TRST	JTAG Test Reset
241	JTAG_TDI	JTAG Test Data Input
242	JTAG_RTCK	JTAG Returned Test Clock

Note: It is recommended to provide access through Test Points to this interface (for Failure Analysis debugging). All signals listed in the table above should be outputs on the customer board to allow JTAG debugging.

3.15.3. Trace Debug

In addition to the USB and JTAG interfaces, the AirPrime HL7528 module provides a Trace Debug interface, providing real-time instruction and data trace of the modem core.

Table 26. Trace Debug Pad Description

Pad Number	Signal Name	Function	Multiplex
2	TRACE_DATA3	Trace data 3	
8	TRACE_DATA1	Trace data 1	
9	TRACE_DATA0	Trace data 0	
10	TRACE_DATA2	Trace data 2	GPIO2
41	MIPI2_TRACE_CLK	Trace clock	GPIO8

Note: It is strongly recommended to provide access to this interface through Test Points for Sierra Wireless' internal debug use (for customer support). Access to the USB debug interface described in section 3.15.1 USB should also always be provided when using this interface.

3.16. RF Interface

The RF interface of the HL7528 module allows the transmission of RF signals. This interface has a 50Ω nominal impedance.

Contact Sierra Wireless technical support for assistance in integrating the AirPrime HL7528 on applications with embedded antennas.

3.16.1. RF Connection

A 50Ω stripline can be used to connect to standard RF connectors such as SMA, UFL, etc. for antenna connection.

Table 27. RF Main Connection

Pad Number	RF Signal	Impedance	VSWR Rx (max)	VSWR Tx (max)
49	RF_MAIN	50Ω	1.5:1	1.5:1

Table 28. RF Diversity Connection

Pad Number	RF Signal	Impedance	VSWR Rx (max)	VSWR Tx (max)
31	RF_DIV	50Ω	1.5:1	---

3.16.2. RF Performances

RF performances are compliant with 3GPP recommendation TS 36.101.

Table 29. Conducted RX Sensitivity (dBm)

Frequency Band		Primary (Typical)	Secondary (Typical)	SIMO (Typical)
LTE B1	Full RB; BW: 20 MHz*	-94.0	-96.0	-97.5
LTE B3	Full RB; BW: 20 MHz*	-93.5	-95.0	-96.5
LTE B5	Full RB; BW: 10 MHz*	-98.0	-98.5	-100.5
LTE B7	Full RB; BW: 20 MHz*	-93.0	-94.0	-96.0

* Sensitivity values scale with bandwidth: x_MHz_Sensitivity = 10 MHz_Sensitivity – 10*log (10 MHz/x_MHz)

3.16.3. TX_ON Indicator (TX_ON)

The AirPrime HL7528 module provides a signal, TX_ON, for TX indication. The TX_ON is a 2.3V signal and its status signal depends on the module transmitter state.

Refer to the following table for the status of the TX_ON signal depending on the embedded module's state.

Table 30. TX_ON Pad Description

Pad #	Signal Name	Function	I/O Type	Power Supply Domain
60	TX_ON	TX indicator	O	2.3V

Table 31. TX_ON Characteristics

Parameter	Minimum	Typical	Maximum
$T_{advance}$	30µs		
T_{delay}		10µs	

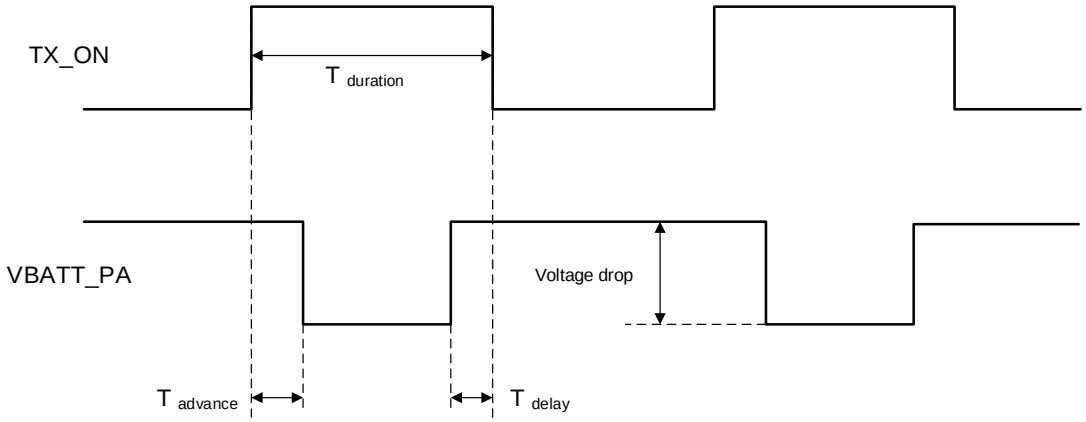

Figure 6. TX_ON State during Transmission

4. Mechanical Drawings

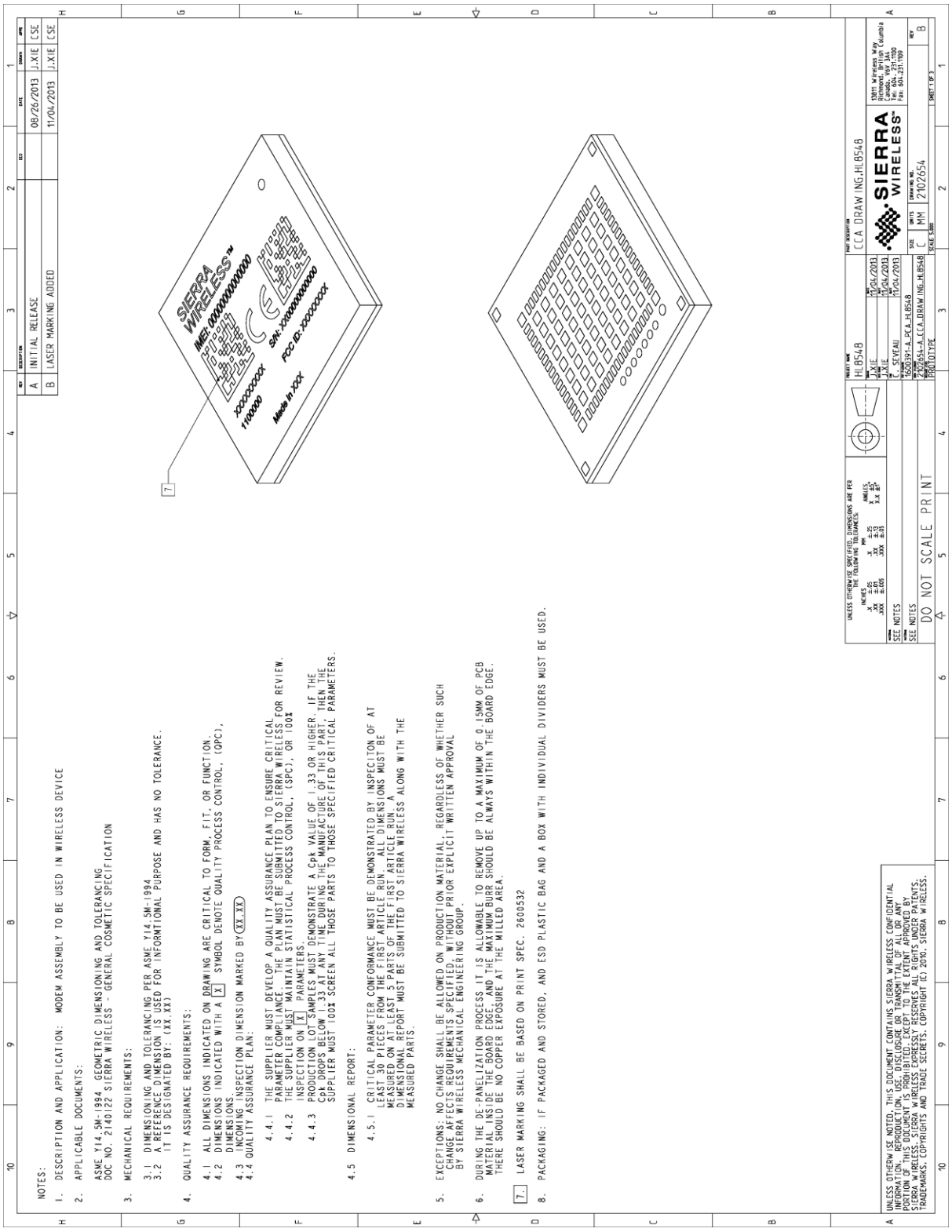

Figure 7. Mechanical Drawing

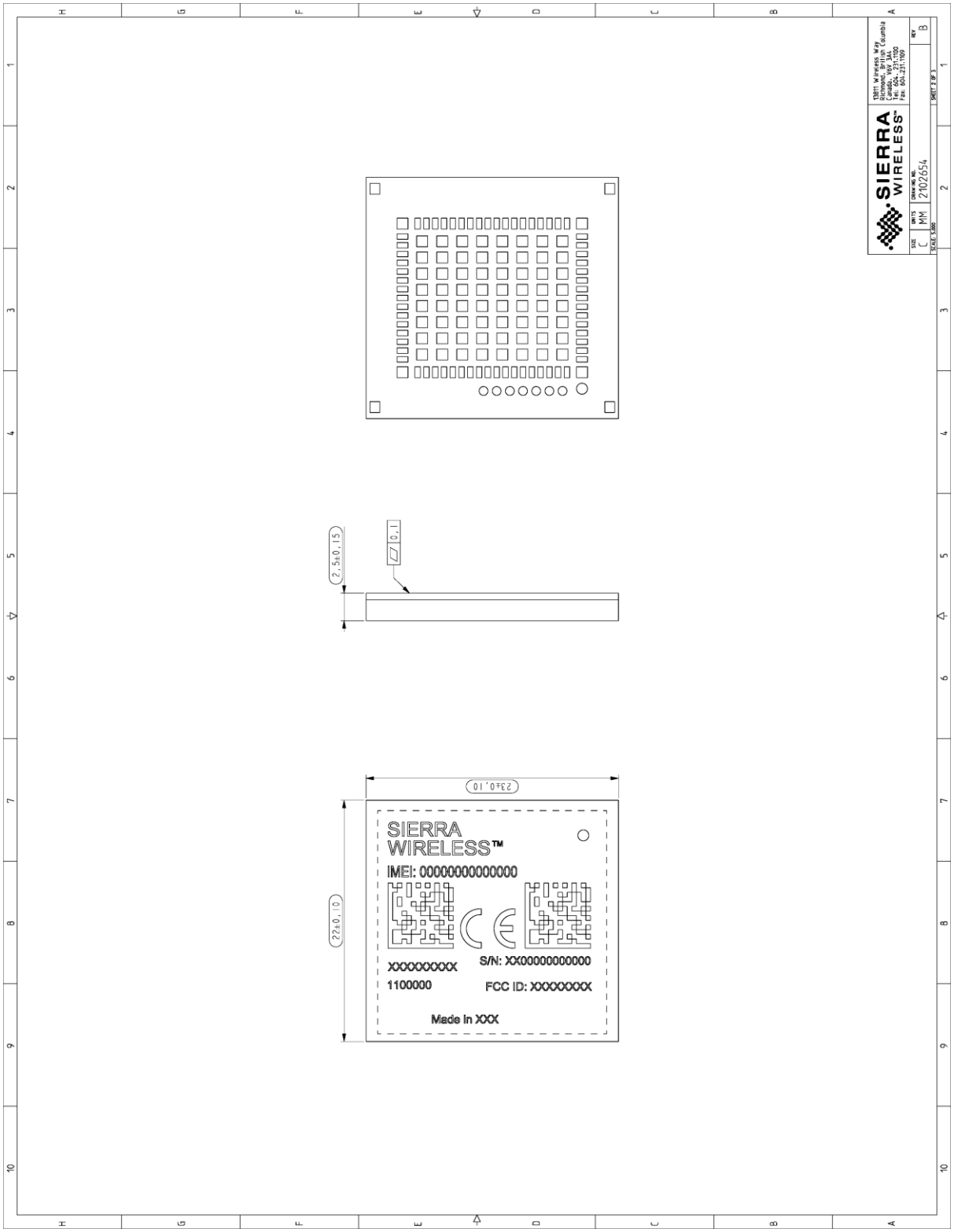

Figure 8. Dimensions Drawing

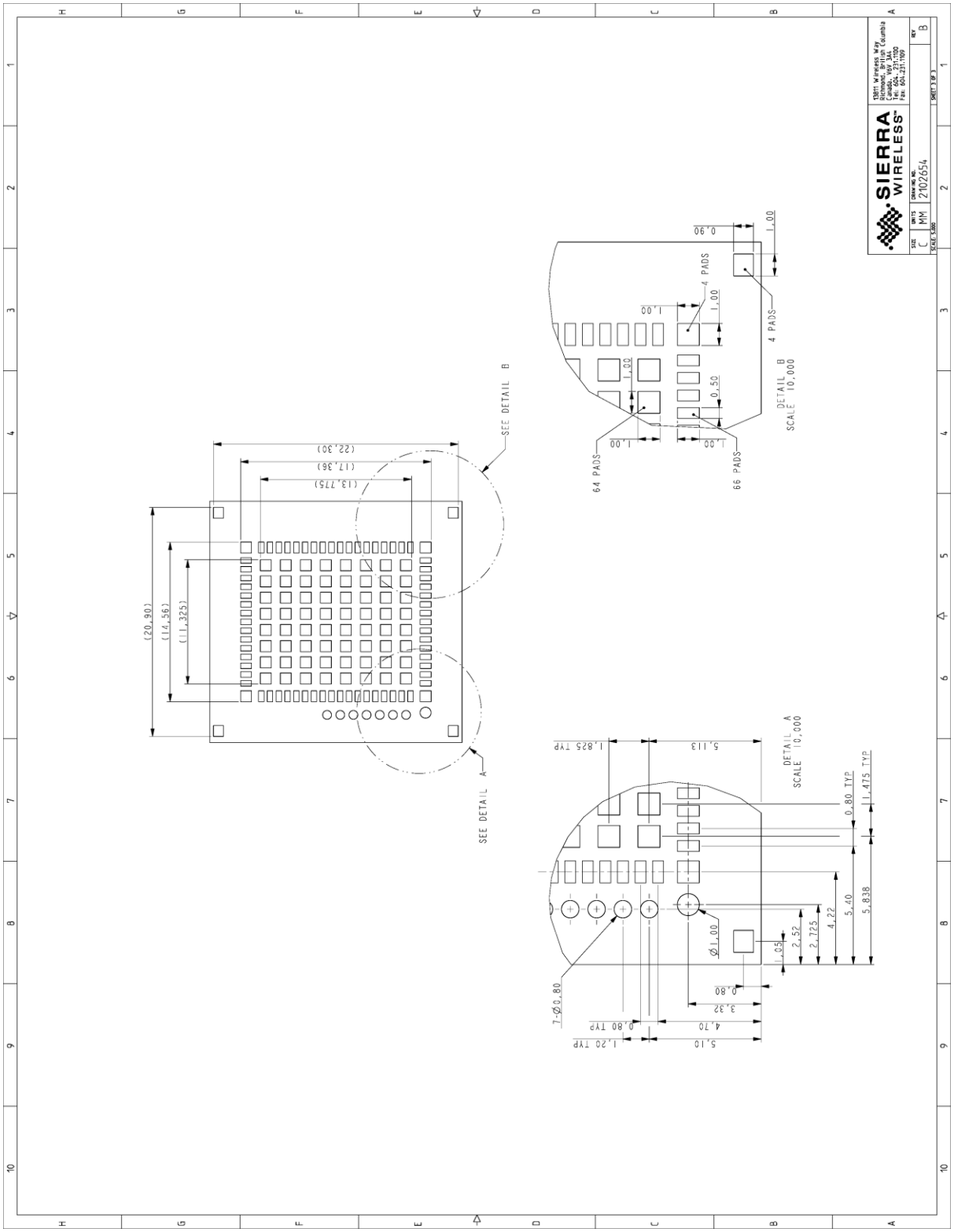

Figure 9. Footprint

5. Design Guidelines

5.1. Power-Up Sequence

Apply a low-level logic to the PWR_ON_N pad (pad 59); within approximately 25ms, VGPIO will appear to be at 1.8V. Either UART1 or the USB interface could be used to send AT commands. The AT command interface is available in about 7 seconds after PWR_ON_N for either UART1 or USB.

When using UART1, the AT command interface is available after the transition of UART1_CTS from high to low level.

When using a USB connection, the HL7528 will start communicating with the host after USB enumeration. The time when AT commands can be sent will depend on the initialization time on the USB host.

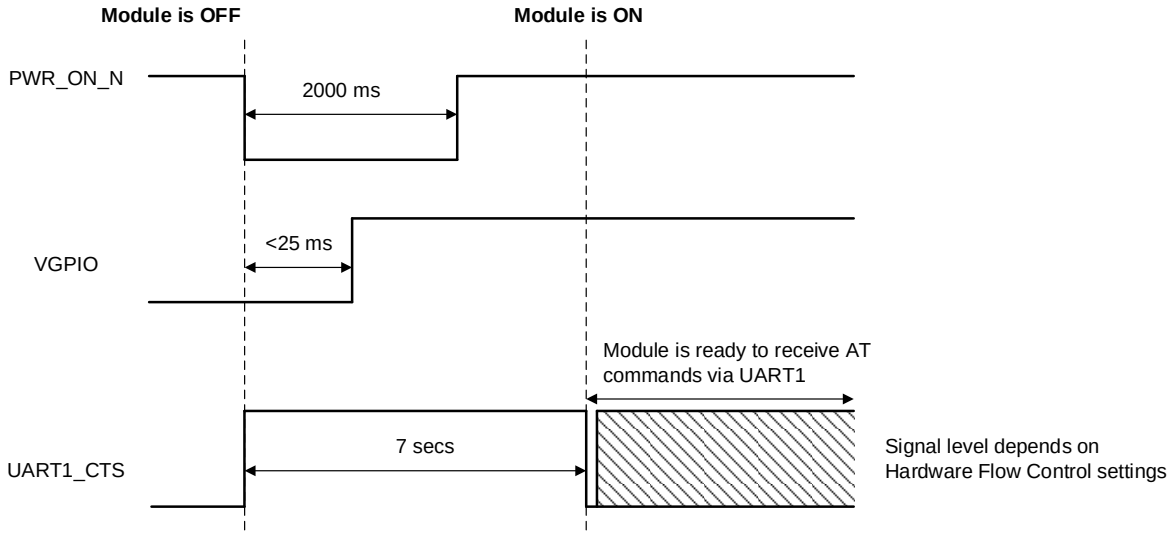

Figure 10. PWR_ON_N Sequence with VGPIO Information

Note: As PWR_ON_N is internally pulled up with 100kΩ, an open collector or open drain transistor must be used for ignition.

The PWR_ON_N pad has the minimum assertion time requirement of 25ms, with LOW active. Once the valid power on trigger is detected, the PWR_ON_N pad status can be left open.

The maximum VBATT ramp up time to 3.2V is 32ms.

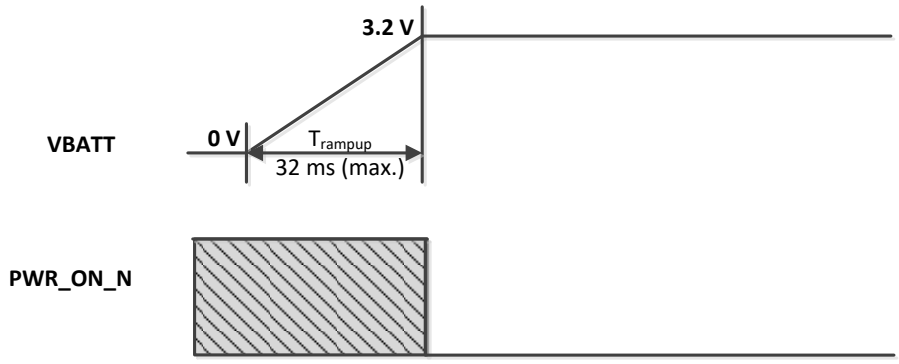

Figure 11. VBATT Ramp Up Timing

5.2. Module Switch-Off

AT command **AT+CFUN** enables the user to properly switch the AirPrime HL7528 module off.

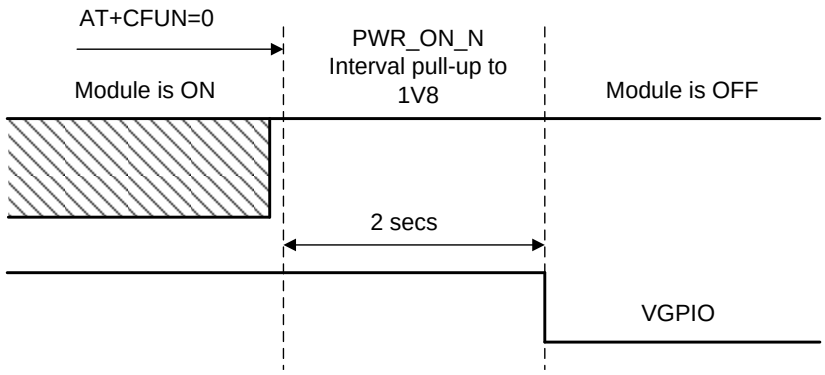

Figure 12. Power OFF Sequence for PWR_ON_N, VGPIO

Note: PWR_ON_N is internally pulled up by 100kΩ to 1.8V.

5.3. Emergency Power OFF

If required, the module can be switched off by controlling the RESET_IN_N pad (pad 11). This must only be used in emergency situations if the system freezes (not responding to AT commands).

To perform an emergency power off, a low-level pulse must be sent on the RESET_IN_N pad for 20ms while the PWR_ON_N signal is inactive (high level). This action will immediately shut the HL7528 module down and the registers of the CPU and RAM memory will be reset for the next power on.

5.4. Sleep Mode Management

5.4.1. Using UART1

AT command **AT+KSLEEP** enables sleep mode configuration.

AT+KSLEEP=0:

- The AirPrime HL7528 module is active when DTR signal is active (low electrical level).
- When DTR is deactivated (high electrical level), the AirPrime HL7528 module enters sleep mode after a while.
- On DTR activation (low electrical level), the AirPrime HL7528 module wakes up.

AT+KSLEEP=1:

- The AirPrime HL7528 module determines when it enters sleep mode (when no more tasks are running).
- “0x00” character on the serial link wakes the AirPrime HL7528 module up.

AT+KSLEEP=2: The AirPrime HL7528 module never enters sleep mode.

5.4.2. Using USB

Use **AT+KSLEEP=1** to allows the module to automatically enter sleep mode while the USB interface is in use.

5.5. Power Supply Design

The AirPrime HL7528 module should not be supplied with voltage over 4.5V even temporarily or however briefly.

If the system's main board power supply unit is unstable or if the system's main board is supplied with over 4.5V, even in the case of transient voltage presence on the circuit, the module's power amplifier may be severely damaged.

To avoid such issues, add a voltage limiter to the module's power supply lines so that VBATT and VBATT_PA signal pads will never receive a voltage surge over 4.5V. The voltage limiter can be as simple as a Zener diode with decoupling capacitors as shown in the diagram below.

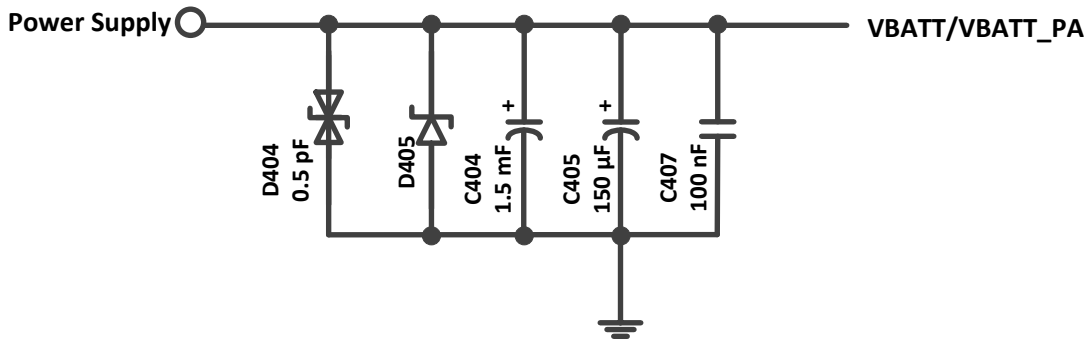

Figure 13. Voltage Limiter Example

5.6. Power Cycle

In addition to Sierra Wireless' reliable recovery mechanisms, it is highly recommended that the ability for a power cycle to reboot the module be included in the design in case the module becomes blocked and stops responding to reset commands.

5.7. ESD Guidelines for SIM Card

Decoupling capacitors must be added according to the drawings below as close as possible to the SIM card connectors on UIM1_CLK, UIM1_RST, UIM1_VCC, UIM1_DATA and UIM1_DET signals to avoid EMC issues and to comply with the requirements of ETSI and 3GPP standards covering the SIM electrical interface.

A typical schematic including SIM detection is provided below.

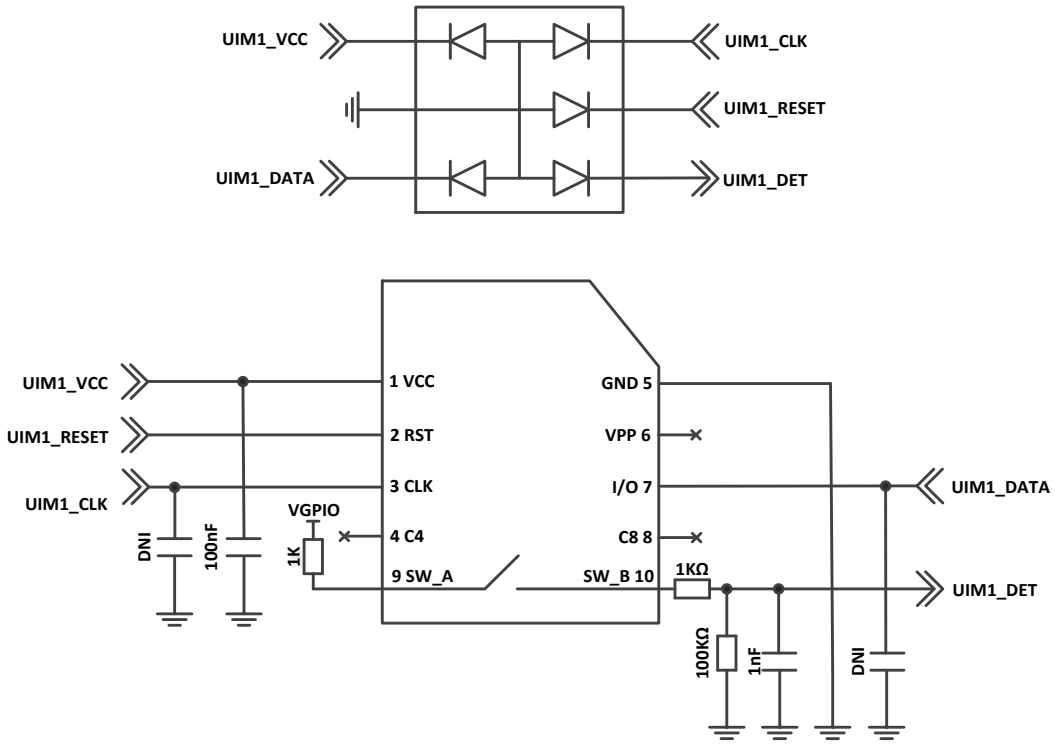

Figure 14. EMC and ESD Components Close to the SIM

5.8. ESD Guidelines for USB

When the USB interface is externally accessible, it is required to have ESD protection on the USB_VBUS, USB_D+ and USB_D- signals.

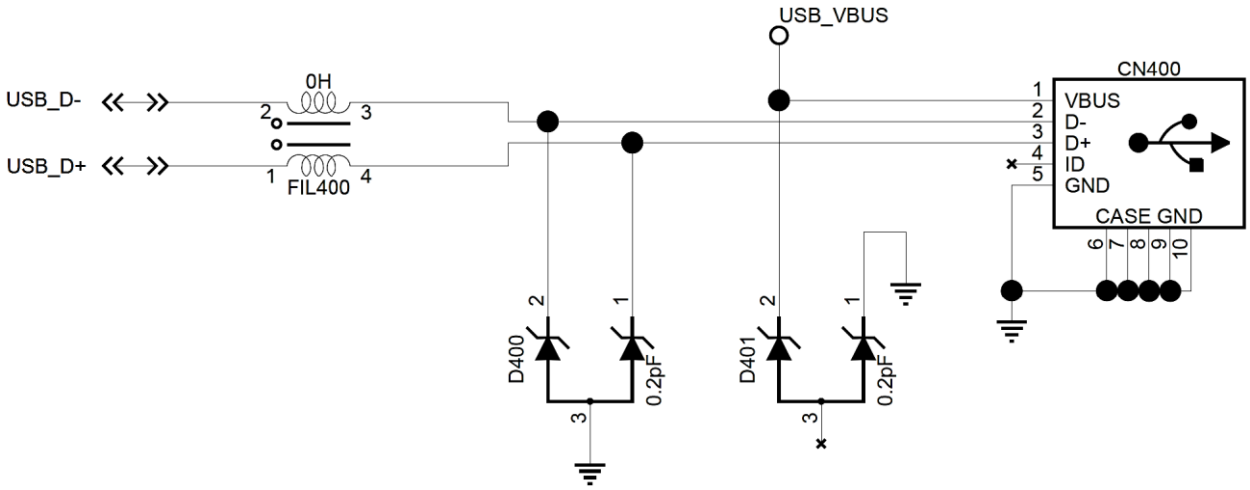

Figure 15. ESD Protection for USB

Note: It is not recommended to have an ESD diode with feedback path from USB_VBUS to either USB_D+ or USB_D-.

Sierra Wireless recommends using a 90Ω DLP0NSN900HL2L EMC filter and an RCLAMP0503N or ESD5V3U2U-03LRH ESD diode.

5.9. Radio Integration

The AirPrime HL7528 is equipped with an external antenna. A 50Ω line matching circuit between the module, the customer's board and the RF antenna is required, for the GSM feed path, as shown in the example below.

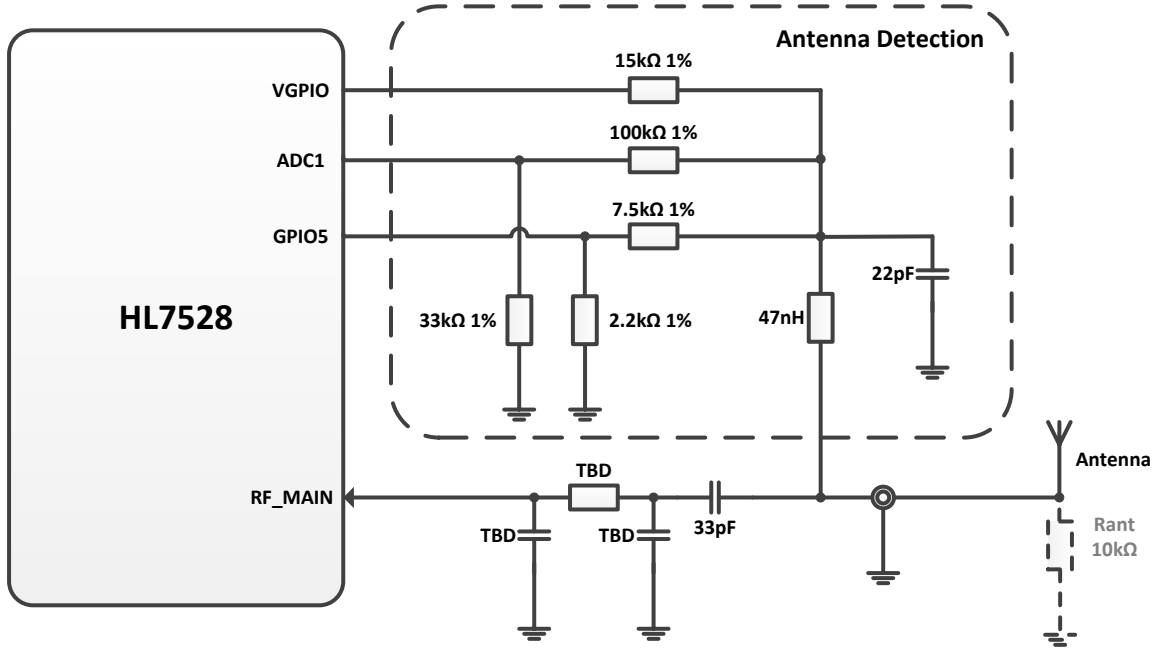

Figure 16. GSM Antenna Connection with Antenna Detection

Note:	*Antenna detection circuit is optional. Rant is the equivalent DC terminating resistor of the antenna. Rant should be close to 10 kΩ.*

6. Ordering Information

Table 32. Ordering Information

Model Name	Description	Part Number
HL7528	HL7528 embedded module	Contact Sierra Wireless for the latest SKU
DEV-KIT	HL Series Development Kit	6000620

7. Terms and Abbreviations

Abbreviation	Definition
ADC	Analog to Digital Converter
AGC	Automatic Gain Control
AT	Attention (prefix for modem commands)
CDMA	Code Division Multiple Access
CF3	Common Flexible Form Factor
CLK	Clock
CODEC	Coder Decoder
CPU	Central Processing Unit
DAC	Digital to Analog Converter
DTR	Data Terminal Ready
EGNOS	European Geostationary Navigation Overlay Service
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
EN	Enable
ESD	Electrostatic Discharges
ETSI	European Telecommunications Standards Institute
FDMA	Frequency-division multiple access
GAGAN	GPS aided geo augmented navigation
GLONASS	Global Navigation Satellite System
GND	Ground
GNSS	Global Navigation Satellite System
GPIO	General Purpose Input Output
GPRS	General Packet Radio Service
GSM	Global System for Mobile communications
Hi Z	High impedance (Z)
IC	Integrated Circuit
IMEI	International Mobile Equipment Identification
I/O	Input / Output
LED	Light Emitting Diode
LNA	Low Noise Amplifier
MAX	Maximum
MIN	Minimum
MSAS	Multi-functional Satellite Augmentation System
N/A	Not Applicable
PA	Power Amplifier
PC	Personal Computer
PCB	Printed Circuit Board
PCL	Power Control Level
PLL	Phase Lock Loop
PWM	Pulse Width Modulation
QZSS	Quasi-Zenith Satellite System

Abbreviation	Definition
RF	Radio Frequency
RFI	Radio Frequency Interference
RMS	Root Mean Square
RST	Reset
RTC	Real Time Clock
RX	Receive
SCL	Serial Clock
SDA	Serial Data
SIM	Subscriber Identification Module
SMD	Surface Mounted Device/Design
SPI	Serial Peripheral Interface
SW	Software
PSRAM	Pseudo Static RAM
TBC	To Be Confirmed
TBD	To Be Defined
TP	Test Point
TX	Transmit
TYP	Typical
UART	Universal Asynchronous Receiver-Transmitter
UICC	Universal Integrated Circuit Card
USB	Universal Serial Bus
UIM	User Identity Module
VBATT	Main Supply Voltage from Battery or DC adapter
VSWR	Voltage Standing Wave Ratio
WAAS	Wide Area Augmentation System