Modules

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Product Technical Specification

HL7900/HL7900E

February 2026

41114801 Rev. 5

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Revision History

Revision Number	Release Date	Changes
1	May 2024	Document creation, preliminary release
1.1	August 2024	Added: ▪ Japan radio and telecom approvals ▪ FCC/IC IDs ▪ Table 4-6 ▪ Fig. 6-1 ▪ 6.5 General Rules and Recommendations ▪ Minor edits from internal reviews ▪ I2C ▪ SPI Updated: ▪ Table 3-6, Table 3-7, Table 3-9, Table 4-4, Table 4-9, Table 4-18 ▪ Power supply min. values

Revision Number	Release Date	Changes
2	June 2025	Updated: ▪ Table 1-3 LGA Pin Types / Distribution (inner ring pin pitch) ▪ Table 1-4 General Features (Cat-M1 UL/DL rates) ▪ Table 2-2 Ring C Pin Definitions (Changed pin C43 from Reserved to EXT_GPS_L-NA_EN; added footnote for MCU/SHUB support) ▪ Table 2-3 Ring B Pin Definitions (added footnote for MCU/SHUB support) ▪ Updated 3.5: Current Consumption (marked as preliminary) ▪ Table 3-6 HL7900 LPM Current Consumption — Cat-M1 (Typ consumption values) ▪ Table 3-7 HL7900 LPM Current Consumption — NB (Typ consumption values) ▪ Table 3-10 HL7900 Current Consumption — LTE NB-2 Connected Mode (Subcarriers uplink MCS value) ▪ Combined Table 4-4 GPIO Pin Descriptions and Table 4-5 GPIO into Table 4-4 GPIO Pin Descriptions ▪ Added section heading 4.3.1: GPIO7 Usage, Figure 4-1, GPIO7 Waveform Behavior Figure 4-2, GPIO7 Waveform—Boot up and Hibernate mode, Figure 4-3, GPIO7 Waveform—Manual Wake Up, Table 4-6 GPIO7 Timing for Manual Wake Up ▪ 4.4.3: UART Application Examples (added 2-wire UART note) ▪ 4.5: Power On Signal (POWER_ON_N) — Description, Bias voltage value, and Table 4-8 (pin description) ▪ Figure 4-7, Power On and Reset Sequence (unmanaged POWER_ON_N) and Table 4-10 POWER_ON_N Timing (unmanaged) (added T7 timing) ▪ 4.6.1: Software Power Off in Unmanaged Mode ▪ Marked 4.11.2: Wakeup from OFF Mode, 4.11.3: Wakeup from Lite Hibernate Mode, and 4.11.4: Wakeup from Hibernate Mode as supported (removed future firmware release note) ▪ Table 4-19 WAKEUP Timing (from OFF Mode) (timing values) ▪ Table 4-20 WAKEUP Timing (from Lite Hibernate Mode) (timing values) ▪ Table 4-21 WAKEUP Timing (from Hibernate Mode) (timing values) ▪ Table 4-28 TX_ON Characteristics (timing values) ▪ 4.16: GNSS — Removed future firmware release note; Noted SKU-dependency ▪ Added Table 4-32 GNSS Active Antenna — Specifications (Preliminary) ▪ Table 4-33 GNSS Performance (typical values) ▪ Added 4.16.2: EXT_GPS_LNA_EN ▪ Added 4.23: Wi-Fi ▪ Updated Figure 5-1, Mechanical Drawing, Figure 5-2, Top Side ▪ 6.1: Power Supply Design (updated recommended ESD parts) ▪ 6.2: UIM1 (removed DNI from UIM1_VCC decoupling capacitor) ▪ 6.6.1: Antenna Matching Circuit (updated recommended TVS parts) ▪ Table 6-1 Recommended Antenna Tuning Switches for HL7900 (added AT commands) ▪ 8.2.2: Japan Radio and Telecom Approval — Updated Radio telecom approval number; added section 8.2.2.1: Transmission restriction note and carrier sense requirement for Sub-GHz regulation

Revision Number	Release Date	Changes
3	September 2025	Updated: ▪ Table 3-3 Digital I/O Electrical Characteristics (1.80V) (min/max values) ▪ Table 3-6 HL7900 LPM Current Consumption — Cat-M1 (Typ values) ▪ Table 3-7 HL7900 LPM Current Consumption — NB (Typ values) ▪ Table 4-5 GPIO7 Timing for Boot up and Hibernate Mode (T3_eDRX values) ▪ Table 4-7 UART1 Pin Description (C3/C5 Default State — replaced pull-down with Hi-Z) ▪ Table 4-17 WAKEUP Pin Description (added pull-down requirement to C44) ▪ 4.10.2: Secondary UART Interface (SHUB to be supported in future update)) ▪ 4.11.2: Wakeup from OFF Mode (updated UART1_CTS timing) ▪ Table 4-25 HL7900 Typical Conducted Cat-M1 RX Sensitivity (values @ 25°C) ▪ Table 4-26 HL7900 Typical Conducted NB1/NB2 RX Sensitivity (values @ 25°C) ▪ 4.22: SPI Interface (updated description, added master/slave timing)
3.1	November 2025	Updated: ▪ 8.2.2 Japan Radio and Telecom Approval
4	December 2025	Updated: ▪ Added HL7900E information
5	February 2026	Updated: ▪ 8.2.1 Important Compliance Information for Canada and the United States ▪ 8.2.2 Japan Radio and Telecom Approval ▪ Table 8-1: Product Name Antenna Gain Specifications

Contents

1: Introduction

This document defines the high-level product features and illustrates the interfaces for the HL7900/HL7900E module, designed for the Internet of Things (IoT) markets. It covers the hardware aspects of the product, including electrical and mechanical. For additional documentation (e.g. Firmware Customer Release Notes, AT Command Reference, etc.), refer to the module page at the Source: source.sierrawireless.com.

Note: Upon commercial release, you may download additional documentation from the Source.

The HL7900/HL7900E module supports a UART as the primary host interface, as well as a variety of peripheral interfaces such as ADCs and GPIOs. It is designed to be extremely low power and supports several low power modes to enable long lasting battery powered applications.

Note: Semtech modules are shipped factory-programmed with industry or mobile operator approved firmware, according to the specific SKU ordered. Periodically, newer firmware versions become available and can include new features, bug fixes, or critical security updates. Semtech strongly recommends that customers establish their own production capability for updating module firmware on their assembled end platform, in the event that a newer firmware must be installed before deployment. Semtech also recommends customers design their products to support post-deployment FOTA upgrades using the AirVantage cloud platform.

1.1 Ready-to-Connect (R2C)

The HL7900/HL7900E is a Sierra Wireless Ready-to-Connect (R2C) module that supports the use of its embedded SIM (eSIM) or an external SIM for global data connectivity on the RF bands detailed in 1.2: Supported RF Bands.

For details about using the HL7900/HL7900E eSIM with Sierra Smart Connectivity, refer to the Semtech Ready-to-Connect Module Integration Guide. For additional information on Sierra Smart Connectivity, explore www.sierrawireless.com or contact Semtech.

Note: The Semtech eSIM is SKU-dependent and not included in all modules. Contact Semtech for details.

1.2 Supported RF Bands

Table 1-1: HL7900/HL7900E Supported RF Bands/Connectivity

RF Band	Transmit (Tx) Frequency (MHz)	Receive (Rx) Frequency (MHz)	Cat-M1	Cat-NB1/NB2
LTE B1	1920–1980	2110–2170	Y	Y
LTE B2	1850–1910	1930–1990	Y	Y[a]
LTE B3	1710–1785	1805–1880	Y	Y
LTE B4	1710–1755	2110–2155	Y	Y[a]
LTE B5	824–849	869–894	Y	Y[a]
LTE B8	880–915	925–960	Y	Y
LTE B12	699–716	729–746	Y	Y[a]

Table 1-1: HL7900/HL7900E Supported RF Bands/Connectivity (Continued)

RF Band	Transmit (Tx) Frequency (MHz)	Receive (Rx) Frequency (MHz)	Cat-M1	Cat-NB1/NB2
LTE B13	777–787	746–756	Y	Y[a]
LTE B18	815–830	860–875	Y	Y
LTE B19	830–845	875–890	Y	Y
LTE B20	832–862	791–821	Y	Y
LTE B25	1850–1915	1930–1995	Y	Y[a]
LTE B26	814–849	859–894	Y	Y[a]
LTE B28	703–748	758–803	Y	Y
LTE B65	1920–2010	2110–2200		Y
LTE B66	1710–1780	2110–2200	Y	Y[a]
LTE B70	1695–1710	1995–2020		Y
LTE B85	698-716	728-746		Y[a]

a. To ensure FCC compliance near NB band edges, Cat-NB2 supported TX channel ranges do not include outer channels. Supported channel ranges are:
- B2: 18602–19198
- B4: 19952–20398
- B5: 20402–20648
- B12: 23012–23178
- B13: 23182–23278
- B25: 26042–26688
- B26: 26692–27038
- B66: 131974–132670
- B70: 132974–133119
- B85: 134004–134179

1.3 Common Flexible Form Factor (CF3)

The HL7900/HL7900E belongs to Semtech's Common Flexible Form Factor (CF3) family of WWAN modules. These modules share a compatible footprint. The CF3 form factor provides a unique solution to a series of problems faced commonly in the WWAN module space as it:

- Accommodates multiple radio technologies (from GSM to LTE advanced) and band groupings
- Offers electrical and functional compatibility
- Provides direct mount, as well as socket mount (depending on customer needs,
- e.g. for use in development kits or for prototype development)

1.3.1 Physical Dimensions and Connection Interface

HL7900/HL7900E modules are compact, robust, fully shielded industrial-grade embedded modules with the dimensions noted in Table 1-2

Table 1-2: Module Dimensions[a]

Parameter	Nominal	Tolerance	Units
Length	18.0	±0.10	mm
Width	15.0	±0.10	mm
Thickness	2.5	±0.20	mm
Weight	1.17	±0.24	g

a. Typical dimensional values, accurate as of the release date of this document.

All electrical and mechanical connections to the HL7900/HL7900E module are made through the 152 Land Grid Array (LGA) Pins on the bottom side of the PCB.

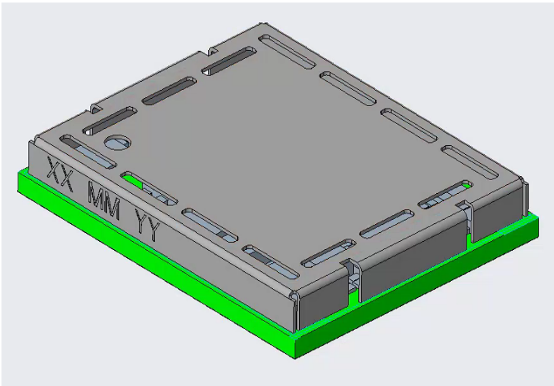


Figure 1-1: Mechanical Overview

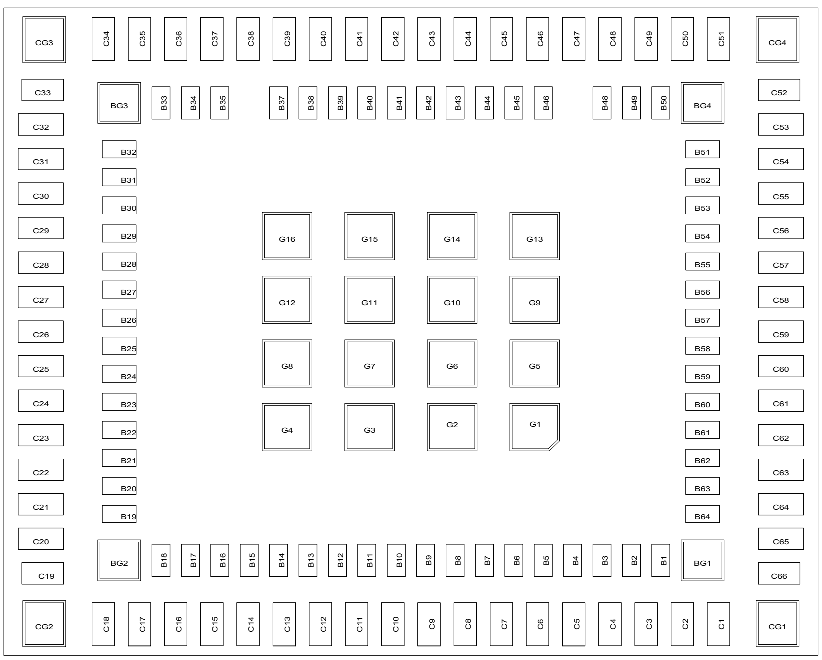


Figure 1-2: Pin Configuration (Bottom View)

Note: The customer-side PCB module footprint is described in the Customer Process Guidelines.

Table 1-3 describes the LGA Pins.

Table 1-3: LGA Pin Types / Distribution

Pin Type	Quantity	Dimensions	Pitch
Signal Pins	66 Pins	1.0×0.5 mm	0.8 mm
	62 Pins	0.75x0.4 mm	0.65 mm

Table 1-3: LGA Pin Types / Distribution (Continued)

Pin Type	Quantity	Dimensions	Pitch
Ground Pins	16 inner Pins	1.0×1.0 mm	1.825 mm/1.475 mm
	4 outer corner Pins	0.85×0.97 mm	-
	4 inner corner Pins	0.85x0.85 mm	-

1.4 General Features

Table 1-4 summarizes the HL7900/HL7900E's features.

Table 1-4: General Features

Feature	Description
Physical	Small form factor (152-Pin solderable LGA Pin). See 1.3.1: Physical Dimensions and Connection Interface for details. Metal shield can RF connection Pins (RF_MAIN and RF_GNSS—for HL7900 only) Baseband signals connection
Power supply	2.5–4.35 V supply voltage (VBAT_BB, VBAT_RF) ▪ Single supply (recommended)—VBAT (VBAT_BB tied to VBAT_RF) or ▪ Dual supplies—Single supply each for VBAT_BB and VBAT_RF
RF	Cat-M1 ▪ Power Class 3 (23 dBm) ▪ Cat-NB2 ▪ Power Class 3 (23 dBm) GNSS ▪ GPS—1575.42 MHz ▪ GLONASS—1589.0625–1605.375 MHz See 4.16: GNSS details. *Note: The GNSS receiver and LTE receiver share the same RF resources, therefore GNSS can only be used when the module is not actively connected on LTE. An example of a suitable implementation of GNSS in an end product would be the use of GNSS positioning for asset management applications where infrequent and no real-time position updates are required.*
SIM interface	1.8V support SIM extraction / hot plug detection SIM/USIM support Conforms with ETSI UICC Specifications Supports SIM application tool kit with proactive UICC commands
Application interface	AT command interface—3GPP 27.007 standard, plus proprietary extended AT commands CMUX multiplexing over UART

Table 1-4: General Features (Continued)

Feature	Description

Protocol stack	Cat-M1
	▪ 3GPP Rel. 14:
	  ▪ Up to 1119 kbit/s UL, 588 kbit/s DL
	  ▪ HARQ-ACK bundling in HD-FDD
	  ▪ 10 DL HARQ processes
	  ▪ Faster frequency returning
	  ▪ Release Assistance Indication
	▪ Half-duplex
	▪ Channel bandwidth—1.4 MHz
	▪ LTE carrier bandwidth—1.4/3/5/10 /15/20 MHz
	▪ Extended Coverage Mode A
	▪ PSM (Power Save Mode)
	▪ I-DRX (Idle Mode Discontinuous Reception)
	▪ C-DRX (Connected Mode Discontinuous Reception)
	▪ Idle mode mobility
	▪ Connected mode mobility
	▪ eDRX (Extended Discontinuous Reception)
	▪ Control Plane CIoT Optimization (Data over NAS)
	NB-IoT
	▪ 3GPP Rel. 14:
	  ▪ Up to 158 kbit/s UL, 127 kbit/s DL
	  ▪ 2 HARQ processes
	  ▪ Release Assistance Indication
	  ▪ Long DRX values with regular wake-up cycle)
	  ▪ Cat-NB2
	▪ Half-duplex
	▪ Channel bandwidth—180 kHz
	▪ LTE carrier bandwidth—1.4/3/5/10 /15/20 MHz
	▪ Operational mode—In-band, Guard band, Standalone
	▪ Control Plane CIoT Optimization (Data over NAS)
	▪ NIDD over SGi tunneling
	▪ NIDD over SCEF
	▪ Extended coverage
	▪ PSM (Power Save Mode)
	▪ I-DRX (Idle Mode Discontinuous Reception)
	▪ C-DRX (Connected Mode Discontinuous Reception)
	▪ Idle mode mobility
	▪ eDRX (Extended Discontinuous Reception)
	Flexible selection
	▪ Manual system selection across RATs
	▪ Dynamic system selection across RATs (preferred RAT)

Table 1-4: General Features (Continued)

Feature	Description
Connectivity	Multiple cellular packet data profiles Sleep mode for minimum idle power draw Mobile-originated PDP context activation / deactivation Static and Dynamic IP address. The network may assign a fixed IP address or dynamically assign one using DHCP (Dynamic Host Configuration Protocol). PDP context type (IPv4, IPv6, IPv4v6) RFC1144 TCP/IP header compression
Environmental	Operating temperature ranges ▪ Class A: -30°C to +70°C ▪ Class B: -40°C to +85°C
RTC	Real Time Clock (RTC)

1.5 Architecture

The following figures present an overview of the HL7900 's and HL7900E's internal architecture and external interfaces.

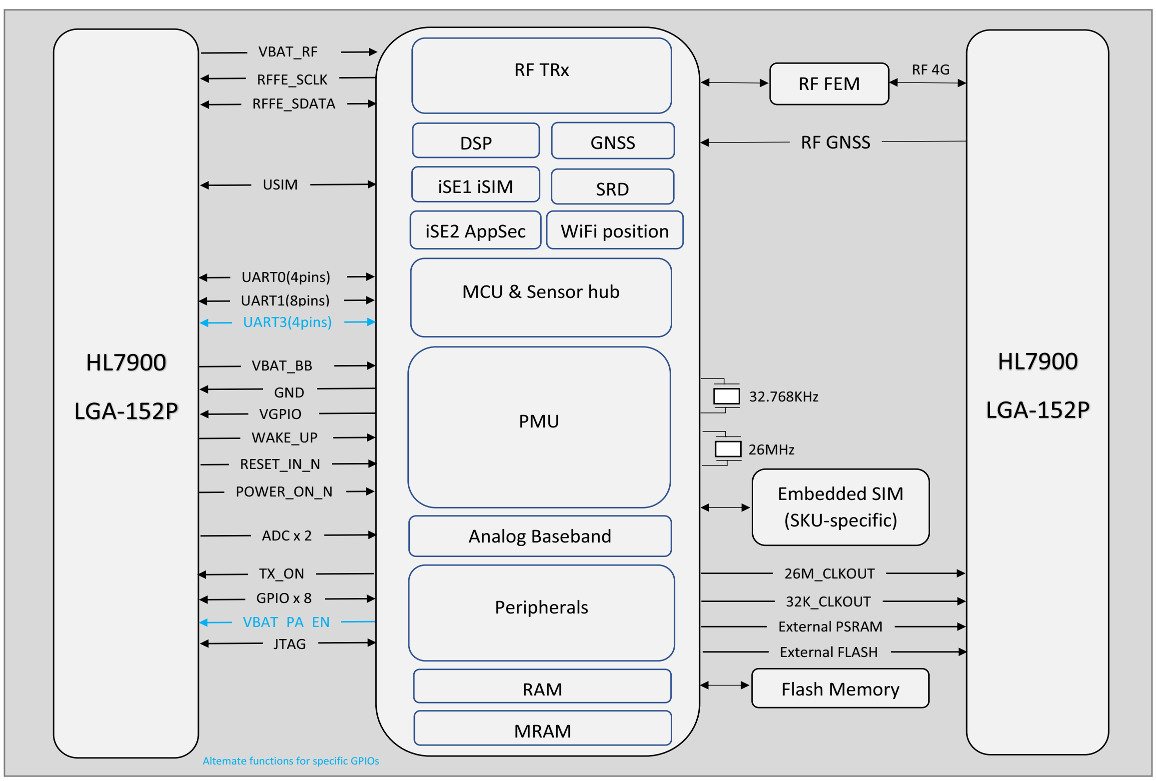


Figure 1-3: HL7900 Architecture Overview

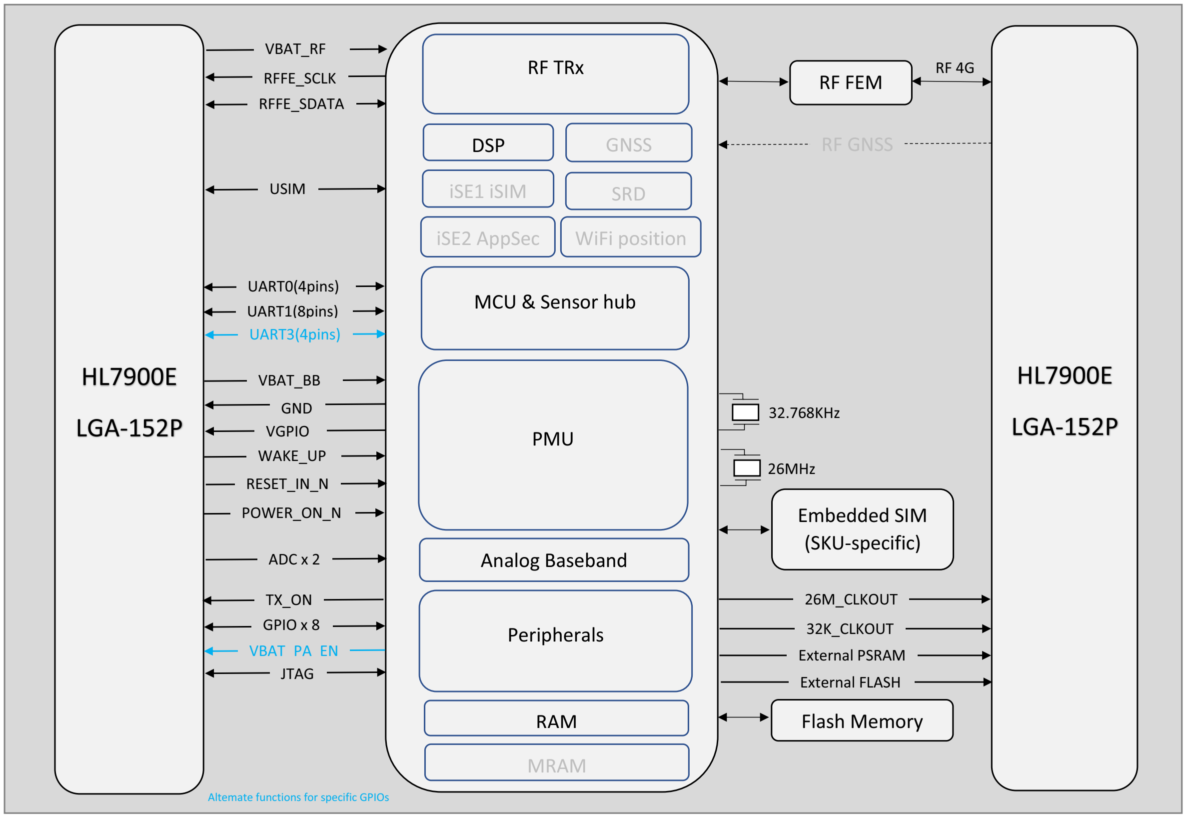


Figure 1-4: HL7900E Architecture Overview

1.6 Interfaces

The HL7900/HL7900E provides the following interfaces and peripheral connectivity:

- (1) VGPIO (1.8V)— See 4.1: VGPIO
- (1) 1.8V USIM— See 4.2: USIM Interface
- (12) GPIOs— See 4.3: General Purpose Input/Output (GPIO).
- (1) 8-wire UART— See 4.4: Main Serial Link (UART1).
- (1) Active low power on signal— See 4.5: Power On Signal (POWER_ON_N).
- (1) Active low reset signal— See 4.7: Reset Signal (RESET_IN_N).
- (2) ADC— See 4.8: Analog to Digital Converter (ADC).
- (2) System clock out (32.768 kHz and 26 MHz)— See 4.9: Clock Interface.
- (1) 4-wire UART for debug interface only— See 4.10: Debug Interfaces.
- (1) Wake up signal— See 4.11: Wake Up Signal (WAKEUP).
- (1) Main RF Antenna— See 4.12: External Host Alarm Pin.
- (1) TX_ON indicator— See 4.14: TX Burst Indicator (TX_ON).
- (1) GNSS Antenna — See 4.16: GNSS.
- (1) External PA Voltage Control Indicator— See4.15: Tx/Rx Activity Indicator; External RF Voltage Control.
- (1) External FLASH interface
- (1) MIPI Interface

- (1) External PSRAM interface

Table 1-5: ESD Specifications[a]

Category	Connection	Specification
Operational	▪ Power supply (C61, C62, C63) ▪ RF ports (C38, C49)	IEC-61000-4-2 (Electrostatic Discharge Immunity Test) ▪ ±6 kV Contact ▪ ±8 kV Air
Non-operational	All pins	Unless otherwise specified: ▪ JESD22-A114 ± 250 V Human Body Model ▪ JESD22-C101C ± 250V Charged Device Model

a. ESD protection is highly recommended on customer platform. For details, see 6.3: ESD Protection for I/Os

1.7 Environmental Specifications

The environmental specifications for operation and storage of the HL7900/HL7900E are defined in Table 1-6.

Table 1-6: Environmental Specifications

Parameter	Range	Operating Class
Ambient Operating Temperature	-30°C to +70°C	Class A
	-40°C to +85°C	Class B
Ambient Storage Temperature	-40°C to +85°C	-

Class A is defined as the operating temperature range within which the device:
- Shall exhibit normal function during and after environmental exposure.
- Shall meet the minimum requirements of 3GPP or appropriate wireless standards.

Class B is defined as the operating temperature range within which the device:
- Shall remain fully functional during and after environmental exposure
- Shall exhibit the ability to establish any of the device’s supported call modes (SMS, Data, and emergency calls) at all times even when one or more environmental constraint exceeds the specified tolerance.
- Unless otherwise stated, full performance should return to normal after the excessive constraint(s) have been removed.

2: Pin Definition

The HL7900/HL7900E includes two rings of pins — an outer ring (Table 2-2, Ring C Pin Definitions, on page 19) and an inner ring (Table 2-3, Ring B Pin Definitions, on page 23). For the pin configuration (layout), see Figure 1-2 on page 10.

The HL7900/HL7900E pins are divided into three categories.

- Core functions and associated pins— Cover all the mandatory features for IoT device connectivity and will be available by default across the CF3 module family. These Core functions are always available and always at the same physical Pin locations. A customer platform using only these functions and associated Pins is guaranteed to be forward and/or backward compatible with the next generation of CF3 modules.
- Extension functions and associated pins— Bring additional capabilities to the customer. Whenever an Extension function is available on a module, it is always at the same Pin location.
- Custom functions and associated pins— Module-specific functionality. If a custom function is available on another module, there is no guarantee that it will be at the same Pin location.

For example:

- UART1 interface is a "Core" function on pins C2–C9 that is available on all CF3 modules (including HL7900/HL7900E).
- UART0 signals are "Custom" functions on pins C57 and C58. These signals may or may not be available on other CF3 modules and, if available, may be on different pins.

Note: Pins marked as 'Not connected' should not be used.

Table 2-1 lists a series of codes used to identify pin characteristics throughout this document.

Table 2-1: Pin Type Codes

Code	Definition
AI	Analog Input
ANT	Antenna
GND	Ground
I	Digital Input
I/O	Digital Input/Output
N/A	Not applicable

Code	Definition
O	Digital Output
PD	Pull-down enabled
PI	Power In
PO	Power Out
PU	Pull-up enabled

Table 2-2: Ring C Pin Definitions

Pin	Signal Name	Group	I/O	Voltage Supply Domain	Function	Unused Pins Recommendation	Isolate required[a]	CF3
C1	GPIO1[b]	GPIO[c]	I/O	1.8V (VGPIO)	General purpose input/output	Leave open	Yes	Extension
	I2C_SCL[b]	I2C	I/O	1.8V (VGPIO)	I2C interface series clock	Leave open		
C2	UART1_RI[d]	UART1[c]	O	1.8V (VGPIO)	UART1 Ring Indicator	Leave open	Yes	Core
C3	UART1_RTS	UART1[c]	I	1.8V (VGPIO)	UART1 Request To Send	Mandatory connection	Yes	Core
C4	UART1_CTS	UART1[c]	O	1.8V (VGPIO)	UART1 Clear To Send	Mandatory connection	Yes	Core
C5	UART1_TX	UART1[c]	I	1.8V (VGPIO)	UART1 Transmit Data	Mandatory connection	Yes	Core
C6	UART1_RX	UART1[c]	O	1.8V (VGPIO)	UART1 Receive Data	Mandatory connection	Yes	Core
C7	UART1_DTR	UART1[c]	I	1.8V (VGPIO)	UART1 Data Terminal Ready	Leave open	Yes	Core
C8	UART1_DCD	UART1[c]	O	1.8V (VGPIO)	UART1 Data Carrier Detect	Leave open	Yes	Core
C9	UART1_DSR	UART1[c]	O	1.8V (VGPIO)	UART1 Data Set Ready	Leave open	Yes	Core
C10	GPIO2[b]	GPIO[c]	I/O	1.8V (VGPIO)	General purpose input/output	Leave open	Yes	Core
C11	RESET_IN_N	H/W Control[e]	I	Internal Bias	Input reset signal	Leave open	No	Core
C12	NC	Not connected			Not Connected	See footnote[f]	No	Not connected
C13	NC	Not connected			Not Connected	See footnote[f]	No	Not connected
C14	NC	Not connected			Not Connected	See footnote[f]	No	Not connected
C15	NC	Not connected			Not Connected	See footnote[f]	No	Not connected
C16	NC	Not connected			Not Connected	See footnote[f]	No	Not connected
C17	NC	Not connected			Not Connected	See footnote[f]	No	Not connected
C18	NC	Not connected			Not Connected	See footnote[f]	No	Not connected
C19	NC	Not connected			Not Connected	See footnote[f]	No	Not connected
C20	NC	Not connected			Not Connected	See footnote[f]	No	Not connected

Table 2-2: Ring C Pin Definitions (Continued)

Pin	Signal Name	Group	I/O	Voltage Supply Domain	Function	Unused Pins Recommendation	Isolate required[a]	CF3
C21	NC	Not connected			Not Connected	See footnote[f]	No	Not connected
C22	26M_CLKOUT	Clock[c]	O	1.8V (VGPIO)	26 MHz System Clock Output	Leave open	Yes	Extension
C23	32K_CLKOUT	Clock[c]	O	1.8V (VGPIO)	32.768 kHz System Clock Output	Leave open	Yes	Extension
C24	ADC1[b]	ADC[c]	AI	1.8V (VGPIO)	Analog to digital converter	Leave open	Yes	Extension
C25	ADC0[b]	ADC[c]	AI	1.8V (VGPIO)	Analog to digital converter	Leave open	Yes	Extension
C26	UIM1_VCC	UIM[c]	PO	1.8V	USIM1 Power supply	Leave open	No	Core
C27	UIM1_CLK	UIM[c]	O	1.8V (VGPIO)	USIM1 Clock	Leave open	No	Core
C28	UIM1_DATA	UIM[c]	I/O	1.8V (VGPIO)	USIM1 Data	Leave open	No	Core
C29	UIM1_RESET	UIM[c]	O	1.8V (VGPIO)	USIM1 Reset	Leave open	No	Core
C30	RF_DIV_GND_1	Ground	GND	Ground	Ground	Mandatory connection	No	Extension
C31	NC	Not connected			Not Connected	See footnote[f]	No	Not connected
C32	RF_DIV_GND_2	Ground	GND	Ground	Ground	Mandatory connection	No	Extension
C33	Reserved	Reserved			Reserved	Leave open	No	Extension
C34	Reserved	Reserved			Reserved	Leave open	No	Extension
C35	NC	Not connected			Not Connected	Leave open	No	Not connected
C36	NC	Not connected			Not Connected	Leave open	No	Not connected
C37	RF_GNSS_GND_1	Ground	GND	Ground	Ground (RF_GNSS)	Mandatory connection	No	Core
C38	RF_GNSS[g]	Antenna	ANT		GNSS antenna input	Leave open	No	Extension
C39	RF_GNSS_GND_2	Ground	GND	Ground	Ground (RF_GNSS)	Mandatory connection	No	Core
C40	GPIO7[b]	GPIO[c]	I/O	1.8V (VGPIO)	General purpose input/output	Leave open	Yes	Core

Table 2-2: Ring C Pin Definitions (Continued)

Pin	Signal Name	Group	I/O	Voltage Supply Domain	Function	Unused Pins Recommendation	Isolate required[a]	CF3
C41[h]	GPIO8[b]	GPIO[c]	I/O	1.8V (VGPIO)	General purpose input/output	Leave open	Yes	Core
	VBAT_PA_EN		O		Tx/Rx activity indicator/ External RF voltage control			Custom
C42	NC	Not connected			Not Connected	See footnote[f]	No	Not connected
C43	EXT_GPS_LNA_EN	Control signal	O	1.8V	External GNSS LNA enable	Leave open	Yes	Extension
C44	WAKEUP	H/W Control[e]	I	1.8V	Wake up signal	Mandatory connection	No	Extension
C45	VGPIO	Power	PO	1.8V (VGPIO)	GPIO voltage output (reference voltage)	Leave open	No	Core
C46	GPIO6[b]	GPIO[c]	I/O	1.8V (VGPIO)	General purpose input/output	Leave open	Yes	Core
C47	NC	Not connected			Not Connected	Leave open	No	Not connected
C48	RF_MAIN_GND_1	Ground	GND	Ground	Ground (RF_MAIN)	Mandatory connection	No	Core
C49	RF_MAIN	Antenna	ANT		Main RF antenna input/ output (Rx/Tx)	Mandatory connection	No	Core
C50	RF_MAIN_GND_2	Ground	GND	Ground	Ground (RF_MAIN)	Mandatory connection	No	Core
C51	GPIO14[b]	GPIO[c]	I/O	1.8V (VGPIO)	General purpose input/output	Leave open	Yes	Extension
	UART3_CTS[b]	UART3[c]	O		UART3 Clear To Send			Custom
	SPIM_EN0[b]	SPI	O		Chip select output from the master (active low)			
C52	GPIO10[b]	GPIO[c]	I/O	1.8V (VGPIO)	General purpose input/output	Leave open	Yes	Extension
	UART3_TX[b]	UART3[c]	I		UART3 Transmit data			Custom
	SPIM_MOSI[b]	SPI	O		Master output to the slave for SPI function			

Table 2-2: Ring C Pin Definitions (Continued)

Pin	Signal Name	Group	I/O	Voltage Supply Domain	Function	Unused Pins Recommendation	Isolate required[a]	CF3
C53	GPIO11[b]	GPIO[c]	I/O	1.8V (VGPIO)	General purpose input/output	Leave open	Yes	Extension
	UART3_RTS[b]	UART3[c]	I		UART3 Request To Send			Custom
	SPIM_MISO[b]	SPI	I		Master input from the slave for SPI interface			
C54	GPIO15[b]	GPIO[c]	I/O	1.8V (VGPIO)	General purpose input/output	Leave open	Yes	Extension
	UART3_RX[b]	UART3[c]	O		UART3 Receive data			Custom
	SPIM_CLK[b]	SPI	O		Clock driven by the master for SPI interface			
C55	UART0_RX	UART0[c]	O	1.8V (VGPIO)	Debug Receive data	Leave open	Yes	Extension
C56	UART0_TX	UART0[c]	I	1.8V (VGPIO)	Debug Transmit data	Leave open	Yes	Extension
C57	UART0_CTS	UART0[c]	O	1.8V (VGPIO)	Debug Clear To Send	Leave open	Yes	Custom
C58	UART0_RTS	UART0[c]	I	1.8V (VGPIO)	Debug Request To Send	Leave open	Yes	Custom
C59	POWER_ON_N	H/W Control[e]	I	Internal Bias	Active-low Power On control signal	Leave open	No	Core
C60	TX_ON	Indication[c]	O	1.8V (VGPIO)	TX transmission indication	Leave open	Yes	Extension
C61 C62	VBAT_RF	Power	PI	2.5V (min) 3.7V (typ) 4.35V (max)	Power supply	Mandatory connection	No	Core
C63	VBAT_BB	Power	PI	2.5V (min) 3.7V (typ) 4.35V (max)	Power supply	Mandatory connection	No	Core
C64	UIM1_DET	UIM1[c]	I	1.8V (VGPIO)	UIM1 Detection	Leave open	Yes	Core
	GPIO3[b]	GPIO[c]	I/O		General purpose input/output			Extension
C65	GPIO4[b]	GPIO[c]	I/O	1.8V (VGPIO)	General purpose input/output	Leave open	Yes	Extension

Table 2-2: Ring C Pin Definitions (Continued)

Pin	Signal Name	Group	I/O	Voltage Supply Domain	Function	Unused Pins Recommendation	Isolate required[a]	CF3
C66	GPIO5[b]	GPIO[c]	I/O	1.8V (VGPIO)	General purpose input/output	Leave open	Yes	Extension
	I2C_SDA[b]	I2C	I/O	1.8V (VGPIO)	I2C interface series data	Leave open		
CG1-CG4	GND	Ground	GND	Ground	Ground	Mandatory connection	No	Core
G1-G16	GND	Ground	GND	Ground	Ground	Mandatory connection	No	Core

a. The host platform should isolate these signals during module Hibernate mode to prevent back-powering the module. For details, see 6.4: Hibernate—Isolation Requirements.
b. Pin can be assigned to either the internal MCU or Sensor Hub (SHUB).
c. By default, signals in group (GPIO, UART, UIM1, ADC, Clock, Indication) are hardware-configured as inputs and are in an undefined state during OFF, reset, and Hibernate modes. The host should ignore all activity on these signals until the module has initialized and reached AT-READY (UART1_CTS transitions from high to low (and stays low) and VGPIO is high, indicating the UART interface is ready). For timing details, see 4.5.1: Unmanaged POWER_ON_N (Default) and 4.11.2: Wakeup from OFF Mode. For further information regarding pre- and post-AT-READY signal states, contact Semtech.
d. UART1_RI cannot be used in Hibernate mode. A GPIO (GPIO2 by default) can be configured as an alternate ring indicator. For details, see 4.4.1: Ring Indicator (UART1_RI or Alternative).
e. Hardware Control signals are available in all module operational modes and determine module behavior. For recommendations on managing these signals, see associated signal topics in 4:: Detailed Interface Specifications.
f. Pin is not connected internally, but is reserved for future use. Leave unconnected to ensure compatibility with other Sierra Wireless CF3 modules.
g. Supported on HL7900 only. Leave open for HL7900E.
h. The default function is VBAT_PA_EN for C41. Contact Semtech to enable the GPIO function.

Table 2-3: Ring B Pin Definitions

Pin	Signal Name	Group	I/O	Voltage Supply Domain	Function	Unused Pins Recommendation	Isolate required[a]	CF3
B1	SF_SI/IO0	External FLASH	I/O	1.8V	Serial Flash Input/Output (IO0) for Dual or Quad commands	Leave open	Yes	Extension
B2	SF_SO/IO1	External FLASH	I/O	1.8V	Serial Flash Input/Output (IO1) for Dual or Quad commands	Leave open	Yes	Extension
B3	SF_nWP/IO2	External FLASH	I/O	1.8V	Serial Flash Input/Output (IO2) for Quad commands	Leave open	Yes	Extension
B4	SF_nHOLD/IO3	External FLASH	I/O	1.8V	Serial Flash Input/Output (IO3) for Quad commands	Leave open	Yes	Extension
B5	SF_CLK	External FLASH	O	1.8V	Serial Flash Serial Clock	Leave open	Yes	Extension

Table 2-3: Ring B Pin Definitions (Continued)

Pin	Signal Name	Group	I/O	Voltage Supply Domain	Function	Unused Pins Recommendation	Isolate required[a]	CF3
B6	SF_nCS0	External FLASH	O	1.8V	Serial Flash Chip Select 0	Leave open	Yes	Extension
B7	EXT_ALARM	PMU	O	1.8V	Alarm output	Leave open	No	Extension
B8	NC	Not connected			Not Connected	Leave open	No	Not Connected
B9	NC	Not connected			Not Connected	Leave open	No	Not Connected
B10	NC	Not connected			Not Connected	Leave open	No	Not Connected
B11	GPIO47[b]	GPIO	I/O	1.8V	General purpose input/output	Leave open	Yes	Extension
B12	NC	Not connected			Not Connected	Leave open	No	Not Connected
B13	WAKEUP_1_SHUB	H/W Control	I/O	1.8V	Wake up signal	Mandatory connection	No	Core
B14	VDD_PSRAM	Power	O	1.8V	Power source for external FLASH/PSRAM	Leave open	No	Core
B15	NC	Not connected			Not Connected	Leave open	No	Not Connected
B16	NC	Not connected			Not Connected	Leave open	No	Not Connected
B17	NC	Not connected			Not Connected	Leave open	No	Not Connected
B18	NC	Not connected			Not Connected	Leave open	No	Not Connected
B19	NC	Not connected			Not Connected	Leave open	No	Not Connected
B20	NC	Not connected			Not Connected	Leave open	No	Not Connected
B21	NC	Not connected			Not Connected	Leave open	No	Not Connected
B22	NC	Not connected			Not Connected	Leave open	No	Not Connected
B23	NC	Not connected			Not Connected	Leave open	No	Not Connected
B24	GPIO46[b]	GPIO	I/O	1.8V	General purpose input/output	Leave open	Yes	Extension
B25	NC	Not connected			Not Connected	Leave open	No	Not Connected
B26	NC	Not connected			Not Connected	Leave open	No	Not Connected

Table 2-3: Ring B Pin Definitions (Continued)

Pin	Signal Name	Group	I/O	Voltage Supply Domain	Function	Unused Pins Recommendation	Isolate required[a]	CF3
B27	NC	Not connected			Not Connected	Leave open	No	Not Connected
B28	NC	Not connected			Not Connected	Leave open	No	Not Connected
B29	NC	Not connected			Not Connected	Leave open	No	Not Connected
B30	NC	Not connected			Not Connected	Leave open	No	Not Connected
B31	NC	Not connected			Not Connected	Leave open	No	Not Connected
B32	NC	Not connected			Not Connected	Leave open	No	Not Connected
B33	NC	Not connected			Not Connected	Leave open	No	Not Connected
B34	NC	Not connected			Not Connected	Leave open	No	Not Connected
B35	GND	Ground	GND	Ground	Ground	Mandatory connection	No	Core
B37	GND	Ground	GND	Ground	Ground	Mandatory connection	No	Core
B38	NC	Not connected			Not Connected	Leave open	No	Not Connected
B39	NC	Not connected			Not Connected	Leave open	No	Not Connected
B40	NC	Not connected			Not Connected	Leave open	No	Not Connected
B41	NC	Not connected			Not Connected	Leave open	No	Not Connected
B42	NC	Not connected			Not Connected	Leave open	No	Not Connected
B43	NC	Not connected			Not Connected	Leave open	No	Not Connected
B44	RFFE_SCLK	MIPI	O	1.8V	MIPI RFFE Clock signal	Leave open	Yes	Extension
B45	RFFE_SDATA	MIPI	I/O	1.8V	MIPI RFFE directional/ bidirectional data	Leave open	Yes	Extension
B46	GND	Ground	GND	Ground	Ground	Mandatory connection	No	Core
B48	GND	Ground	GND	Ground	Ground	Mandatory connection	No	Core
B49	GND	Ground	GND	Ground	Ground	Mandatory connection	No	Core

Table 2-3: Ring B Pin Definitions (Continued)

Pin	Signal Name	Group	I/O	Voltage Supply Domain	Function	Unused Pins Recommendation	Isolate required[a]	CF3
B50	GND	Ground	GND	Ground	Ground	Mandatory connection	No	Core
B51	PSRAM_CSN	External PSRAM	O	1.8V	PSRAM Chip Select	Leave open	Yes	Extension
B52	PSRAM_IO2	External PSRAM	I/O	1.8V	PSRAM I/O 2	Leave open	Yes	Extension
B53	PSRAM_IO0	External PSRAM	I/O	1.8V	PSRAM I/O 0	Leave open	Yes	Extension
B54	PSRAM_IO3	External PSRAM	I/O	1.8V	PSRAM I/O 3	Leave open	Yes	Extension
B55	PSRAM_IO1	External PSRAM	I/O	1.8V	PSRAM I/O 1	Leave open	Yes	Extension
B56	PSRAM_CLK	External PSRAM	O	1.8V	PSRAM Clock	Leave open	Yes	Extension
B57	SF_nCS1 / PSRAM DQS	External FLASH for SF_nCS1 / External PSRAM for PSRAM DQS	O	1.8V	Serial Flash Chip Select 1 for SF_nCS1 / PSRAM DQS for PSRAM DQS	Leave open	Yes	Extension
B58	EJ_TCK	JTAG	I/O	1.8V	JTAG Test Clock	Leave open	Yes	Core
B59	EJ_TDO	JTAG	O	1.8V	JTAG Test Data Output / Serial Wire	Leave open	Yes	Core
B60	EJ_TRST	JTAG	I/O	1.8V	JTAG Test Reset	Leave open	Yes	Core
B61	EJ_TMS	JTAG	I/O	1.8V	JTAG Test Mode Select / Serial Wire Debug	Leave open	Yes	Core
B62	EJ_TDI	JTAG	I/O	1.8V	JTAG Test Data Input	Leave open	Yes	Core
B63	NC	Not connected			Not Connected	Leave open	No	Not Connected

Table 2-3: Ring B Pin Definitions (Continued)

Pin	Signal Name	Group	I/O	Voltage Supply Domain	Function	Unused Pins Recommendation	Isolate required[a]	CF3
B64	EJ_DEBUG_RST_N	JTAG	I/O	1.8V	Reset pin for the JTAG probe	Leave open	Yes	Core
BG1-4	GND	Ground	GND	Ground	Ground	Mandatory connection	No	Core

a. The host platform should isolate these signals during module Hibernate mode to prevent back-powering the module. For details, see 6.4: Hibernate—Isolation Requirements.
b. Pin can be assigned to either the internal MCU or Sensor Hub (SHUB).

3: Power Specifications

Note: If not specified, all electrical values are given for VBAT_BB and VBAT_RF = 3.7V, operating temperature of 25 °C. and with conducted 50Ω load on RF port(s).

3.1 Power Supply

The module is supplied through the VBAT_BB and VBAT_RF signals.

For standard applications, VBAT_BB and VBAT_RF must be tied externally to the same power supply. For some specific applications (e.g. applications requiring a lower VBAT_RF), the module supports separate VBAT_BB and VBAT_RF connection as per Table 3-1.

Table 3-1 and Table 3-2 describe the Power Supply interface.

Table 3-1: Power Supply Pin Description

Pin	Signal Name	I/O	Description
C63	VBAT_BB	PI	Power supply (baseband)
C61, C62	VBAT_RF	PI	Power supply (radio frequency)
C30, C32, C37, C39, C48, C50, CG1– CG4, G1–G16, B35, B37, B46, B48-50, BG1-4		GND	Ground

Caution: *Operation outside the minimum/maximum specified operating voltage (Table 3-2) is not recommended, and functional operation of the device and specified typical performance are neither implied nor guaranteed.*

Table 3-2: Power Supply Current Requirements

Parameter		Min	Typ	Max	Unit	Notes
VBAT_BB voltage		2.5	3.7	4.35	V	Must be within min/max values overall operating conditions (including voltage ripple, droop, and transient)
VBAT_RF voltage Full Specification		2.5	3.7	4.35	V	
VBAT_BB voltage Extended Range		2.2[a]	3.7	4.35	V	
Power Supply Ripple		-	-	100[b]	mVpp	
Max Supply Current	VBAT_BB	-	-	60	mA	
	VBAT_RF (LTE)	-	-	420	mA	

a. VBAT_BB from 2.2-2.5V is functional but the power source must be sufficient, and the impedance of power source / power path should be as low as possible to reduce the voltage drop. Note that operation in this range requires a separate VBAT_BB supply.
b. Measured at nominal supply voltage (3.7V), nominal ambient temperature (25 °C), and with conducted 50W load on RF port(s).

Note: The host power supply should be capable of supplying $VBAT\_BB_{max}$ + $VBAT\_RF_{max}$.

3.2 Electrical Specifications

3.2.1 Digital I/O Characteristics

The I/O characteristics for supported digital interfaces/signals are described in Table 3-3. These interfaces/signals include:

- UARTs
- GPIOs
- Clock output signals
- UIM1
- TX_ON
- External PA voltage control indicator
- I2C
- SPI

These signals are not available in Hibernate mode since VGPIO is OFF.

Note: The host platform should isolate these signals during module Hibernate mode to prevent back-powering the module. For details, see 6.4: Hibernate—Isolation Requirements.

Table 3-3: Digital I/O Electrical Characteristics (1.80V)[a]

Parameter	Description	Min	Max	Unit
V_{IH}	Logic High Input Voltage	0.7 × VGPIO	VGPIO	V
V_{IL}	Logic High Input Voltage	0	0.3 × VGPIO	V
V_{OH}	Logic High Input Voltage	0.8 × VGPIO		V
V_{OL}	Logic High Input Voltage		0.2 × VGPIO	V
I_O	Output Current	2	4	mA
IR_{PD}	Internal Pull-Down Resistor current	27	53	μA
IR_{PU}	Internal Pull-Up Resistor current	26	51	μA
R_{PU}	Internal Pull-Up Resistor	33	66	kΩ
R_{PD}	Internal Pull-Down Resistor	33	66	kΩ

a. VGPIO=1.8V (See 4.1: VGPIO.)

3.3 3GPP Power Saving Features

This section describes 3GPP power saving features (PSM, eDRX) that are supported by the HL7900/HL7900E module. Per 3GPP specifications, these features pertain to the module's cellular communication.

The HL7900/HL7900E also features low power modes that contribute to power savings by selectively limiting or turning off other elements of the module, such as memory states, I/O states, etc. (For details, see 3.4: HL7900/HL7900E Low Power Modes.)

3.3.1 Power Saving Mode (PSM)

Power Saving Mode (PSM) is a 3GPP feature that allows the Semtech HL7900/HL7900E to minimize power consumption by registering on a PSM-supporting LTE network and then entering PSM state for a configured duration.

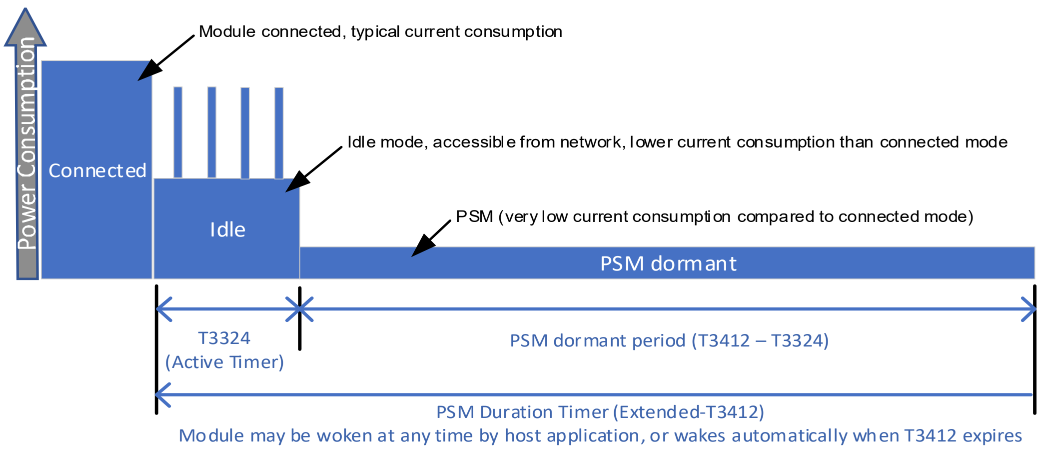


Figure 3-1: PSM—Timers

When the module enters the PSM state:

1. The module remains active (accessible from the network) in a lower-power idle state for a short period (T3324 Active Timer).
2. The module then drops to a very-low power 'dormant' state for the remainder of the PSM duration or until the host platform wakes the module to initiate a network contact. During this dormant period, the module is not accessible from the network.
3. After the module contacts the network (for either reason), the process repeats.

Using PSM, an HL7900/HL7900E-based host platform can reduce power consumption significantly because:

- It can enter a very low power state (TBD) during a very long PSM dormant period.
- The platform can wake the HL7900/HL7900E at any time to initiate data transaction immediately with minimal overhead (signaling/procedure) since the network keeps the module registered during the entire PSM period.

Typical candidates for PSM are systems (such as monitors and sensors) that:

- Require long battery life (low power consumption)
- Infrequently send mobile originated data (every few hours, days, weeks, etc.), with optional reply data from the network
- Tolerate modules being inaccessible for long periods of time
- Do not use mobile-terminated voice/data/SMS. If the host platform needs the module to be able to receive mobile-terminated data, eDRX is a more suitable option.

Figure 3-2 describes an example of a module operating in PSM. In a typical application, the module will always be woken from the dormant state to transmit data (illustrated in the 'Typical MO Use Case' portion of the figure). This is accomplished by setting the T3412 timer much longer than anticipated transmission frequency.

However, if the module is not woken by the host, a TAU will be sent when T3412 expires (illustrated in the 'Default PSM Use Case' portion of the figure). By setting the T3412 longer, unnecessary TAU transmissions can be avoided.

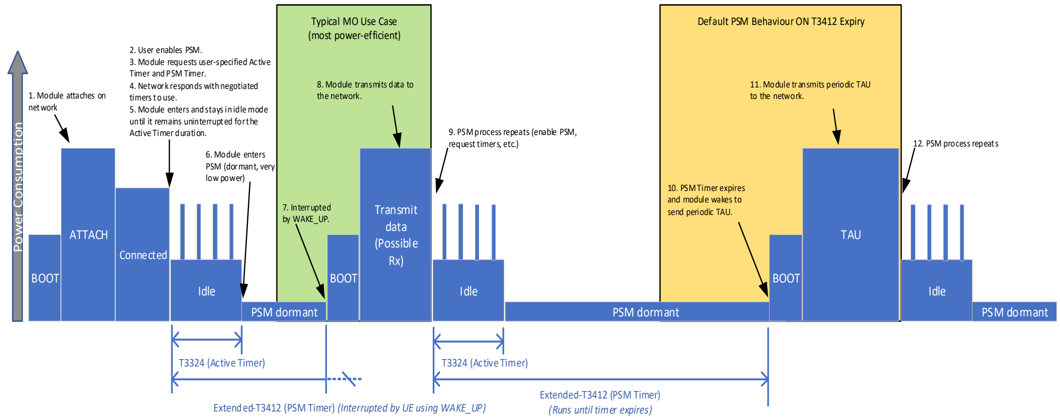


Figure 3-2: Power Saving Mode—Use Cases Example

3.3.2 Extended DRX (eDRX)

3.3.2.1 eDRX Overview

Extended Idle DRX (I-eDRX) is a 3GPP-specified extension of the Discontinuous Reception (DRX) low power consumption feature. This extension reduces the number of paging opportunities (PO) the module must monitor while in idle state, resulting in a corresponding decrease in power consumption.

Many data module applications are tolerant to delays in downlink data packets so extending the period between paging opportunities would allow for current consumption savings for these applications.

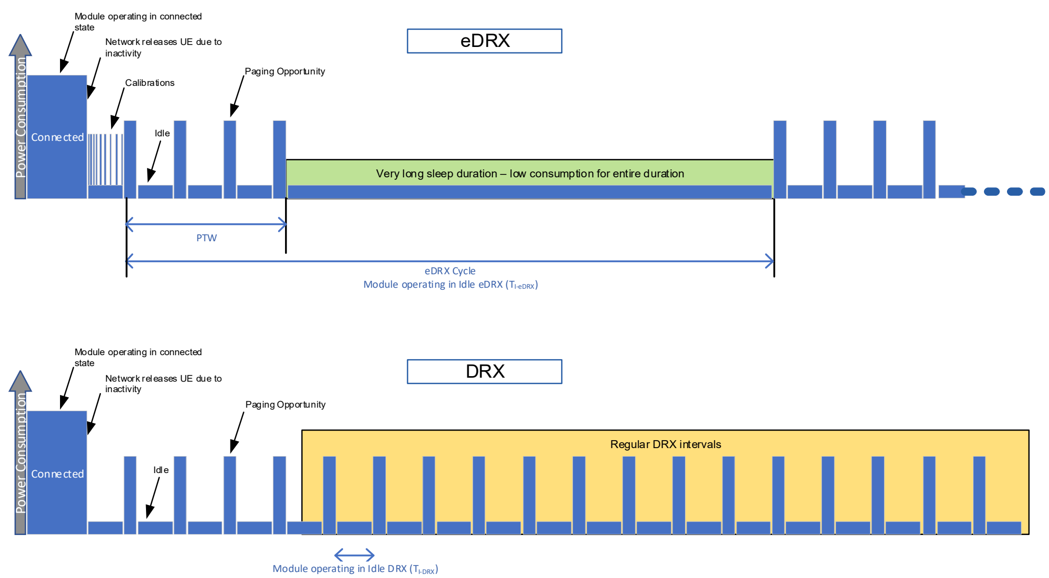


Figure 3-3: eDRX vs DRX

As shown in Figure 3-3, the HL7900/HL7900E supports eDRX, taking advantage of the feature by monitoring a set number of paging opportunities in a Paging Time Window (PTW) and then entering a low power state between PTWs. This sequence (PTW followed by low power state) comprises a single eDRX cycle. The size of the PTW and the length of the eDRX cycle (TI-eDRX) are negotiated between the module (which submits desired values when enabling eDRX) and the network (which indicates the values that will actually be used).

The module remains in I-eDRX until it detects a page from the network during a PO or needs to access the network (e.g. to make a data connection, send a mobility TAU or periodic TAU, etc.), at which time it returns to the connected state.

Note that for a short period of time immediately after the module is released from connected state by the network and enters idle state, it has a few extra short wake ups for clock calibration (shorter than a single PO). Figure 3-4 shows an eDRX power consumption profile with a periodic TAU event. Notice that after the TAU, the eDRX 81.92s cycle is restored slowly by several iterations from 10s to 20s then to 40s before reaching the 81.92s wake. This behavior is an HL7900/HL7900E design feature and cannot be modified.

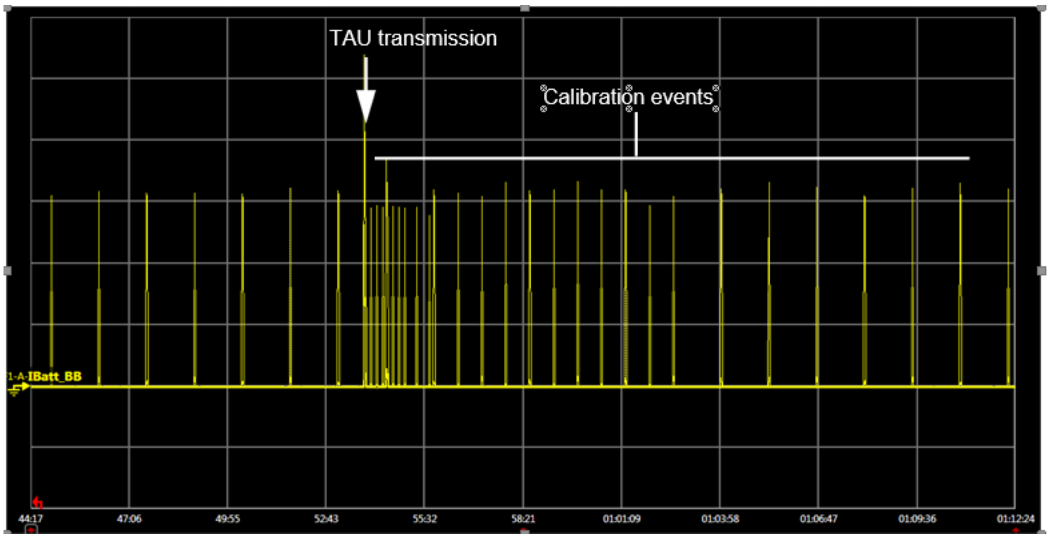


Figure 3-4: eDRX Power Consumption Profile Interruption

3.3.2.2 Configuring eDRX

Table 3-4 describes available methods for configuring eDRX.

Table 3-4: eDRX-Related Commands

AT Command	Description
AT+CEDRXS AT+KEDRXCFG	Enable/disable eDRX and configure related settings
AT+CEDRXRDP	Display current eDRX settings

For example:

- Use AT+CEDRXS to configure the desired TI-eDRX value.
- During the network attach or TAU process:
  - Module sends eDRX request with the settings (as specified in AT+CEDRXS) to the network.
  - Network response indicates if the module may use eDRX and the eDRX parameters that should be used. The network may adjust the eDRX parameters from those requested by the module.

- If eDRX is accepted by the network, the module only needs to monitor during the eDRX paging opportunities. The module may enter low power mode state between the eDRX paging opportunities (depending on the module configuration).

Note that:

- eDRX parameters must be carefully selected to match the intended use case(s) for the module.
  - Given that the module can only be paged at an eDRX paging opportunity:
  - Longer eDRX cycles will delay (increase the latency of) mobile terminated data reception.
  - Shorter eDRX cycles will reduce the latency but will also reduce the eDRX power savings.
  - Setting a cycle longer than 81.92s may not improve power saving significantly, since the module will wake every 81.92s to do a clock calibration.

  The duration of the eDRX cycle should be appropriately selected for the specific use case.
- Network-side store and forward is supported— Packets will be stored until the module's next eDRX paging opportunity or, if the network has a storage time limit, until that limit is reached.

3.3.2.3 Concurrent PSM and eDRX

eDRX may be performed during the Active Timer (T3324) window of PSM. For example, if PSM and eDRX are configured with the following settings:

- PSM:
  - T3412 (PSM Timer)— 86400s (24 hours)
  - T3324 (Active Timer)— 327.68s (~5.5 minutes)
- eDRX:
  - eDRX cycle time— 81.92s

Assuming the network does not attempt to contact the module after the module leaves the connected state and enters PSM idle state, the module will stay in the idle state for 327.68 seconds (the Active Timer).

While in the idle state, the module will be in eDRX power saving mode for 4 cycles of 81.92 seconds each, and then go to PSM dormant state for ~23h55m until the T3412 timer expires. At that point the module wakes, sends a periodic TAU, and then the PSM process repeats.

3.4 HL7900/HL7900E Low Power Modes

In addition to the 3GPP power saving features 3.3.1: Power Saving Mode (PSM) and 3.3.2: Extended DRX (eDRX), the HL7900/HL7900E supports the low power modes in Table 3-5.

Table 3-5: Low Power Modes

Power Mode	Possible Modem State	Impact on Module	Hardware Wake-Up Signal Sources
Sleep	Stack OFF, DRX, eDRX, PSM, No service	▪ 26 MHz system clock is OFF ▪ Application processor is idle ▪ Modem is out-of-coverage, sleeping, or off ▪ I/Os are retained	WAKEUP UART1_DTR[a] RTC alarm event
Lite Hibernate	Stack OFF, eDRX, PSM, No service	▪ 26 MHz system clock is OFF ▪ Application processor is OFF ▪ Modem is out-of-coverage, sleeping, or off ▪ Flash memory and most RAM is off (some retention memory remains on) ▪ I/Os are retained	WAKEUP UART1_DTR[a] RTC timeout interrupt

Table 3-5: Low Power Modes (Continued)

Power Mode	Possible Modem State	Impact on Module	Hardware Wake-Up Signal Sources
Hibernate	Stack OFF, eDRX, PSM, No service	▪ 26 MHz system clock is OFF ▪ Application processor is OFF ▪ Modem is OFF ▪ Flash memory and most RAM is off (some retention memory may remain on, PSM/eDRX-dependent) ▪ I/Os are not retained (e.g. in an undefined state)	WAKEUP RTC timeout interrupt
OFF	Stack OFF	▪ 26 MHz system clock is OFF & RTC clock is OFF ▪ Application processor is OFF ▪ Modem is OFF ▪ Flash memory and RAM off ▪ I/Os are not retained (e.g. in an undefined state)	WAKEUP

a. Only if configured with +KSLEEP <mngt> parameter set to 0

3.5 Current Consumption

This section describes the HL7900/HL7900E module's current consumption under various power states/modes.

- Low Power Current Consumption Modes— Table 3-6 to Table 3-7
- Connected Mode— Table 3-8 to Table 3-10

Important: *The current consumption ranges listed in Table 3-6 to Table 3-10 are preliminary typical values based on the projected distribution of initial test modules. Values that fall outside these ranges are to be expected. This document will be updated with final values based on the chipset vendor power distribution when available—make sure to refer to the latest version (available at source.sierrawireless.com/resources/airprime/hardware_specs_user_guides/hl7900-product-technical-specification/).*

Important: *The module's current consumption will depend on the actual operating/environmental conditions of the customer platform. The current consumption measurements presented in this section (Table 3-6 to Table 3-10) are typical values obtained under the following test conditions:*

- *Nominal supply voltage—3.7V, TX power—0 dBm*
- *Nominal ambient temperature—25°C*
- *PSM connect type (call box equipment setting)—test mode*
- *eDRX test conditions:*
  - *Cat-M1 eDRX paging cycle—1.28 sec*
  - *Cat-NB eDRX paging cycle—2.56 sec*
- *Conducted 50Ω load on RF port(s)*
- *External UICC/USIM that can be activated*

- *In addition, the following conditions apply to Hibernate and OFF mode measurements:*
  - *VGPIO is OFF*
  - *Customer platform ensures module I/Os are **not** driven > 0.2V*
  - *External UICC/USIM that is pre-configured to allow the module to automatically disable the USIM power.*
  - *WAKEUP signal Low*

Note: To be able to enter PSM mode when the module's lowest attainable power state is Lite Hibernate or Hibernate (i.e., +KSLEEP <level> is 1 or 2) and LwM2M is enabled (AutoConnect is enabled by default), the host must not de-assert the WAKEUP pin until it receives a CEREG:4 unsolicited result code.

Table 3-6: LPM Current Consumption — Cat-M1[a][b]

Modem Radio State	Lowest Power Mode	Details	Typ[c]		Unit
			HL7900	HL7900E	
OFF	OFF	▪ Module is switched off by AT command (+CPWROFF) ▪ Power supplies (VBAT_BB, VBAT_RF) are connected	1.2–1.8	1.2–1.8	µA
PSM		TAU—Occurrence is network dependent	23–28	23–28	µAh
	Hibernate	Floor current during PSM dormant	1.1–1.5	1.1–1.7	µA
	Lite Hibernate		5–7	21–24	µA
	Hibernate Cycle[d]	▪ T3412 = 24h ▪ T3324 = 20s	1.8–2.3	2.6–2.8	µA
	Lite Hibernate Cycle[d]		5–7	22–25	µA
	Hibernate Cycle[d]	▪ T3412 = 1h ▪ T3324 = 20s	11–20	37–40	µA
	Lite Hibernate Cycle[d]		23–26	46–52	µA
eDRX[e]		Calibration—Applies to eDRX 81.92s and longer	1.4–12	1.4–12	µAh
	Hibernate	Floor current during eDRX	3–6	11–14	µA
	Lite Hibernate		8–11	21–24	µA
	Hibernate Cycle[d]	▪ eDRX cycle ($T_{I\text{-}eDRX}$) = 81.92s ▪ PTW and DRX = 1.28s	5–8	20–22	µA
	Lite Hibernate Cycle[d]		10–13	29–33	µA
	Hibernate Cycle[d]	▪ eDRX cycle ($T_{I\text{-}eDRX}$) = 20.48s ▪ PTW and DRX = 1.28s	15–20	45–49	µA
	Lite Hibernate Cycle[d]		20–25	54–59	µA
DRX	Sleep	1.28s	2.8–3.8	3.5–3.8	mA
	Hibernate		0.28–0.36	0.64–0.66	mA
	Sleep	2.56s	3–5	3.3–3.7	mA
	Hibernate		0.18–0.26	0.37–0.39	mA
	Running	DRX independent, +KSLEEP=2 or Wake active	9–13	11–12	mA
Standby		Module registered, Idle mode, without TX power / data transfer	7–10	7–15	mA

a. Preliminary values, subject to change
b. Values measured under following conditions:
- Good channel conditions (SINR > 5 dB)
- Static scenario
c. Nominal supply voltage 3.7V, Tx Pwr=0 dBm; Nominal ambient temperature 25°C. For full test condition details, refer to the Important note on page 34.

d. Cycle (Lite Hibernate or Hibernate) includes boot, cell acquisition, network attach, wait for timer expiry, and back to Sleep
e. See 3.3.2: Extended DRX (eDRX) for details. System stabilizes after a wait time of 20–30 minutes.

Table 3-7: LPM Current Consumption — NB[a,b]

Modem Radio State	Lowest Power Mode	Details	Typ[c]		Unit
		▪	HL7900	HL7900E	
OFF	OFF	▪ Module is switched off by AT command. ▪ Power supplies (VBAT_BB, VBAT_RF) are connected.	1.2–1.8	1.2–1.8	µA
PSM		TAU—Occurrence is network dependent	22–28	22–28	µAh
	Hibernate	Floor current during PSM dormant	1.2–1.5	1.1-1.4	µA
	Lite Hibernate		5–7	21–24	µA
	Hibernate Cycle[d]	▪ T3412 = 24 h ▪ T3324 = 20 s	2.2–2.5	2.6–2.8	µA
	Lite Hibernate Cycle[d]		6.4–7.8	22–25	µA
	Hibernate Cycle[d]	▪ T3412 = 1 h ▪ T3324 = 20 s	26–33	37–39	µA
	Lite Hibernate Cycle[d]		27–35	46–52	µA
eDRX[e]		Calibration—Applies to eDRX 81.92 s and longer	1.4–19	1.4–19	µAh
	Hibernate	Floor current during eDRX	2.5–4	11–14	µA
	Lite Hibernate		8–11	21–24	µA
	Hibernate Cycle[d]	▪ eDRX cycle ($T_{I\text{-}eDRX}$) = 81.92 s ▪ PTW and DRX = 2.56 s	9.5–13	24–27	µA
	Lite Hibernate Cycle[d]		10–16	33–37	µA
	Hibernate Cycle[d]	▪ eDRX cycle ($T_{I\text{-}eDRX}$) = 20.48 s ▪ PTW and DRX = 2.56 s	30–38	63–67	µA
	Lite Hibernate Cycle[d]		36–40	71–77	µA
DRX	Sleep	1.28 s	3–4.2	3.7–4	mA
	Hibernate		0.5–0.8	0.92–0.96	mA
	Sleep	2.56 s	2.7–3.7	3.4–3.7	mA
	Hibernate		0.3–0.5	0.51–0.53	mA
	Sleep	10.24 s	2.5–3.5	3.2–3.6	mA
	Hibernate		0.15–0.25	0.2–0.22	mA
	Running	DRX independent, +KSLEEP=2 or Wake active	11–14	12–14	mA
Standby		Module registered, Idle mode, without TX power/data transfer	7–10	7–15	mA

a. Preliminary values, subject to change
b. Values measured under following conditions:
- Good channel conditions (SINR > 5 dB)
- Static scenario
c. Nominal supply voltage 3.7 V, Tx Pwr=0 dBm; Nominal ambient temperature 25°C. For full test condition details, refer to the Important note on page 34.

d. Cycle (Lite Hibernate or Hibernate) includes boot, cell acquisition, network attach, wait for timer expiry, and back to Sleep
e. See 3.3.2: Extended DRX (eDRX) for details. System stabilizes after a wait time of 20~30 minutes.

Table 3-8: HL7900/HL7900E Current Consumption — LTE Cat-M1 Connected Mode[a]

Parameter	Band	Output Power	Avg Current (Typical Values)[b][c]
LTE Cat-M1 ▪ Modem State: Connected ▪ 4 RB DL at MCS 14 1 RB UL at MCS 15 ▪ Maximum 3 UL sub-frames and 3 DL sub-frames every 10 ms ▪ Transferring UDP payload data rates: concurrent 280 kbps DL + 45 kbps UL	1, 2, 3, 4, 5, 8,12,13,18, 19, 20, 25, 26, 28, 66	23 dBm	110–170 mA
		0 dBm	30–70 mA

a. Preliminary values, subject to change
b. Ranges reflect variations between band/channel combinations
c. Nominal supply voltage 3.7V, Tx Pwr=0 dBm; Nominal ambient temperature 25°C. For full test condition details, refer to the Important note on page 34.

Table 3-9: HL7900/HL7900E Current Consumption — LTE NB-1 Connected Mode[a]

Parameter	Bands	Output Power	Avg Current (Typical Values)[b]
NB1 DL peak throughput (27.2 kbps) UL Subcarrier spacing: 15 kHz Subcarriers downlink: 12 MCS.TBS:13	1, 2, 3, 4, 5, 8, 12, 13, 18, 19, 20, 25, 26, 28, 65, 66, 70, 85	23 dBm	40–70 mA
		0 dBm	20–50 mA
NB1 UL peak throughput (62.5 kbps) UL Subcarrier spacing: 15 kHz Subcarriers uplink:3 MCS.TBS:13		23 dBm	70–110 mA
		0 dBm	20–50 mA

a. Preliminary values, subject to change
b. Nominal supply voltage 3.7V, Tx Pwr=0 dBm; Nominal ambient temperature 25°C. For full test condition details, refer to the Important note on page 34.

Table 3-10: HL7900/HL7900E Current Consumption — LTE NB-2 Connected Mode[a]

Parameter	Bands	Output Power	Avg Current (Typical Values)[b]
NB2 DL peak throughput (127 kbps) UL Subcarrier spacing: 15 kHz Subcarriers downlink: 12 MCS.TBS:13	1, 2, 3, 4, 5, 8, 12, 13, 18, 19, 20, 25, 26, 28, 65, 66, 70, 85	23 dBm	70–120 mA
		0 dBm	25–60 mA
NB2 UL peak throughput (158 kbps) UL Subcarrier spacing: 15 kHz Subcarriers uplink:12 MCS.TBS:13		23 dBm	180–260 mA
		0 dBm	35–100 mA

a. Preliminary values, subject to change
b. Nominal supply voltage 3.7V, Tx Pwr=0 dBm; Nominal ambient temperature 25°C. For full test condition details, refer to the Important note on page 34.

4: Detailed Interface Specifications

This chapter describes the interfaces supported by the Semtech HL7900/HL7900E and provides specific voltage, timing, and circuit recommendations for those interfaces, as appropriate

Note: GNSS, SRD, and Wi-Fi functions are not supported on the HL7900E.

4.1 VGPIO

The VGPIO (GPIO voltage output) 1.8 V supply state is:
- ON (available)— Voltage output is high when module is in Active, Sleep, or Lite Hibernate mode
- OFF (not available)— Voltage output is low when module is in OFF, Reset, or Hibernate mode

VGPIO can be used to:
- Pull-up signals such as I/Os. For additional details, see 4.1.1: I/O Behavior in Hibernate Mode.
- Supply LED drivers
- Indicate the module power state
- Control buffering of module I/O (required in Hibernate)

Table 4-1 and Table 4-2 describe the VGPIO supply.

Table 4-1: VGPIO Pin Description

Pin	Signal Name	I/O[a]	Description
C45	VGPIO	PO	GPIO voltage supply

a. Signal direction with respect to the module

Refer to the following table for the electrical characteristics of the VGPIO supply.

Table 4-2: VGPIO Electrical Characteristics

Parameter		Min	Typ	Max	Unit	Remarks
Voltage level		1.75	1.8	1.85	V	Applies to Active, Sleep, and Lite Hibernate modes
Current capability	Active, Sleep	–	–	50	mA	Total current supplied by VGPIO should not exceed 25 mA.
	Lite Hibernate	–	–	TBD	mA	
Output capacitance		–	–	1	µF	External decoupling capacitance should not exceed 1 µF.

4.1.1 I/O Behavior in Hibernate Mode

The following behaviors apply, only in Hibernate mode, to I/Os that are referenced to VGPIO (i.e. UART, GPIO, Clock, UIM1, Indication, and ADC signal groups— see Table 2-2); they do not apply in Lite Hibernate or Sleep modes.
- VGPIO is OFF (voltage output is low)

Note: The host platform should isolate these signals during module Hibernate mode to prevent back-powering the module. For details, see 6.4: Hibernate—Isolation Requirements.

- No I/O should be biased as no internal source exists. The maximum allowed voltage is ±0.2V at any I/O.
- All I/Os that are referenced to VGPIO will be in an undefined state.

The host should ignore all activity on these signals until the module has initialized and reached AT-READY state (i.e. when UART1_CTS transitions from high to low (and stays low) and VGPIO is high). For timing details, see 4.5.1: Unmanaged POWER_ON_N (Default) and 4.11.1: Wakeup from Low Power Modes.

4.2 USIM Interface

The HL7900/HL7900E implements a USIM interface that can be used to control either:

- the module's eSIM (internal, embedded SIM—optional and SKU-dependent)
  or
- an external 1.8V USIM (UIM1); 3V USIM is not supported

To associate USIM1 with the eSIM or external USIM, use the AT+KSIMSEL command.

4.2.1 eSIM Interface (SKU-specific)

eSIM is an internal interface supporting Sierra Smart Connectivity. For details about using the HL7900's eSIM with Sierra Smart Connectivity, refer to Semtech Ready-to- Connect Module Integration Guide. For additional information on Sierra Smart Connectivity, explore www.sierrawireless.com or contact Semtech.

4.2.2 External UIM1 Interface

The USIM1 interface is fully compliant with GSM 11.11 recommendations concerning USIM functions.

Table 4-3 describes the USIM1 interface.

Table 4-3: UIM1 Pin Description

Pin	Signal Name	I/O[a]	Description	Voltage Supply Domain
C26	UIM1_VCC	PO	USIM1 Power supply	1.8V
C27	UIM1_CLK	O	USIM1 Clock	1.8V (VGPIO)
C28	UIM1_DATA	I/O	USIM1 Data	1.8V (VGPIO)
C29	UIM1_RESET	O	USIM1 Reset	1.8V (VGPIO)
C64	UIM1_DET[b]	I	USIM1 Detection	1.8V (VGPIO)

a. Signal direction with respect to the module
b. Buffer is required if UIM_DET1 is powered from host; not required if powered from VGPIO. UIM1_DET can be used as GPIO3 if external SIM is not required.

Note: UIM1_VCC max output current is 50 mA in Active and Sleep modes, TBD in Lite Hibernate, and Off in Hibernate. For UIM1 electrical interface details, see UIM1.

4.2.3 UIM1_DET

UIM1_DET is used to detect the insertion or removal of a USIM in the USIM socket connected to the main USIM interface (UIM1).

When a USIM is:

- Inserted— UIM1_DET is HIGH.
- Removed— UIM1_DET is LOW.

Note: In Hibernate mode, UIM1_DET is in an undefined state. It is not recommended to connect a high level voltage to UIM1_DET when the module is in Hibernate mode, it is recommended to connect UIM1_DET to VGPIO when USIM is inserted. GPIO3 must remain configured as input with pull-down when used as UIM1_DET. This configuration cannot be changed.

4.3 General Purpose Input/Output (GPIO)

The HL7900/HL7900E provides several GPIOs, some of which are multiplexed with other signals, as described in Table 4-4. For electrical specifications, see Table 3-3.

Table 4-4: GPIO Pin Descriptions

Pin	Signal Name	Alternate Function	I/O	Default State[a]	Voltage Supply Domain
C1	GPIO1	I2C_SCL	I/O	Input Pull-down	1.8V (VGPIO)
C10	GPIO2	Alternative default Ring Indicator (Active High Output)	I/O	Input Pull-down	1.8V (VGPIO)
C40	GPIO7	Module activity indicator	I/O	Input Pull-down	1.8V (VGPIO)
C41[b]	GPIO8	VBAT_PA_EN (Output)	I/O	Input Pull-down	1.8V (VGPIO)
C46	GPIO6	–	I/O	Input Pull-down	1.8V (VGPIO)
C51	GPIO14	UART3_CTS (Output) / SPIM_EN0 (Output)	I/O	Input Pull-down	1.8V (VGPIO)
C52	GPIO10	UART3_TX (Input) / SPIM_MOSI (Output)	I/O	Input Pull-down	1.8V (VGPIO)
C53	GPIO11	UART3_RTS (Input) / SPIM_MISO (Input)	I/O	Input Pull-down	1.8V (VGPIO)
C54	GPIO15	UART3_RX (Output) / SPIM_CLK (Output)	I/O	Input Pull-down	1.8V (VGPIO)
C64	GPIO3	UIM1_DET (Input)	I/O	Input Pull-down	1.8V (VGPIO)
C65	GPIO4	–	I/O	Input Pull-down	1.8V (VGPIO)
C66	GPIO5	I2C_SDA	I/O	Input Pull-down	1.8V (VGPIO)
B11	GPIO47	–	I/O	Input Pull-down	1.8V
B24	GPIO46	–	I/O	Input Pull-down	1.8V

a. Default state is software-controlled when module has initialized and reached AT-READY state. Default state is configurable by customer using AT+KGPIOCFG command.
b. The default function is VBAT_PA_EN for C41. Contact Semtech to enable the GPIO function.

Table 4-4 notes the default state for each signal.

By default, at power up, all GPIOs are configured as inputs. During power up, power down, reset and Hibernate, the signals are in an undefined state. Therefore, the host should ignore all activity on I/Os until the module has reached AT-READY state (i.e. when UART1_CTS transitions from high to low (and stays low) and VGPIO is high). For timing details, see 4.5.1: Unmanaged POWER_ON_N (Default) and 4.11: Wake Up Signal (WAKEUP).

4.3.1 GPIO7 Usage

The GPIO7 can be set as a module activity indicator via AT commands AT+KGPIOCFG or AT+KGPIO. For details, refer to HL7900 AT Command Reference Guide . When set as a module activity indicator, the GPIO7 will indicate High activity once the module is active. Power IC levels can be controlled using GPIO7 to initiate power saving methods. Note that power saving methods may also be affected by the overall hardware schematic design.

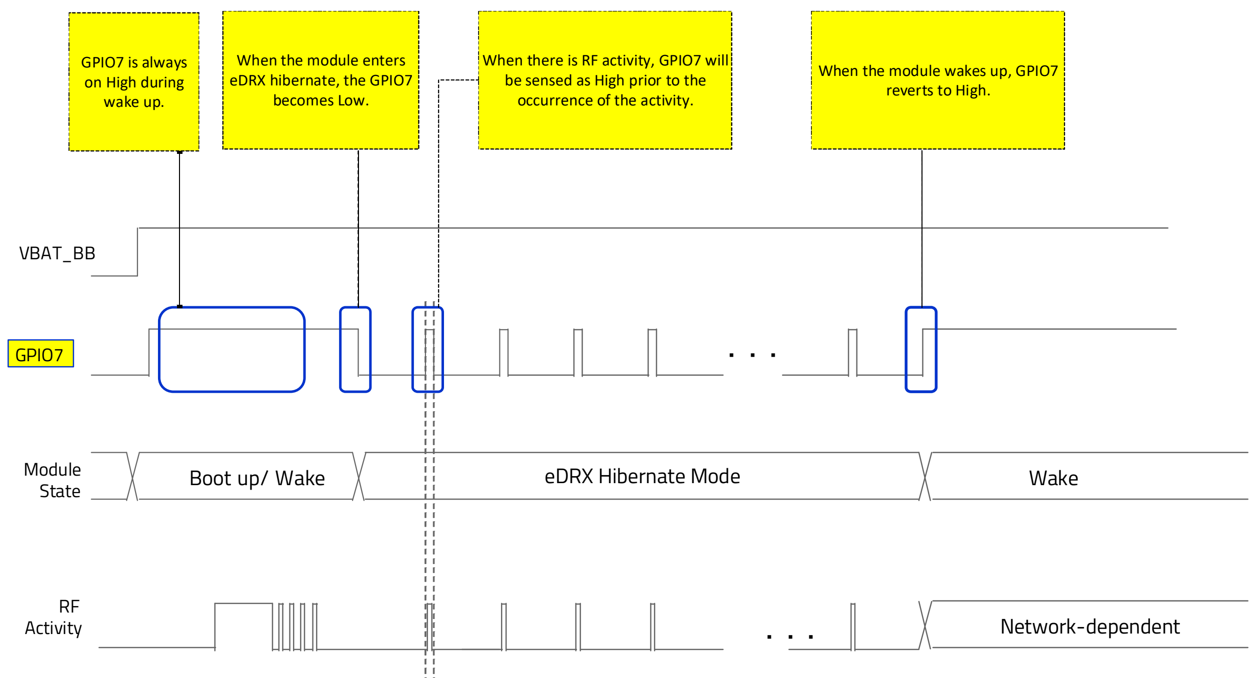


Figure 4-1: GPIO7 Waveform Behavior

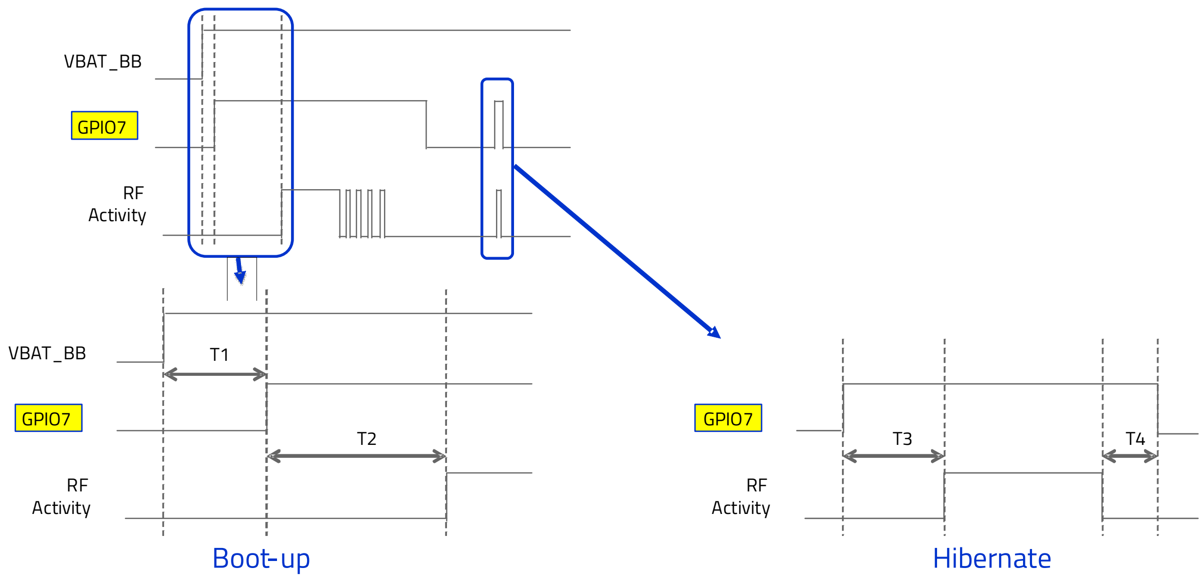


Figure 4-2: GPIO7 Waveform—Boot up and Hibernate mode

Table 4-5: GPIO7 Timing for Boot up and Hibernate Mode

Parameter	Description	Min	Max	Unit
T1	Delay between VBAT_BB and GPIO7	0.9	2	ms
T2	Delay between GPIO7 and RF activity	3	6	s
T3_eDRX	Delay between GPIO7 and RF activity under eDRX	7	10	ms
T3_PSM	Delay between GPIO7 and RF activity under PSM	370	600	ms
T4_eDRX	Delay between RF activity and GPIO7 under eDRX	14	24	ms
T4_PSM	Delay between RF activity and GPIO7 under PSM (wake up by TAU)	54	84	ms

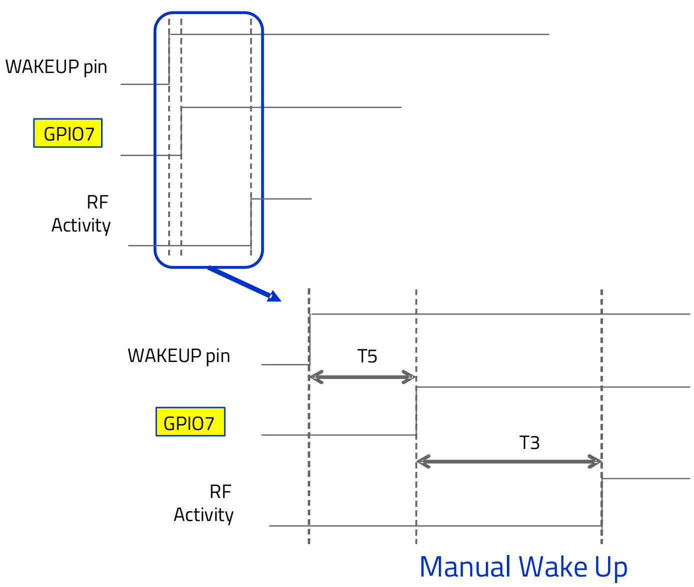


Figure 4-3: GPIO7 Waveform—Manual Wake Up

Table 4-6: GPIO7 Timing for Manual Wake Up

Parameter	Description	Min	Max
T5_eDRX	High during wake up state	0.22 ms	0.385 ms
T5_PSM		0.22 ms	0.385 ms

4.4 Main Serial Link (UART1)

The HL7900/HL7900E implements the UART1 serial interface (up to 921.6 kbps, default rate of 115.2 kbps) for communication between the module and a PC or host processor. UART1 consists of a flexible, 8-wire asynchronous serial, 1.8V interface that complies with RS- 232 interface. UART1 can also be used to upgrade the module firmware locally.

Note: The host platform may use UART1 as an 8-wire, 4-wire, or 2-wire interface as shown in Figure 4-4, Figure 4-5, and Figure 4-6.

Note that in Hibernate mode the host platform (MCU) interfaces can remain powered— it is important that the host interfaces do not back-power the module.

The UART1 interface is not active during Hibernate mode, so the host should ignore all activity on UART1 during Hibernate. If the module will enter Hibernate mode, Semtech recommends adding buffer circuits to ensure UART signals are not driven high (i.e. >0.2V).

Note that a buffer is not required in Lite Hibernate mode. For detailed information, refer to 4.1.1: I/O Behavior in Hibernate Mode.

Table 4-7 describes the UART1 interface.

Table 4-7: UART1 Pin Description

Pin	Signal Name[a]	Default State[b,c]	Active	Voltage Supply Domain	Description
C2	UART1_RI	Output	L	1.8V (VGPIO)	Ring Indicator Data reception, SMS, etc.
C3	UART1_RTS	Input with Hi-Z	L	1.8V (VGPIO)	Request To Send
C4	UART1_CTS	Output	L	1.8V (VGPIO)	Clear To Send[d] The module is ready to receive AT commands.
C5[e]	UART1_TX	Input with Hi-Z	-	1.8V (VGPIO)	Transmit data
C6[e]	UART1_RX	Output	-	1.8V (VGPIO)	Receive data
C7	UART1_DTR	Input with pull-up	L	1.8V (VGPIO)	Data Terminal Ready[f]
C8	UART1_DCD	Output	L	1.8V (VGPIO)	Data Carrier Detect Signal data connection in progress
C9	UART1_DSR	Output	L	1.8V (VGPIO)	Data Set Ready Signal UART interface is ON

a. Signals are named with respect to the host device (i.e. DTE (Data Terminal Equipment) convention—PC view). For example, UART1_RX is the signal used by the host to receive data from the module.
b. Signal direction with respect to the module. For example, UART1_RX is an output from the module to the host.
c. Default state is software-controlled when module has initialized and reached AT-READY state.

d. Host can monitor UART1_CTS and VGPIO to determine when the module is ready to receive AT commands (AT-READY). The UART1 interface is not active during Hibernate mode, so the host should ignore all activity on UART1_CTS during Hibernate.
e. Pull-up resistor is needed for UART1_RX pin, recommend reserve pull-up resistor design on UART1_TX also. the pull-up resistor value(10kohm – 100k ohm) will depend on customer's circuit design.
f. UART1_DTR has software-controlled pull-up (PU) (if enabled by using AT+KSLEEP with the <mngt> parameter set to 0), which is active only when module has initialized and reached AT-READY state. When the signal is low, the module wakes in all operational modes except Hibernate.

Note: If possible, it is highly recommended to add 0Ω on every line on the host platform to help the debug process. This will force the UART signal layout to the top PCB layer and allow access to the signal on the resistors.

4.4.1 Ring Indicator (UART1_RI or Alternative)

UART1_RI is an active-low output signal that indicates incoming events (e.g. SMS, data reception, etc.).

The signal is available in all power modes except Hibernate mode. In Hibernate mode, the UART_RI signal is in an undefined state.

Therefore, if a customer platform requires a RI signal to wake its host processor on SMS or IP reception, an alternative signal must be used.

The AT+KRIC command can configure GPIO2 (by default) as an inverted RI signal (RI_inverse_gpio).

Note: Because GPIO2 is in an undefined state while in (and exiting) Hibernate, use the following recommendations when GPIO2 is used as an RI signal: If firmware is used, enable the internal PD on GPIO2 using AT+KRIC (default state is No Pull).

4.4.2 UART1_RTS/UART1_CTS

UART1_RTS (Request to Send) is an active-low input signal used for module flow control (in combination with UART1_CTS).

By default, the UART1_RTS signal state is software-controlled as pull-down, and the host platform must drive this signal. The signal can be configured as a pull-up using the AT+KHWIOCFG command.

4.4.3 UART Application Examples

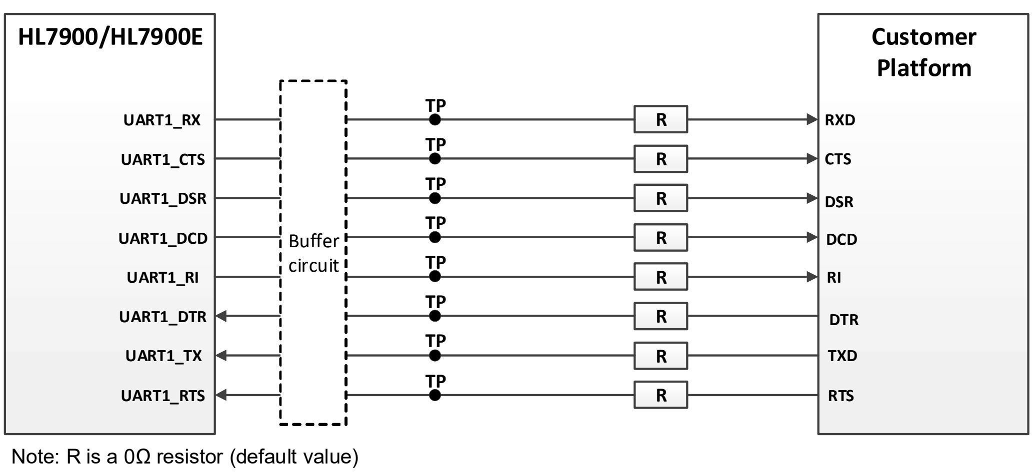
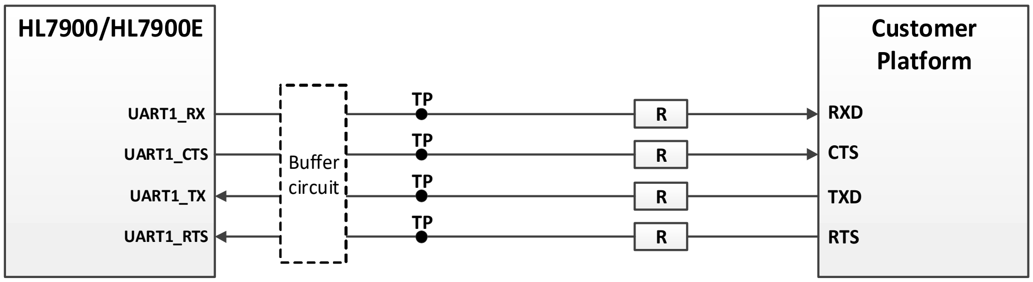
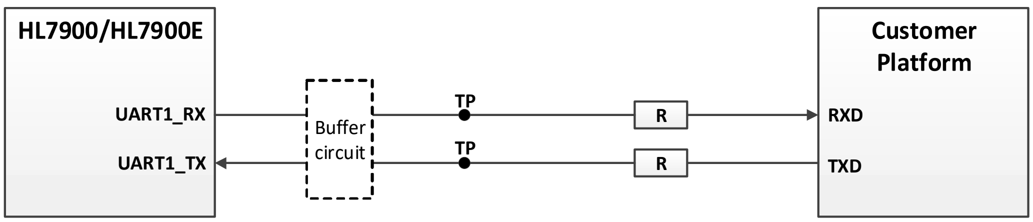


Figure 4-4: 8-wire UART Application Example



Note: R is a 0Ω resistor (default value)

Figure 4-5: 4-wire UART Application Example



Note: R is a 0Ω resistor (default value)

Figure 4-6: 2-wire UART Application Example

Note:

- *2-wire UART (Figure 4-6) is not recommended for higher baud rates (over 115200 bps).*
- *All UART signals operate at 1.8V. A voltage level shifter is required when connecting to a 3.3 V domain.*

4.5 Power On Signal (POWER_ON_N)

The signal is internally biased high by default. Bias voltage is dependent on the module mode— 0.8–1 V in Active or Sleep mode, and 0.6–0.8 V in Hibernate or Lite Hibernate mode.

The module has only one operational mode:

- Unmanaged— The module starts regardless of the POWER_ON_N state. In this mode, the POWER_ON_N signal must be left open.

Table 4-8 and Table 4-9 describe the POWER_ON_N signal.

Table 4-8: POWER_ON_N Pin Description

Pin	Signal Name	I/O[a]	Description
C59	POWER_ON_N	I	Power-on pin for unmanaged mode. Must be kept open.

a. Signal direction with respect to the module

Table 4-9: POWER_ON_N Electrical Characteristics

Parameter	Min	Typ	Max	Unit
Input Voltage-Low (v)	–	–	0.3	V

To ensure safe power on, the module VBAT (VBAT_BB/VBAT_RF) must be discharged below 0.3V before re-applying VBAT power.

4.5.1 Unmanaged POWER_ON_N (Default)

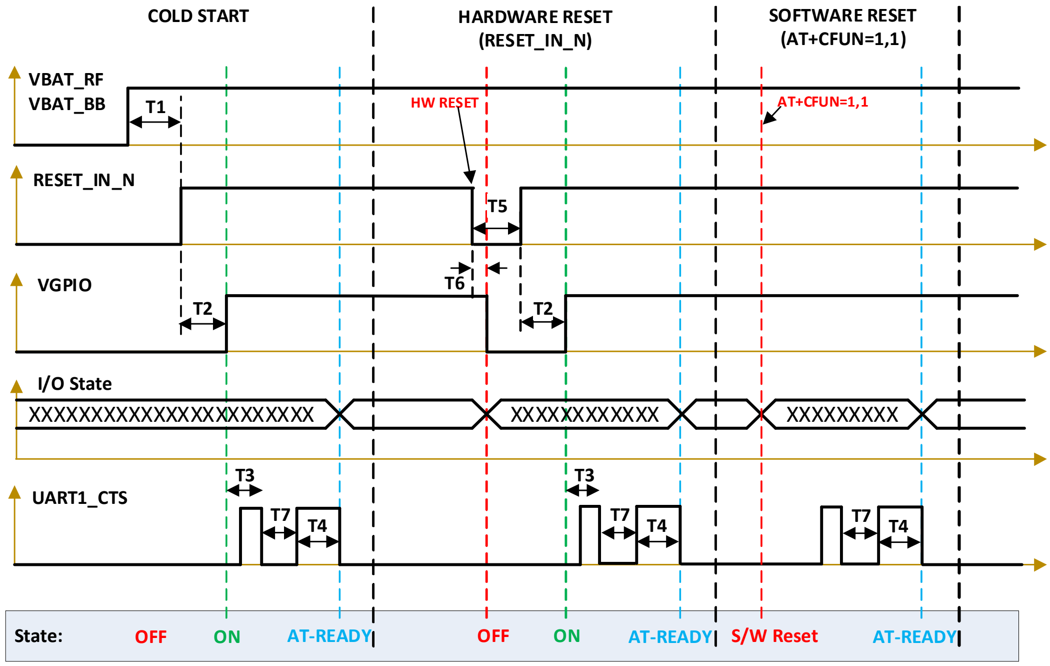


Figure 4-7: Power On and Reset Sequence (unmanaged POWER_ON_N)

Important: *At completion of T4, the module is ready to receive AT commands ('AT-READY') via UART1.*

Table 4-10: POWER_ON_N Timing (unmanaged)[a]

Parameter	Min	Typ	Max[b]	Unit
T1: Delay between VBAT_BB and RESET_IN_N	–	–	30	ms
T2: Delay between RESET_IN_N and VGPIO	–	–	3	ms
T3: Delay between VGPIO and UART1_CTS	–	–	3.2	s
T4: Delay	–	–	5	s
T5: HW RESET_IN_N assertion time	10	–	–	ms
T6: Off delay between VGPIO and RESET_IN_N	–	–	63	µs
T7: uboot delay	–	2	–	s

a. Timing of first power cycle after FOTA/FW upgrade is not captured in this table.
b. Measurements taken with HL78xx Development Kit

4.6 Power Down, Off, and VBAT Removal

4.6.1 Software Power Off in Unmanaged Mode

To power down the module via software:

1. Initiate the power down process:
   a. Disable sleep mode:
      AT+KSLEEP=2
      OK
   b. Set WAKEUP low.
   c. Stop SIM processes:
      AT+CFUN=0
      OK
   d. Use the +CPWROFF command:
      AT+CPWROFF
      OK
2. Monitor VGPIO— When VGPIO is low (e.g. < 0.2 V), the module is in OFF mode. (Note— The module can be woken from OFF mode by setting WAKEUP high. For timing details, see 4.11: Wake Up Signal (WAKEUP)
3. It is now safe to remove power (VBAT_BB and VBAT_RF) from the module.

Note: While the module is in OFF mode, the host platform (MCU) interfaces can remain powered. To prevent these signals from back-powering the module, the host platform should make sure to isolate them—the signals should not be driven high (i.e. > 0.2 V).

If the module is back-powered, the VGPIO low value will be higher (e.g. 0.8–1.1 V).

4.6.2 Emergency Power Removal

The Software Power Off in Unmanaged Mode procedure (which uses AT commands) should be used to safely power down the module.

However, if the module's UART interfaces cannot be accessed, or are unresponsive (i.e. do not respond after an AT command is issued, the following procedure can be used to power down the module, if necessary.

Important: *This procedure should be used with caution. If the module is interrupted while processing certain AT commands or performing a firmware upgrade, or the procedure is not followed correctly, the module may become unusable.*

1. Set RESET_IN_N low, and keep it asserted.
2. Monitor VGPIO- When VGPIO is low (e.g. < 0.2 V), the module is powered down.
3. Remove VBAT (both VBAT_BB and VBAT_RF) power.
4. Monitor VBAT- When VBAT is discharged below 0.3V, de-assert RESET_IN_N.

Note: :To power up the module, it is critical that VBAT be fully discharged (or below 0.3V) and that RESET_IN_N must be de-asserted. For details, refer to 4.5.1: Unmanaged POWER_ON_N (Default).

While the module is in OFF mode, the host platform (MCU) interfaces can remain powered. To prevent these signals from back-powering the module, the host platform should make sure to isolate them-the signals should not be driven high (i.e. > 0.2 V).

If the module is back-powered, the VGPIO low value will be higher (e.g. 0.8–1.1 V).

4.7 Reset Signal (RESET_IN_N)

The RESET_IN_N hardware control signal can be used to reset the module in any power state.

To reset the module, assert RESET_IN_N low for 10 ms (minimum)—this action immediately resets the module. For timing details, see Figure 4-7 (HARDWARE RESET segment).

Use an open drain/open collector type circuit to drive the signal low (< 0.3V (Input Voltage-Low (V))),

Do not add a pull-up resistor on this signal as it is internally biased high by default. The bias voltage depends on the module operating state in Active and Sleep modes, and in Hibernate and Lite Hibernate modes.

Note: For power-sensitive applications, the module does not reach minimal power consumption when held in reset. Therefore, it is not recommended to hold the module in reset state for long periods.

Warning: *RESET_IN_N should only be used to reset the module if it is unresponsive to AT commands and a power cycle cannot be performed. If used inappropriately (e.g. to reset during a firmware upgrade), memory corruption can occur.*

As an alternative, Semtech recommends implementing a software reset using AT+CFUN=1,1.

Warning: *During a module reset:*
- *All I/Os will be in an undefined state.*
- *I/Os must not be driven high (over 0.2 V), otherwise the module may be damaged*
- *RESET_IN_N must not be set low during a power cycle, otherwise the module will not boot.*
- *VBAT_BB must always be >3.2V when reset is asserted.*

Table 4-11 and Table 4-12 describe the RESET_IN_N signal.

Table 4-11: RESET_IN_N Pin Description

Pin	Signal Name	I/O[a]	Active	Description
C11	RESET_IN_N[b]	I	L	Reset signal

a. Signal direction with respect to the module.
b. Signal provided by host. Does not need to be buffered, and can be directly connected to module using an open drain/collector type circuit.

Refer to the following table for the electrical characteristics of the RESET_IN_N interface.

Table 4-12: RESET_IN_N Electrical Characteristics

Parameter	Min	Typ	Max	Unit
Input Voltage-Low	–	–	0.2	V
Reset assertion time	10	–	–	ms

4.8 Analog to Digital Converter (ADC)

The HL7900/HL7900E provides two general purpose ADC signals (ADC0, ADC1). These converters are 12-bit resolution ADCs with voltage range of 0–1.8V.

Typical ADC use is for monitoring external signals. The AT+KADC command is used to read the ADC values.

Table 4-13 describes the ADC signals.

Table 4-13: ADC Pin Description

Pin	Signal Name	I/O[a]	Description	Voltage Supply Domain
C24	ADC1	AI	Analog to digital converter	1.8V (VGPIO)
C25	ADC0	AI	Analog to digital converter	1.8V (VGPIO)

a. Signal direction with respect to the module.

4.9 Clock Interface

The HL7900/HL7900E supports two digital clock output signals.

These signals are disabled by default. To enable (or disable) these signals, use the AT+KHWIOCFG command.

Note: To reduce noise and radiated spurious emission (RSE), disable the clock signals if they are not being used.

Table 4-14 describes the clock signals.

Table 4-14: Clock Interface Pin Description

Pin	Signal Name	I/O[a]	Voltage Supply Domain	Description
C22	26M_CLKOUT	O	1.8V (VGPIO)	26 MHz Digital Clock output
C23	32K_CLKOUT	O	1.8V (VGPIO)	32.786 kHz Digital Clock output

a. Signal direction with respect to the module.

4.10 Debug Interfaces

The HL7900/HL7900E provides two 4-wire debug port interfaces (Diagnostic Interface, Modem Logs) that can be used with the AT interface for full debug capability.

Note: All UART signals operate at 1.8V. A voltage level shifter is required when connecting to a 3V3 domain.

UART interfaces are not active during Hibernate mode, so the host should ignore all activity on UART interfaces during Hibernate. If the module will enter Hibernate mode, Semtech recommends adding buffer circuits to ensure module I/Os are not driven high (i.e. >0.2V).

4.10.1 Diagnostic Interface

The Diagnostic interface is implemented over UART0. Refer to HL7900 AT Command Reference Guide for more information on enabling and configuring the DEBUG UART (AT%SETSRMCFG="DBGUARTMODE", 1 for enable and 2 for disable).

Table 4-15: Diagnostic Interface Pin Description

Pin	Signal Name[a]	Default State[b]	Active	Voltage Supply Domain	Description
C55	UART0_RX	Output	—	1.8V (VGPIO)	Debug Receive Data
C56	UART0_TX	Input	—	1.8V (VGPIO)	Debug Transmit Data
C57	UART0_CTS	Output	L	1.8V (VGPIO)	Debug Clear to Send
C58	UART0_RTS	Input	L	1.8V (VGPIO)	Debug Request to Send

a. Signals are named with respect to the host device (i.e. DTE (Data Terminal Equipment) convention—PC view). For example, UART0_RX is the signal used by the host to receive data from the module.
b. Signal direction with respect to the module. For example, UART0_RX is an output from the module to the host.

Note: It is highly recommended to provide access through Test Points to this interface (required for customer platform debugging).

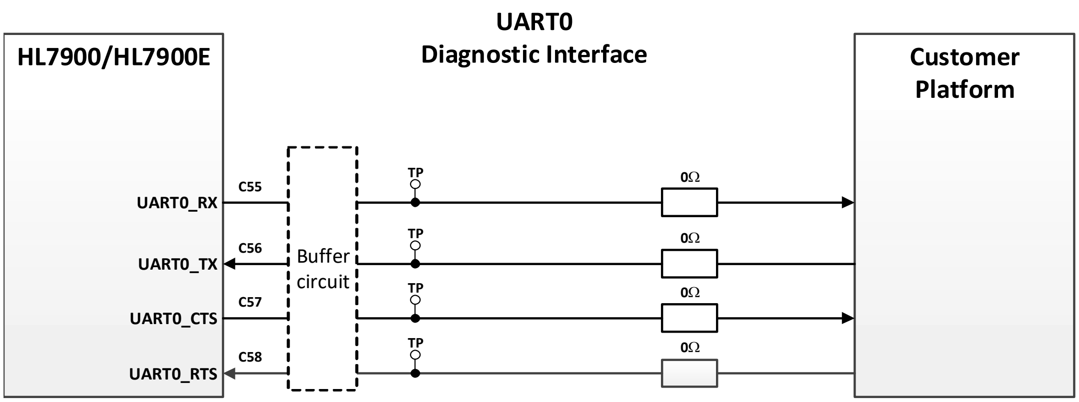


Figure 4-8: Diagnostic Interface connection example

4.10.2 Secondary UART Interface

Note: The Sensor Hub (SHUB) feature will be supported in a future firmware release.

Table 4-16: Modem Logs Interface Pin Description

Pin	Signal Name	I/O[a]	Voltage Supply Domain	Description
C51[b]	GPIO14	O	1.8V (VGPIO)	UART3_CTS[c]
C52[b]	GPIO10	I	1.8V (VGPIO)	UART3_TX[c]
C53[b]	GPIO11	I	1.8V (VGPIO)	UART3_RTS[c]
C54[b]	GPIO15	O	1.8V (VGPIO)	UART3_RX[c]

a. Signal direction with respect to the module. For example, GPIO14 is an output from the module to the host.
b. Pin can be assigned to either the internal MCU or Sensor Hub (SHUB).
c. Signals are named with respect to the host device (i.e. DTE (Data Terminal Equipment) convention—PC view). For example, UART3_RX is the signal used by the host to receive data from the module.

Note: To enable use of the UART3 interface for customer sensor hub application, it is highly recommended to provide access through Test Points to these 4 GPIOs.

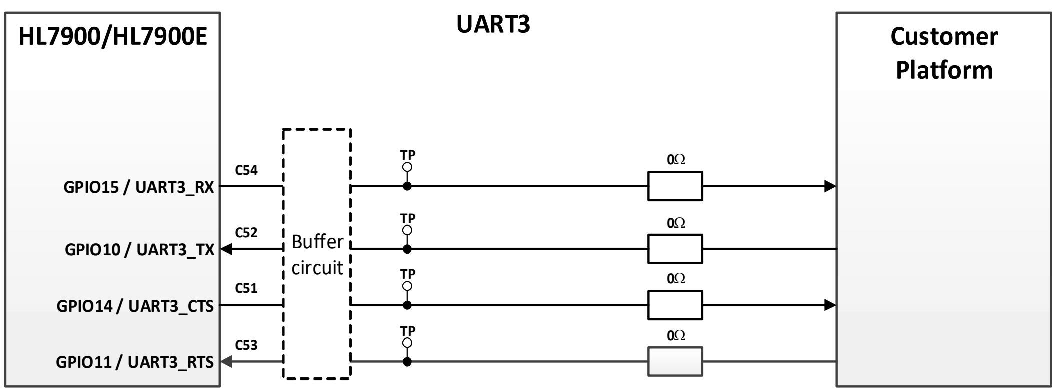


Figure 4-9: UART connection example

4.11 Wake Up Signal (WAKEUP)

The WAKEUP hardware control signal is used to wake the module from low power modes (Sleep, Lite Hibernate, Hibernate, OFF) by driving the signal high to 1.8V.

The module will not enter or return to low power mode while the WAKEUP signal is high. Table 4-17 and Table 4-18 describe the WAKEUP signal.

Table 4-17: WAKEUP Pin Description

Pin	Signal Name	I/O[a]	Voltage Supply Domain	Description
C44[b]	WAKEUP[c]	I	1.8V	Wakes the module up from low power mode
B13	WAKEUP_1_SHUB	I	1.8V	Wake up active high (For Sensor HUB wake up)

a. Signal direction with respect to the module.
b. Pin C44 (WAKEUP) requires an external pull-down (100 kΩ).
c. Signal provided by host. Signal does not need to be buffered, and can be directly connected to the module.

Table 4-18: WAKEUP Electrical Characteristics

Parameter	Min	Typ	Max	Unit
V_{IL}	–	–	0.2	V
V_{IH}	0.6	–	1.98	V
Wakeup assertion time[a]	100	–	–	µs

a. Assertion time—Time required to keep WAKEUP at high level to ensure module can wake up successfully.

4.11.1 Wakeup from Low Power Modes

This section describes the module's signal behaviors when waking from the low power modes defined in Table 3-5.

4.11.2 Wakeup from OFF Mode

Figure 4-10 and Table 4-19 describe signal behavior when WAKEUP is used to wake the module from OFF mode.

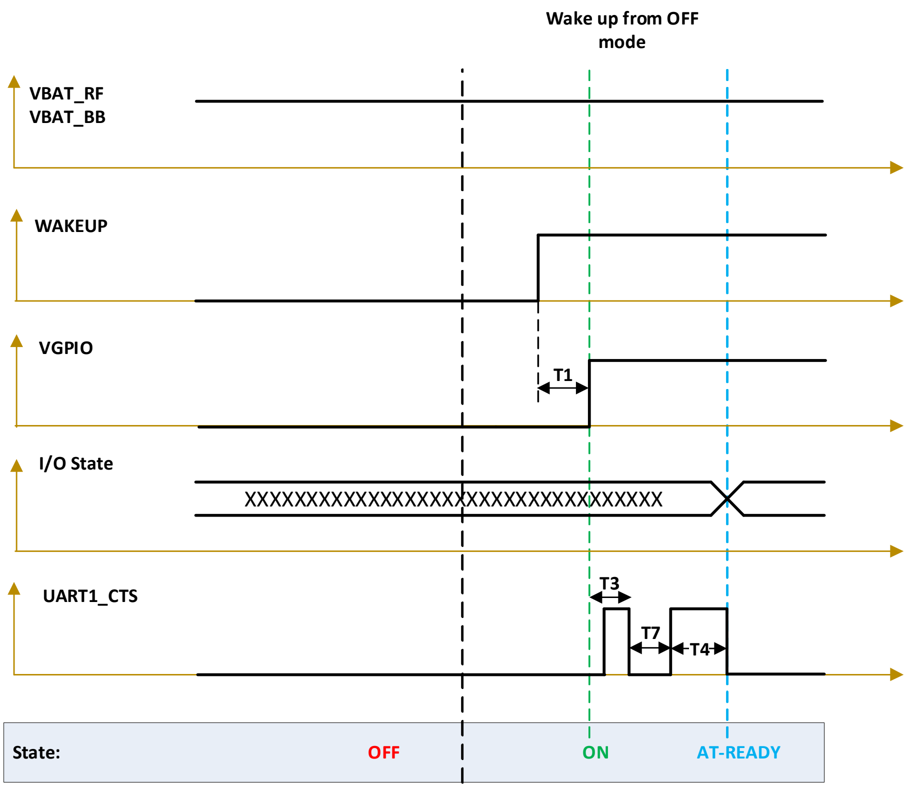


Figure 4-10: Wake up from OFF Mode

Table 4-19: WAKEUP Timing (from OFF Mode)

Parameter	Min	Typ	Max[a]	Unit
T1: Delay between WAKEUP and VGPIO	–	–	420	µs
T3: Delay	–	–	3.2	s
T4: Delay	–	–	5	s
T7: uboot delay	–	2	–	s

a. Measurements taken with HL78 Development Kit

4.11.3 Wakeup from Lite Hibernate Mode

Figure 4-11 and Table 4-20 describe the module's signal behaviors when WAKEUP is used to wake the module from Lite Hibernate mode.

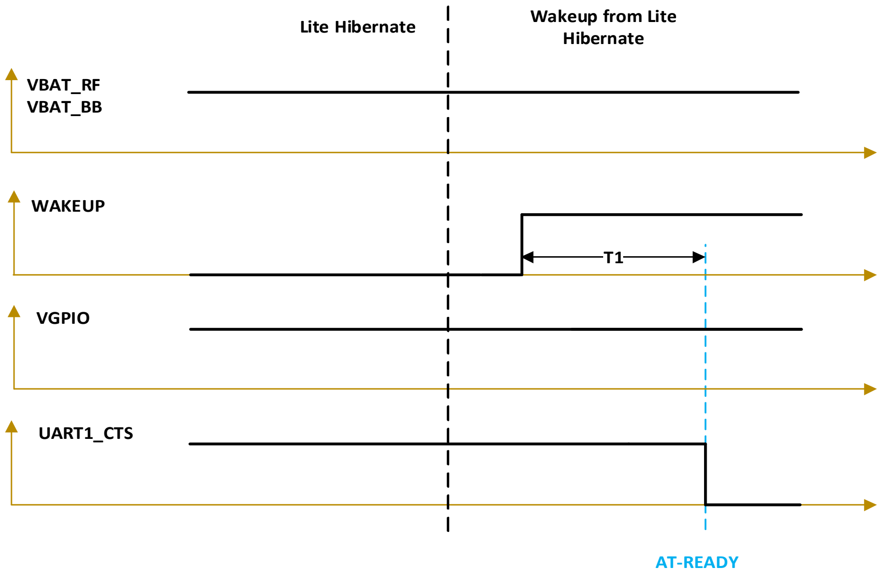


Figure 4-11: Wake up from Lite Hibernate Mode

Table 4-20: WAKEUP Timing (from Lite Hibernate Mode)

Parameter	Min	Typ	Max[a]	Unit
T1: Delay between WAKEUP and AT-READY	–	–	20	ms

a. Measurements taken with HL7900/HL7900E Development Kit

4.11.4 Wakeup from Hibernate Mode

Figure 4-12 and Table 4-21 describe the module's signal behaviors when WAKEUP is used to wake the module from Hibernate mode.

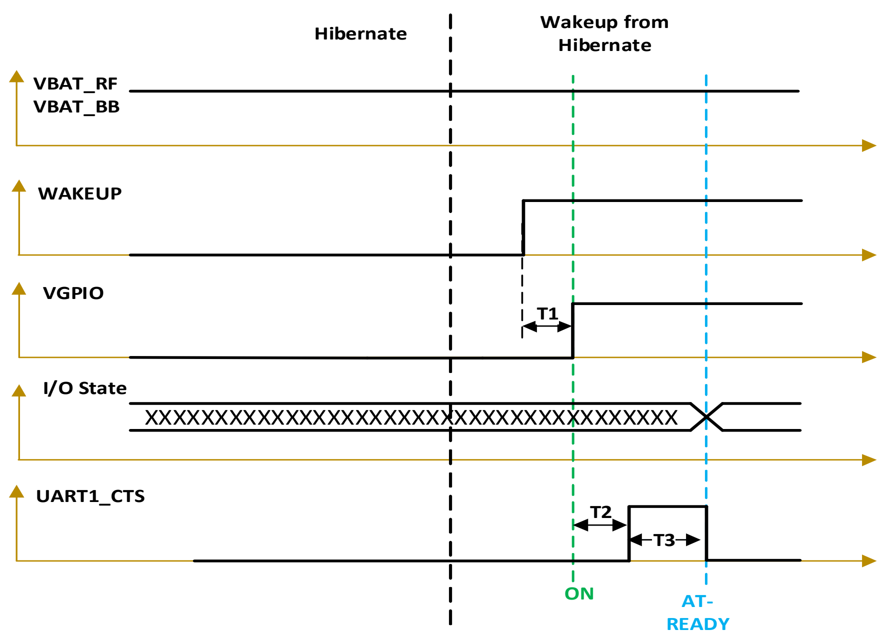


Figure 4-12: Wake up from Hibernate Mode

Table 4-21: WAKEUP Timing (from Hibernate Mode)

Parameter	Min	Typ	Max[a]	Unit
T1: Delay between WAKEUP and VGPIO	–	–	0.4	ms
T2: Delay between VGPIO and UART1_CTS high	–	–	60	µs
T3: UART1_CTS high to AT-READY	–	–	15	ms

a. Measurements taken with HL78 Development Kit

4.12 External Host Alarm Pin

The EXT_ALARM pin can be used as an alarm indicator to an external host as per the HL7900/HL7900E's power mode.

Table 4-22: Power Mode Alarm (TBD)

Pin	Signal Name	I/O	Voltage Supply Domain	Description
B7	EXT_ALARM	O	1.8V	Alarm indicator to an external host as per the HL7900/HL7900E power mode. Module active: high

4.13 RF Interface

The RF interface of the Semtech HL7900/HL7900E provides a single RF antenna connection for the transmission/reception of RF signals.

Contact Semtech technical support for assistance in integrating the Semtech HL7900/HL7900E on applications with embedded antennas.

4.13.1 RF Antenna Connection

A 50Ω RF track (with maximum VSWR 1.1:1, and 0.5 dB loss) is recommended to connect the module's RF_MAIN to standard RF antenna connectors (e.g. SMA, U.FL, etc).

Table 4-23 describes the module's RF interface.

Table 4-23: RF Main Pin Description

Pin	RF Signal	Impedance	VSWR Rx (max)	VSWR Tx (max)
C48	GND	–	–	–
C49	RF_MAIN	50Ω	2.5:1	2.5:1
C50	GND	–	–	–

4.13.2 LTE RF Interface

4.13.2.1 Maximum Output Power

The HL7900/HL7900E module's LTE maximum transmitter output power for all bands in normal operation conditions (25°C) is specified in Table 4-24.

Table 4-24: HL7900/HL7900E Conducted Tx Max Output Power Tolerances - LTE[a]

LTE Bands	Min	Typ	Max	Units	Notes
All bands	21.5[b]	23	24.5	dBm	Power class 3

a. Under normal operating conditions (25°C)
b. Additional power reduction is applied to the lowest and highest supported channels for each band — see Table 1-1 footnote "a" for supported Tx channel ranges. (e.g. applies to B2 channels 18602 and 19198)

4.13.2.2 Rx Sensitivity

The module's LTE receiver sensitivity is specified in the following tables.

Table 4-25: HL7900/HL7900E Typical Conducted Cat-M1 RX Sensitivity[a]

LTE Band	Typical Reference Sensitivity Level @ 95% of Maximum Throughput		
	@ +25°C (dBm)	@ Class A (dBm)	3GPP Limit (dBm)[b]
B1	-107	-104.5	-102.3
B2	-107	-105	-100.3
B3	-107	-105	-99.3
B4	-107	-104.5	-102.3
B5	-107.5	-105.5	-100.8
B8	-107	-105	-99.8
B12	-106.5	-105	-99.3
B13	-106.5	-105	-99.3
B18	-107	-105.5	-100.3
B19	-107.5	-105.5	-102.3
B20	-107	-105	-99.8
B25	-107	-105	-100.3
B26	-107.5	-105.5	-100.3[c]
B28	-107	-105	-100.8
B66	-106.5	-105	-102.3[c]

a. Test conditions per 3GPP TS 36.521-1 v13: Bandwidth: 5MHz on Reference Measurement Channel.
b. Displayed limits derived from 3GPP TS 36.521-1 V16.3.0, Table 7.3EA-2, adjusted by +0.7 dB for measurement uncertainty.
c. Band not defined by 3GPP therefore no associated limit.

Table 4-26: HL7900/HL7900E Typical Conducted NB1/NB2 RX Sensitivity[a]

LTE Band	Typical Reference Sensitivity Level @ 95% of Maximum Throughput		
	@ +25°C (dBm)	@ Class A (dBm)	3GPP Limit (dBm)[b]
B1	-114.5	-113.5	-107.5
B2	-114.5	-114	-107.5
B3	-114.5	-113.5	-107.5
B4	-114.5	-113.5	-107.5
B5	-115	-114	-107.5
B8	-114.5	-114	-107.5
B12	-114.5	-113.5	-107.5
B13	-114.5	-113	-107.5
B18	-115	-114	-107.5
B19	-115	-114	-107.5
B20	-115	-114	-107.5
B25	-115	-113.5	-107.5
B26	-115	-114	-107.5
B28	-115	-113.5	-107.5
B65	-114.5	-113.5	-107.5
B66	-114.5	-113.5	-107.5
B70	-114.5	-113.5	-107.5
B85	-114.5	-113.5	-107.5

a. Test conditions per 3GPP TS 36.521-1 v13: on DL Reference Measurement Channel defined
b. Displayed limits derived from 3GPP TS 36.521-1 V16.3.0, Table 7.3F.1.3-1, adjusted by +0.7 dB for measurement uncertainty

4.14 TX Burst Indicator (TX_ON)

The HL7900/HL7900E provides the TX_ON signal for TX activity indication.

Table 4-27: TX_ON Pin Description

Pin	Signal Name	I/O[a]	Voltage Supply Domain	Description
C60	TX_ON	O	1.8V (VGPIO)	High during Tx activity

a. Signal direction with respect to the module

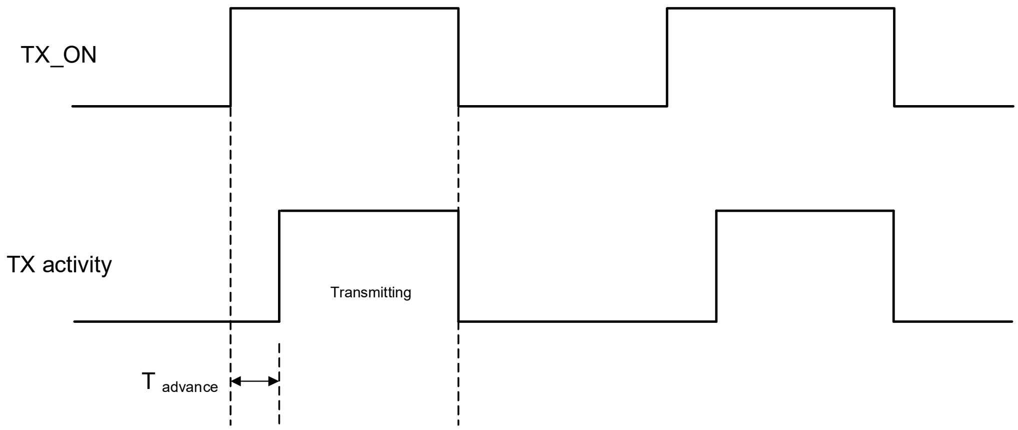


Figure 4-13: TX_ON State High during TX Activity

Table 4-28: TX_ON Characteristics

Parameter	Typical
$T_{advance}$	32 µs

4.15 Tx/Rx Activity Indicator; External RF Voltage Control

The HL7900/HL7900E provides the VBAT_PA_EN signal for RF activity (Tx/Rx) indication.

Depending on customer requirements, it can be also be used to select the module VBAT_RF power source during RF activity, and support antenna switching.

To enable/disable this feature, use the AT+KHWIOCFG command. The following tables and figure describe the VBAT_PA_EN signal.

Table 4-29: VBAT_PA_EN Pin Description

Pin	Signal Name	I/O[a]	Voltage Supply Domain	Description
C41[b]	GPIO8	I/O	1.8V (VGPIO)	High during Tx/Rx activity
	VBAT_PA_EN	O		

a. Signal direction with respect to the module
b. The default function is VBAT_PA_EN for C41. Contact Semtech to enable the GPIO function.

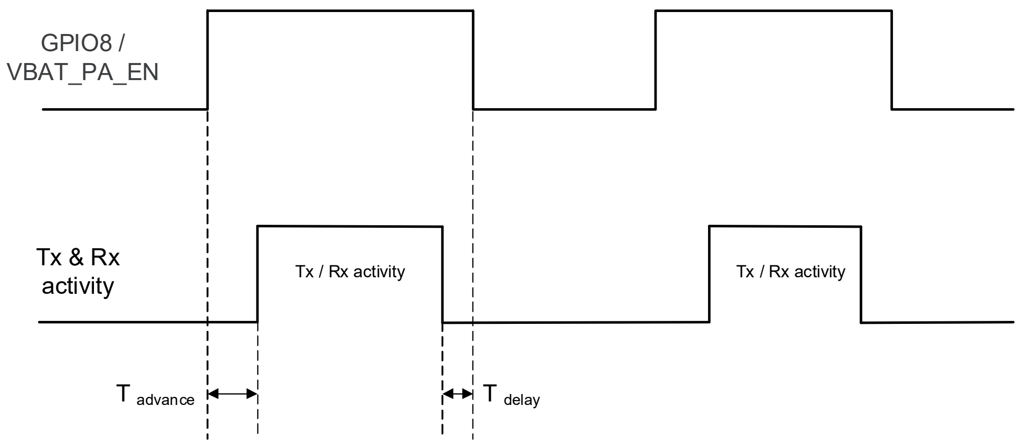


Figure 4-14: VBAT_PA_EN State during Tx/Rx Activity

Table 4-30: VBAT_PA_EN Characteristics (TBC)

Parameter	Min	Max
$T_{advance}$	2 ms	8 ms
T_{delay}	550 µs	3 ms

4.16 GNSS (for HL7900 only)

The HL7900's GNSS implementation supports GPS L1 operation (GLONASS G1 will be supported in a future firmware release).

Note: HL7900 GNSS support is hardware SKU-dependent. For details, contact your Semtech account representative.

Note: The GNSS receiver and LTE receiver share the same RF resources, therefore GNSS can only be used when the module is not actively connected on LTE. An example of a suitable implementation of GNSS in an end product would be the use of GNSS positioning for asset management applications where infrequent and no real-time position updates are required.

Table 4-31 and Table 4-32 describe the GNSS antenna specifications.

Table 4-31: GNSS Passive Antenna — Specifications

Characteristic		Value
Frequency	GPS L1	1563–1587 MHz
	GLONASS G1[a]	1593–1610 MHz
RF Impedance (RF_GNSS Pin)		50Ω
VSWR max		2:1

a. GLONASS G1 will be supported in a future firmware release.

Table 4-32: GNSS Active Antenna — Specifications (Preliminary)[a]

Characteristic	Requirements	Comment
Antenna gain	Customer-specified	For active antenna configuration details, see 4.16.2: EXT_GPS_LNA_EN.
SAW filter position	LNA input	—
Pass band	1559.05–1605.89 MHz	GPS L1; GLONASS L1
Supply voltage	1.8 V	EXT_GPS_LNA_EN drives (enables/disables) the active antenna (see 4.16.2: EXT_GPS_LNA_EN).
Current consumption	< 10 mA	—
Power gain	14–22 dB (1559.05–1605.89 MHz)	—
Noise figure	< 2.5 dB (1559.05–1605.89 MHz)	—
Impedance (in/out)	50Ω	—
VSWR (in/out)	< 2:1 (1559.05–1605.89 MHz)	—
700 MHz harmonic	< -85 dBm	▪ Input jammer tones — 777/787.5 MHz at +15 dBm ▪ Measure the harmonic at 1554/1575 MHz. ▪ **Note:** To satisfy this requirement, a high-Q LC notch filter is required at the input of the GNSS FEM.
Input 1 dB compression point	> -10 dBm (in-band) > 25 dBm (out-of-band)	—
Input second-order intercept Point IIP2 (out-of-band)	> 85 dBm	▪ Input jammer tones — 824.6/2400 MHz at +15 dBm ▪ Output IM2 at 1575.4 MHz
Input third-order intercept point IIP3 (out-of-band)	> 65 dBm	▪ Input jammer tones — 1712.7/1850 MHz at +15 dBm ▪ Output IM3 at 1575.4 MHz
Absolute attenuation	> 45 dB (777–915 MHz) > 35 dB (915–1463 MHz) > 40 dB (1710–2700 MHz)	—

a. Active GNSS antenna support will be available in a future firmware release.

4.16.1 GNSS Performance

Table 4-33 summarizes the HL7900 module's GNSS performance characteristics.

Table 4-33: GNSS Performance

Parameters	Conditions	Typical Value
Sensitivity	Cold Start	-145 dBm
	Hot Start	-152 dBm
	Tracking	-161 dBm
Time To First Fix (TTFF)	Cold start, Input power -130 dBm	35 s
	Hot start, Input power -130 dBm	1 s
2D Position Error (2DRMS)	Input power -130 dBm	1 m

4.16.2 EXT_GPS_LNA_EN

Note: This feature will be supported in a future firmware release.

The HL7900/HL7900E can be configured to use a passive antenna or (pending a future firmware release) an active antenna. EXT_GPS_LNA_EN (pin C43) is used to enable or disable the active antenna.

Table 4-34: EXT_GPS_LNA_EN Pin Description

Pin	Signal Name	I/O[a]	Voltage Supply Domain	Description
C43	EXT_GPS_LNA_EN	O	1.8 V	Enable active antenna

a. Signal direction with respect to the module

The AT command +KGNSSACTANT is used to configure the module to use a passive antenna (configuration value 0) or an active antenna (configuration values 15, 18, 21).

When the module is configured to use:

- Passive antenna — Leave EXT_GPS_LNA_EN floating
- Active antenna — Drive EXT_GPS_LNA_EN (1.8 V) high

Table 4-35: Active / Passive antenna configuration

EXT_GPS_LNA_EN state	Antenna type	+KGNSSACTANT gain configuration value[a]	Supported Gain (dBm)	Notes
0 V	Passive	0	0	
1.8 V	Active	15	14–16	Set the gain configuration value (15, 18, or 19) to choose a supported gain range that matches the connected active antenna.
		18	17–19	
		21	20–22	

a. For +KGNSSACTANT command details, refer to *[1] HL7900 AT Command Reference Guide (Doc# 41114811).*

4.17 External Flash Interface

Note: This feature will be supported in a future firmware release.

HL7900/HL7900E is designed to operate with an external quad SPI flash memory of at least 64 Mbit. The required memory size depends on the number of applications the device will be supporting.

Table 4-36: External FLASH Interface

Pin	Signal Name	I/O	Voltage Supply Domain	Description
B1	SF_SI/IO0	I/O	1.8V	Serial Flash Input/Output (IO0) for Dual or Quad commands
B2	SF_SO/IO1	I/O	1.8V	Serial Flash Input/Output (IO1) for Dual or Quad commands
B3	SF_nWP/IO2	I/O	1.8V	Serial Flash Input/Output (IO2) for Quad commands
B4	SF_nHOLD/IO3	I/O	1.8V	Serial Flash Input/Output (IO3) for Quad commands
B5	SF_CLK	O	1.8V	Serial Flash Serial Clock
B57	SF_nCS1 / PSRAM DQS	O	1.8V	Serial Flash Chip Select 1/ PSRAM DQS
B14	VDD_PSRAM	O	1.8V	Power source for external FLASH/PSRAM

4.18 MIPI Interface

Note: This feature will be supported in a future firmware release.

HL7900/HL7900E supports MIPI interface for antenna tuning.

Table 4-37: MIPI Interface

Pin	Signal Name	I/O	Voltage Supply Domain	Description
B44	RFFE_SCLK	O	1.8V	MIPI RFFE Clock signal
B45	RFFE_SDATA	I/O	1.8V	MIPI RFFE directional/bidirectional data signal

4.19 External PSRAM Interface

Note: This feature will be supported in a future firmware release.

The HL7900/HL7900E is designed to operate with an external SPI / Quad SPI PSRAM memory 16 Mbit or larger.

Table 4-38: External PSRAM Interface

Pin	Signal Name	I/O	Voltage Supply Domain	Description
B14	VDD_PSRAM	O	1.8V	Power source for external FLASH/PSRAM
B51	PSRAM_CSn	O	1.8V	PSRAM Chip Select
B52	PSRAM_IO2	I/O	1.8V	PSRAM I/O 2
B53	PSRAM_IO0	I/O	1.8V	PSRAM I/O 0
B54	PSRAM_IO3	I/O	1.8V	PSRAM I/O 3
B55	PSRAM_IO1	I/O	1.8V	PSRAM I/O 1
B56	PSRAM_CLK	O	1.8V	PSRAM Clock
B57	Serial Flash Chip Select 1 / PSRAM DQS	O	1.8V	SF_nCS1 / PSRAM DQS

4.20 JTAG Interface

Table 4-39: JTAG Interface

Pin	Signal Name	I/O	Voltage Supply Domain	Description
B58	EJ_TCK	I/O	1.8V	JTAG Test Clock
B59	EJ_TDO	O	1.8V	JTAG Test Data Output / Serial Wire Debug
B60	EJ_TRST	I/O	1.8V	JTAG Test Reset
B61	EJ_TMS	I/O	1.8V	JTAG Test Mode Select / Serial Wire Debug
B62	EJ_TDI	I/O	1.8V	JTAG Test Data Input
B64	EJ_DEBUG_RST_N	I/O	1.8V	Reset pin for the JTAG probe

4.21 I2C Interface

Note: This feature will be supported in a future firmware release.

The HL7900/HL7900E supports the I2C Master/Slave interface, depending on the SHUB application. I2C master interface from SHUB subsystem can be used by the MCU.

The I2C interface circuitry uses two bidirectional open-drain lines, Serial Data Line (SDA) and Serial Clock (SCL), pulled up with external resistors (on customer's PCB, 2.2K – 10K Ω based on customer's application design).

The I2C bus consists of 2 lines: SDA (serial data) & SCL (serial clock); each device connected to the I2C bus is defined as master/slave/transmitter/receiver.

Each slave device is targeted via a dedicated device address. All transactions on the I2C bus are addressed transactions. The address of the transaction is published at the first phase of the transaction. Device address is usually 7 bit and 10 bit address is optional.

The following I2C speed modes are supported:

- Standard mode up to 100 kbps
- Fast mode up to 400 kbps

4.22 SPI Interface

Note: This feature will be supported in a future firmware release.

The HL7900/HL7900E supports Serial Peripheral Interface (SPI), where the internal MCU has an SPI master interface and dedicated SPI slave interface (MCU_SPIS).

4.22.1 SPI Master Interface

The SPI master interface is a synchronous serial data link standard that operates in Full Duplex mode. Devices communicate in Master/Slave mode where the master device initiates the data frame. Multiple slave devices are allowed with individual slave select (chip select) lines.

This interface prepares data to be written to, or read from, to "offload" from the bus fabric or DMA. The divide clock speeds match the appropriate slave speed. The maximum support clock is TBD.

The SPI bus specifies the following four logic signals.

- SCLK: Clock driven by the master
- MISO: Master input from the slave
- MOSI: Master output to the slave
- CS: Chip select output from the master (active low)

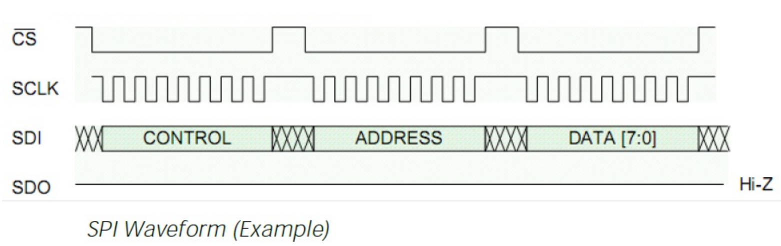


Figure 4-15: SPI waveform example

4.22.1.1 SPI Master Mode Timing

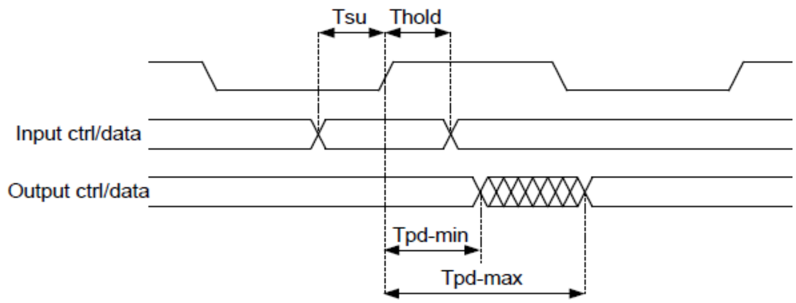


Figure 4-16: SPI Master—SPI_CLK_POS Timing

Table 4-40: SPI Master — SPI_CLK_POS Timing Parameters

Parameter	Min (ns)	Max (ns)	Description
T_{cycle}	30.77	—	32.5 MHz clock
T_{su}	4.5	—	Input setup time (with respect to the CLK's rising edge)
T_{hold}	0	—	Input hold time (with respect to the CLK's rising edge)
T_{pd}	1.5	13.5	Output delay (with respect to the CLK's rising edge)

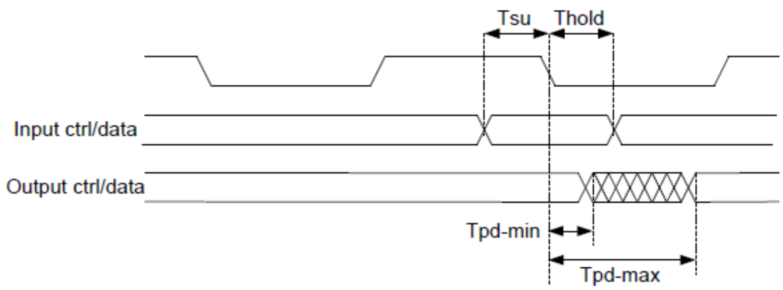


Figure 4-17: SPI Master—SPI_CLK_NEG Timing

Table 4-41: SPI Master — SPI_CLK_POS Timing Parameters

Parameter	Min (ns)	Max (ns)	Description
T_{cycle}	30.77	—	32.5 MHz clock
T_{su}	4.5	—	Input setup time (with respect to the CLK's falling edge)
T_{hold}	0	—	Input hold time (with respect to the CLK's falling edge)
T_{pd}	1	15.5	Output delay (with respect to the CLK's falling edge)

4.22.2 SPI Slave Interface

4.22.2.1 SPI Slave Mode Timing

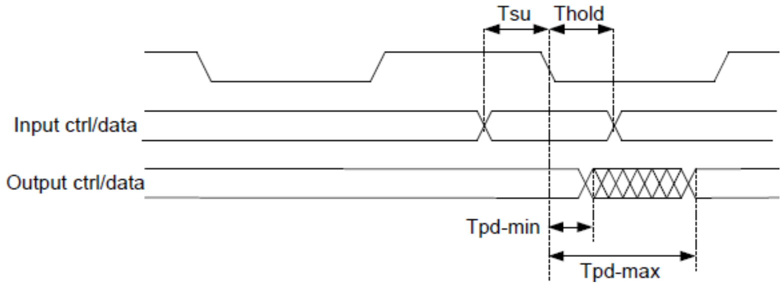


Figure 4-18: SPI Slave—SPI_CLK_POS Timing

Table 4-42: SPI Slave—SPI_CLK_POS Timing Parameters

Parameter	Min (ns)	Max (ns)	Description
T_{cycle}	30.77	—	25 MHz clock
T_{su}	4.5	—	Input setup time (with respect to the CLK's rising edge)
T_{hold}	0	—	Input hold time (with respect to the CLK's rising edge)
T_{pd}[a]	1.5	13.5	Output delay (with respect to the CLK's rising edge)

a. MISO is ready to output data approximately 50 ns after the chip select is asserted.

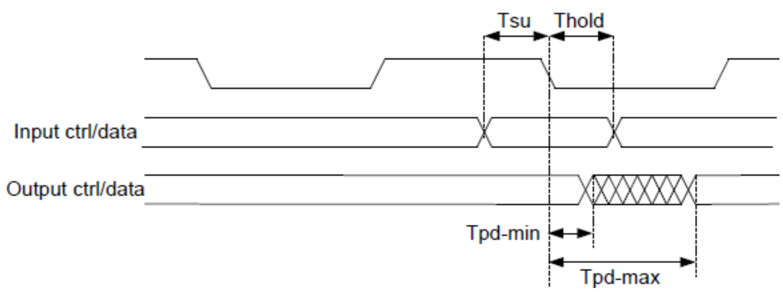


Figure 4-19: SPI Slave—SPI_CLK_NEG Timing

Table 4-43: SPI Slave—SPI_CLK_NEG Timing Parameters

Parameter	Min (ns)	Max (ns)	Description
T_{cycle}	40	—	25 MHz clock
T_{su}	5	—	Input setup time (with respect to the CLK's rising edge)
T_{hold}	0	—	Input hold time (with respect to the CLK's rising edge)
T_{pd}[a]	4.5	30.5	Output delay (with respect to the CLK's rising edge)

a. MISO is ready to output data approximately 50 ns after the chip select is asserted.

4.23 Wi-Fi (for HL7900 only)

The HL7900 supports Wi-Fi passive scan functionality (e.g., receive only) that is enabled by leveraging the module's existing Rx chain.

The Wi-Fi functionality is accessible via AT commands and software APIs.

HL7900 Wi-Fi features include:

- Integrated Wi-Fi to support Wi-Fi positioning under poor GNSS coverage conditions.
- Indoor positioning and geofencing, which enables device tracking even when GNSS positioning is unavailable
- Integration with LTE modem to translate received SSIDs / MAC for geolocation

For details, refer to the HL79 Wi-Fi User Guide .

Note: There may be additional costs associated with this feature. Contact Semtech Sales for details.

5: Mechanical Drawings

For tolerances, refer to Table 1-2 and Table 1-3.

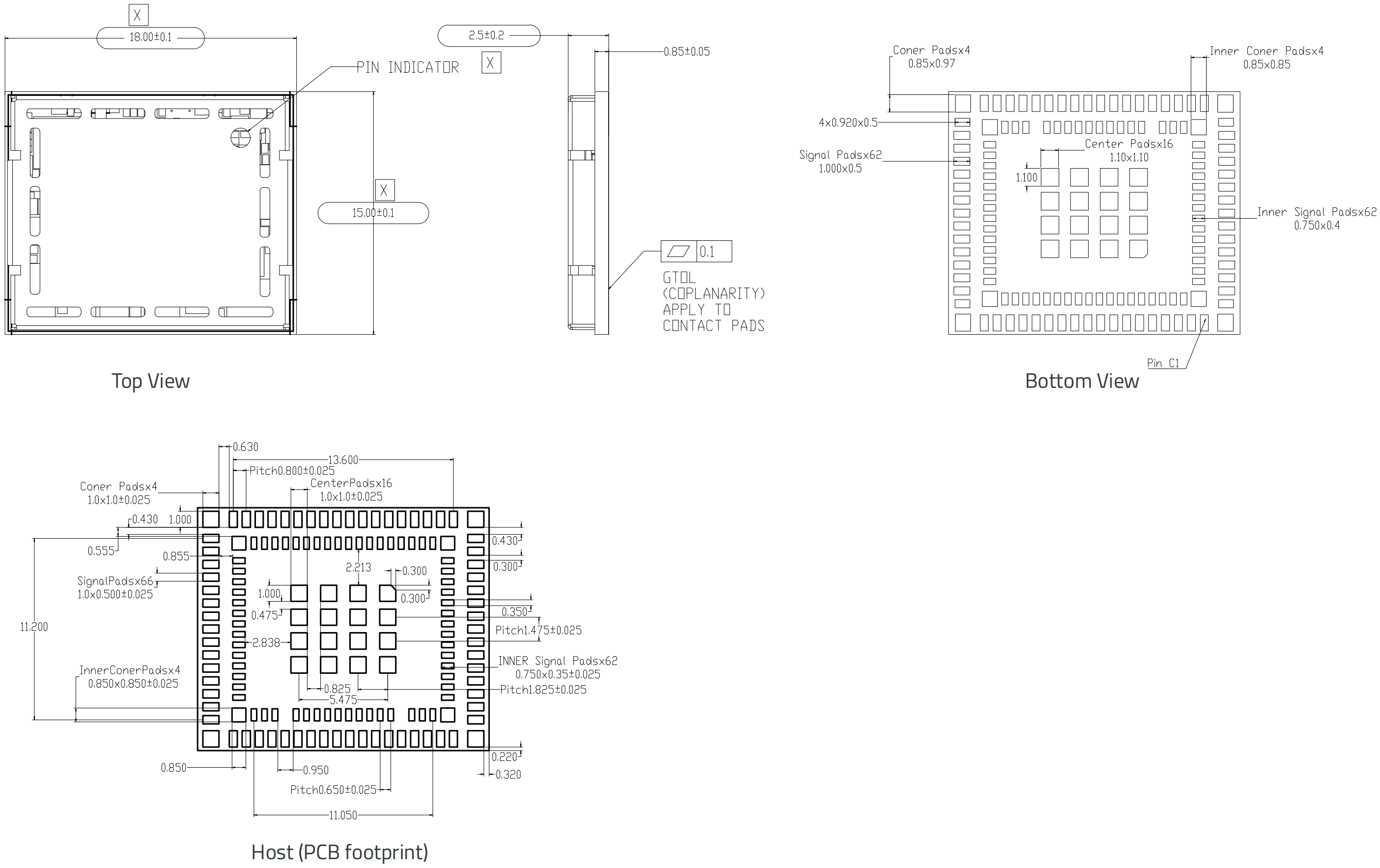


Figure 5-1: Mechanical Drawing

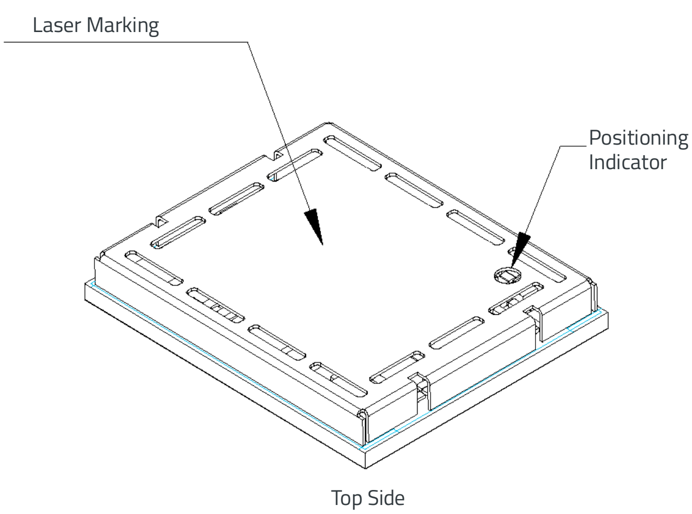


Figure 5-2: Top Side

6: Design Guidelines

6.1 Power Supply Design

When designing the power supply, make sure VBAT_BB/VBAT_RF meet the requirements listed in Table 3-2— Semtech recommends adding a 30% design margin, if possible.

Careful attention should be paid to the following:

- Power supply design— A low-ripple, low-noise source such as LDO, battery, or switching power supply (SMPS) is recommended.
- Capacity to deliver high current peaks in a short time
    - VBAT_BB/VBAT_RF must support peak currents with an acceptable voltage drop that guarantees the minimum required VBAT_BB/VBAT_RF value.
- VBAT_BB/VBAT_RF signal voltage must never exceed the maximum value, otherwise the module may be severely damaged.
    - If necessary, add a voltage limiter to the module’s power supply lines to ensure VBAT will never receive a voltage surge over 4.35V. There are a few protection options from a basic linear regulator to a voltage limiter, as simple as a Zener diode.
- ESD protection is recommended on VBAT_BB/VBAT_RF supply rails— Semtech recommends Diodes Inc part # D8V0L1B2LP3-7 or Semtech uClamp0531ZA.
- Both over-voltage protection and ESD protection devices will increase platform current consumption.
- All ground pins (C30, C32, C37, C39, C48, C50, CG1–CG4, G1–G16) must be connected to the same net.

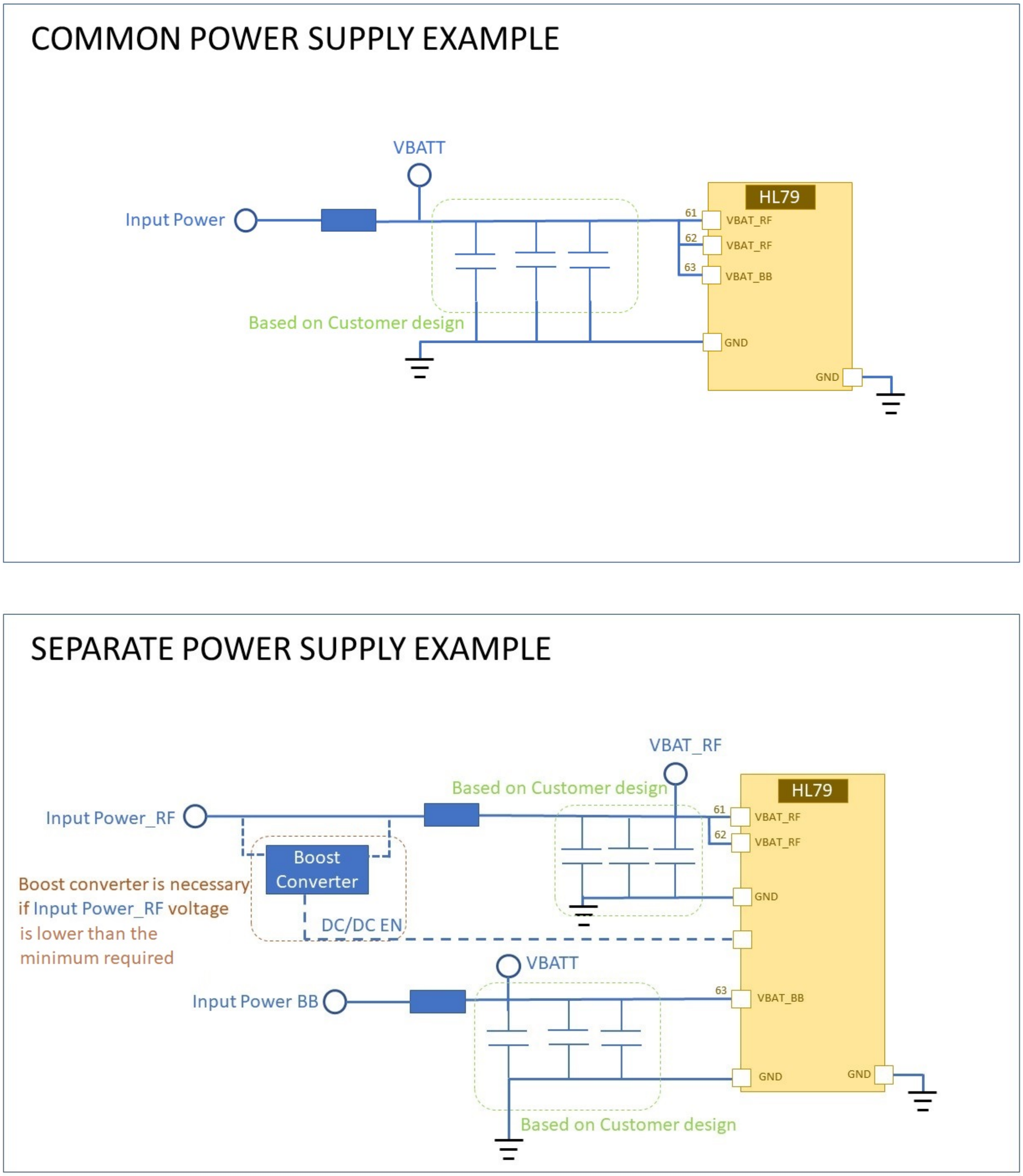


Figure 6-1: Common Power Supply and Separate Power Supply Samples

The HL7900/HL7900E requires a solid, central ground plane (with solder mask defined pads) located directly under the module. This will:

- Ensure high current signal returns.
- Provide heat dissipation under higher operating temperatures.

The ground plane should be connected (with vias) to the reference ground layer of the application board.

6.2 UIM1

UIM1 can operate at clock rates up to 5 MHz.

Most UIM1 signal lines do not require a buffer during Hibernate, and can be directly connected to the UIM card or holder. A buffer is required for UIM_DET1 if powered from the host (not required if powered from VGPIO).

Decoupling capacitor(s) must be added to UIM1_VCC (≥ 1 µF) and UIM1_DET, as close as possible to the UIM card. Decoupling capacitors for UIM1_CLK, UIM1_RST, and UIM1_DATA are recommended to be added as placeholders for potential EMC issues.

The two resistors (RCLK and RDAT) should be added as placeholders to compensate for potential layout issues. Both can be populated to slew the UIM1 signals, if required.

The UIM1_DATA trace should be routed away from the UIM1_CLK trace.

Keep the distance between the module and the UIM holder as short as possible.

To avoid ESD issues based on the host platform's design requirements, Semtech recommends using the following ESD protection diodes or Transient Voltage Suppressors (TVS) on the UIM1 interface:

- INFINEON part # ESD112-B1-02EL E6327— UIM1_CLK, UIM1_DATA, UIM1_RESET
- Diodes Inc part # D8V0L1B2LP3-7 — UIM1_VCC, UIM1_DET

Figure 6-2 illustrates the recommended implementation of a UIM interface

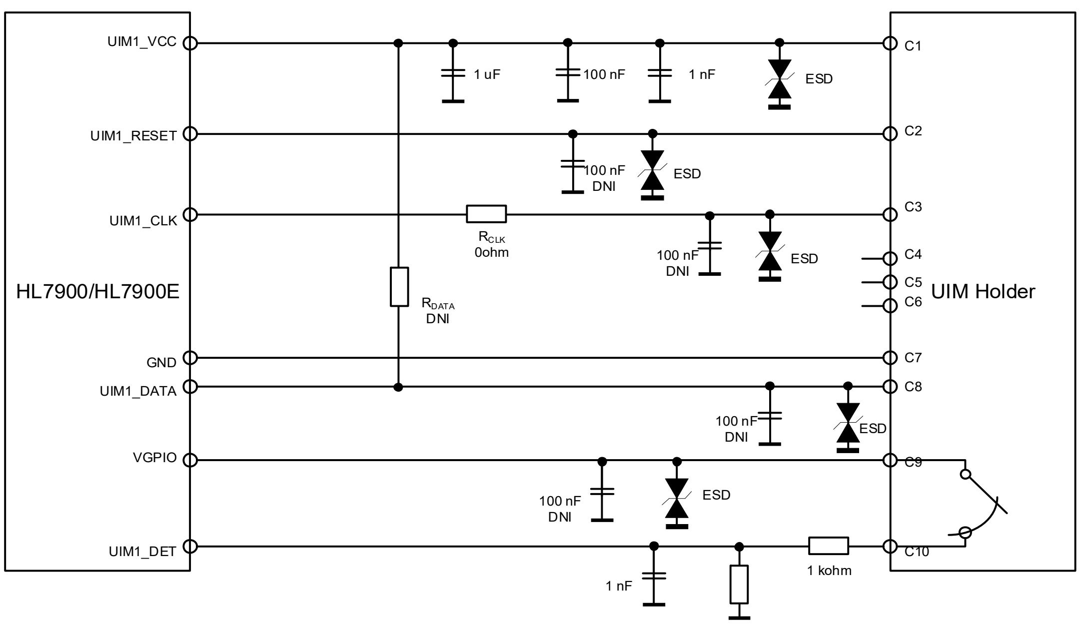


Figure 6-2: EMC and ESD Components Close to the USIM

6.3 ESD Protection for I/Os

ESD protection is highly recommended where module signals (GPIO, UART, H/W control, Indication, ADC, Clock) are externally accessible and potentially subjected to ESD by the user. Semtech recommends using Diodes Inc part # D8V0L1B2LP3-7.

6.4 Hibernate—Isolation Requirements

While the module is in Hibernate mode, the host platform (MCU) interfaces can remain powered.

Important: *To prevent these signals from back-powering the module, the host platform should make sure to isolate them—the signals should not be driven high (e.g. > 0.2 V).*

To ensure the host platform does not back-power the module:

- The host can add a buffer circuit to isolate module I/O during Hibernate. Semtech recommends using VGPIO to tristate I/O signals.
- The MCU can tristate any I/O that does not have an external PU/PD.

Note: A buffer is not required in Lite Hibernate mode.

If adding a buffer circuit, consider the signal type:

- Bidirectional (Input/Output) signals— For module I/O signals (e.g. GPIOs), an analog switch that can tri-state both the output and the input can be used (e.g. Texas Instruments TMUX1511). As shown in Figure 6-3, I/O signals connected to the buffer will be tri-stated.
- Directional (Input) signals— For module inputs (e.g. UART1_TX), a logic buffer with output tri-state mode can be used (e.g. Texas Instruments SN74LVC1G126). As shown in Figure 6-4, the signal is controlled and, when disabled, the output signal is tri-stated.

Note: Parts and usage descriptions above are intended as examples to assist the host platform designer in developing an appropriate solution for the platform. Selection and use of specific parts is the responsibility of the host platform designer.

Control of the buffer circuit is based on the status of VGPIO— for details, see 6.4.1: VGPIO Monitoring and Buffer Control.

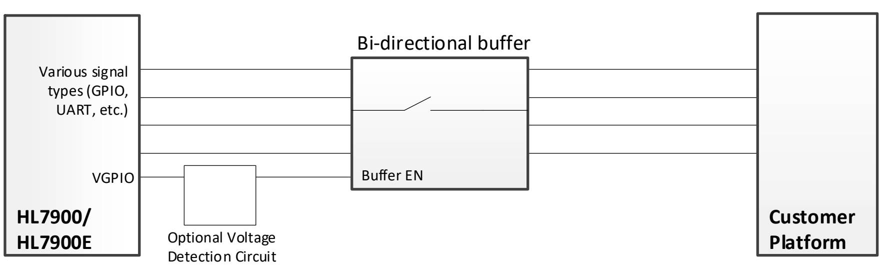


Figure 6-3: Example-Buffer - Bidirectional Signal

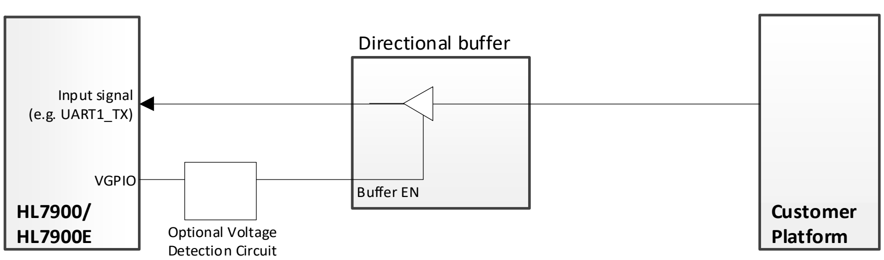


Figure 6-4: Example-Buffer - Directional Signal

6.4.1 VGPIO Monitoring and Buffer Control

Because the host platform can remain powered in Hibernate and Reset states, the host platform must react quickly, when VGPIO transitions low, to ensure signals do not back- power the module.

The host platform can monitor VGPIO to determine the HL7900/HL7900E module's current operating mode— for details, see 4.1: VGPIO.

To ensure faster detection of VGPIO transitions, Semtech recommends adding an optional voltage detection circuit (as shown in Figure 6-3 and Figure 6-4) to monitor and detect the transition low, and then control (enable/disable) the associated buffer circuit.

Note: VGPIO can be used to directly connect to the buffer enable signal but the host platform must ensure that all host outputs are not driven high (i.e. > 0.2 V) before the module enters Hibernate mode.

6.5 General Rules and Recommendations

Clock and other high-frequency digital signals (e.g. serial buses) should be routed as far as possible from the module's analog signals. If the application design makes it possible, all analog signals should be separated from digital signals by a ground trace on the PCB.

6.6 Radio Frequency Integration

The HL7900/HL7900E is equipped with an external antenna.

6.6.1 Antenna Matching Circuit

Note: GNSS function is for HL7900 only

A 50Ω line matching circuit between the module, the customer's board and the RF antenna is required as shown in Figure 6-5.

Because matching is dependent on the customer's platform, values marked as 'TBD' for the recommended components must be determined by the customer.

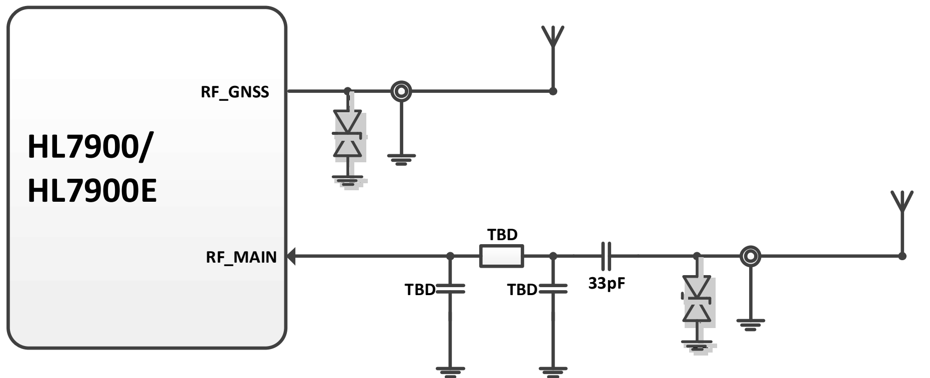


Figure 6-5: Antenna Connection

Semtech recommends using the following ESD diodes or Semtech TVS:

- INFINEON ESD103-B1-02EL E6327 or Semtech RClamp0561Z—RF_MAIN, RF_GNSS

6.6.2 RF Circuit

The RF signal must be routed on the application board using tracks with a 50Ω characteristic impedance.

The characteristic impedance depends on the dielectric, the track width and the ground plane spacing.

It is recommended to use stripline design if the RF path is fairly long (more than3 cm), since microstrip design is not shielded. Consequently, the RF (transmit) signal may interfere with neighboring electronic circuits. In the same way, the neighboring electronics (micro-controllers, etc.) may interfere with the RF (receive) signal and degrade the reception performance.

The RF trace on the development board is routed from the module antenna port to the RF connector (SMA). The RF trace is designed as a 50Ω coplanar stripline and its length is 22 mm.

The following drawings show the location of the Semtech HL7900/HL7900E on the development board, the routing cross section and the top view of the RF trace on the development board.

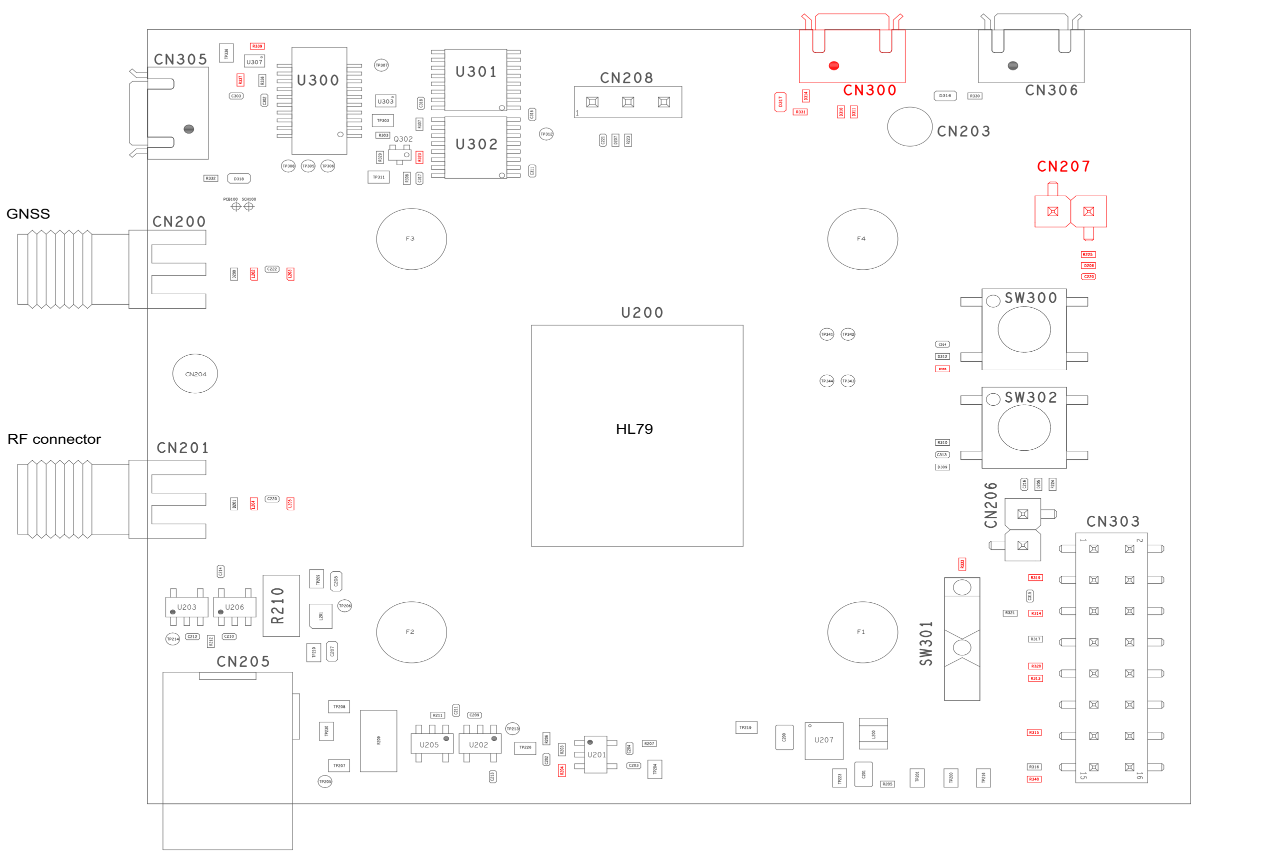


Figure 6-6: Module Location on Development Board

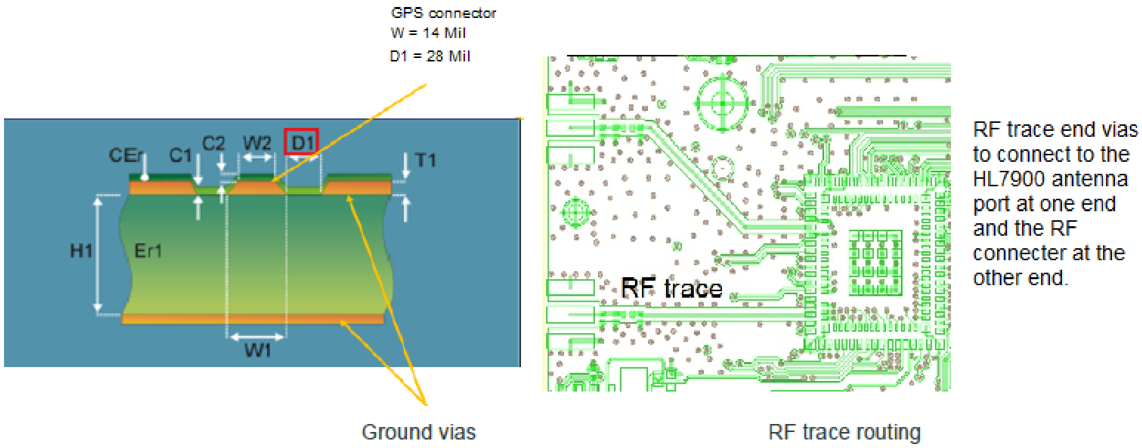


Figure 6-7: Development Board RF Trace Design

6.7 Antenna Tuning Specifications

The HL7900/HL7900E module is compatible with antenna tuning solutions that utilize specialized RF switches with MIPI control. These can be implemented either in antenna aperture tuning or in direct impedance tuning circuits, each offering multiple resonant frequency configurations.

Table 6-1 lists recommended antenna tuning switches for use with the HL7900/HL7900E.

Table 6-1: Recommended Antenna Tuning Switches for HL7900/HL7900E

Vendor	Part Number	Type	CTRL IF	AT command[a]	Main features
Skyworks	SKY19249	SP4T	MIPI	AT+KANTTUNE=1	1.1 x 1.5 mm 1.0 Ω, 45 Vpk
Sony	CXA4612XR	4xSPST	MIPI	AT+KANTTUNE=3	1.1 x 1.5 mm 1.6 Ω, 55 Vpk
Sony	CXA4605XR	4xSPST	MIPI	AT+KANTTUNE=2	1.1 x 1.5 mm 1.22 Ω, 55 Vpk
Other	Consult with Semtech about using other antenna tuning switches.				

a. For antenna tuning AT command details (TBD), refer to *[1] HL7900 AT Command Reference Guide (Doc# 41114811).*

The HL7900/HL7900E applies a default configuration that assigns a specific frequency range to each port. Customers can select an antenna tuning part via AT command.

Default frequency range settings are:
- RF1: 698–803 MHz
- RF2: 804–960 MHz
- RF3: 1710–1880 MHz
- RF4: 1881–2200 MHz

If a non-default frequency range is required (e.g., a customer chooses not to use a default setting), contact Semtech to request a customized firmware file (BSP) based on the customer's requirements and then deploy it to the module.

7: Reliability Specification

The HL7900/HL7900E will be tested against the Industrial Reliability Specification defined below.

7.1 Preconditioning Test

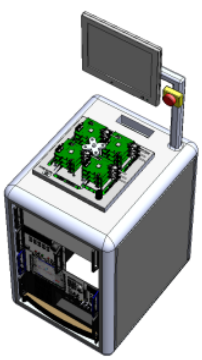
Per JESD22A113, this tests the preconditioning of non-hermetic surface mount devices prior to reliability testing.

Table 7-1: Preconditioning Test

Designation	Condition
Preconditioning Test PCRM	2 reflow cycles with Tmax 245-250°C

7.2 Performance Test

Table 7-2: Performance Test

Designation	Condition
Performance Test PT3T & PTRT 	Standard: N/A

	Special conditions:
	▪ Temperature:
	  ▪ Class A: -30°C to+70°C
	  ▪ Class B: -40°C to +85°C
	  ▪ Rate of temperature change: ± 3°C/min
	▪ Recovery time: 3 hours

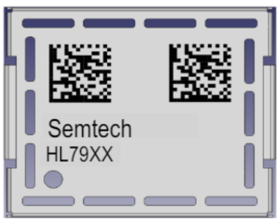
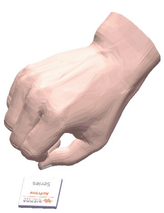
	Operating conditions: Powered
	Duration: 14 days

7.3 Aging Tests

Table 7-3: Aging Tests

Designation	Condition
High Temperature Operating Life test HTOL	Standard: IEC 60068-2-2, Test Bb
	Special conditions: ▪ Temperature: +85°C ▪ Temperature variation: 1°C/min
	Operating conditions: Powered ON with a power cycle of 45 minutes ON and 15 minutes Idle
	Duration: 20 days
Thermal Shock Test TSKT	Standard: IEC 60068-2-14, Test Na
	Special conditions: ▪ Temperature: -40°C to +85°C ▪ Temperature Variation: less than 30s ▪ Number of cycles: 300 ▪ Dwell Time: 10 minutes
	Operating conditions: Unpowered
	Duration: 7 days
Humidity Test HUT	Standard: IEC 60068-2-3, Test Ca
 	Special conditions: ▪ Temperature: +85°C ▪ RH: 85%
	Operating conditions: Powered on, DUT is powered up for 15 minutes and OFF for 15 minutes.
	Duration: 10 days

7.4 Characterization Tests

Designation	Condition
Low Temperature and Cold Start Cycles LTCS	Special conditions: ▪ Temperature: -40°C ▪ AT commands read or write memory
	Operating conditions: 5 mins powered ON, 30 mins powered OFF (1 power cycle)
	Duration: 5 days
Component Solder Wettability CSW	Standard: JESD22 - B102, Method 1/Condition C, Solderability Test Method
	Special conditions: ▪ Test method: Surface mount process simulation test (preconditioning 16h ±30 minutes dry bake)
	Operating conditions: Unpowered
	Duration: 1 day
Unprotected Free Fall Test FFT1	Standard: IEC 680068-2-32, Test Ed
	Special conditions: ▪ Number of drops: 6 drops per unit (1 drop per direction: ±X, ±Y, ±Z) ▪ Height: 1m
	Operating conditions: Unpowered
	Duration: 1 day

8: Regulatory Compliance and Industry Certifications

This chapter describes the current certification status of the HL7900/HL7900E. Certifications in other countries may be attained upon customer request—contact your Semtech account representative for details.

Additional testing and certification may be required for the host product with an embedded HL7900/HL7900E module and are the responsibility of the OEM. Semtech offers professional services-based assistance to OEMs with the testing and certification process, if required.

Important: *Regulatory approval testing for the HL7900E module is in progress. This chapter will be updated accordingly upon completion of its certification.*

8.1 Compliance Acceptance and Certification

The HL7900/HL7900E is designed to be compliant with the 3GPP Release 14 E-UTRA Specification for Mobile Terminated Equipment.

Final regulatory and operator certification requires regulatory agency testing and approval with the fully integrated UE host device incorporating the HL7900/HL7900E.

The OEM host device and, in particular, the OEM antenna design and implementation will affect the final product functionality, RF performance, and certification test results.

Note: Tests that require features not supported by the HL7900/HL7900E (as defined by this document) are not supported.

8.2 Regulatory Compliance

The HL7900/HL7900E module meets the requirements of the following regulatory bodies and regulations, where applicable:

- Federal Communications Commission (FCC) of the United States
- Innovation, Science and Economic Development Canada (ISED)
- Radio Equipment Directive (RED) and RoHS Directive of the European Union
- The National Communications Commission (NCC) of Taiwan, Republic of China
- Japan Ministry of Internal Affairs and Communications (MIC)

8.2.1 Important Compliance Information for Canada and the United States

The HL7900 and HL7900E modules have been granted modular approval for mobile applications under:

- **HL7900**
  - FCC ID: N7NHL79
  - IC: 2417C-HL79
- **HL7900E**
  - FCC ID: N7NHL79E

- IC: 2417C-HL79E

Integrators may use the HL7900/HL7900E module in their host products without additional FCC/ISED certification if they meet the following conditions. Otherwise, additional FCC/ISED approvals must be obtained.

1. The host product must use the RF trace design approved for the HL7900/HL7900E module. The Gerber file of the trace can be obtained from Semtech upon request.
2. At least 20 cm separation distance between the antenna and the user’s body must be maintained at all times.
3. To comply with FCC/ISED regulations limiting both maximum RF output power and human exposure to RF radiation, the maximum antenna gain including cable loss in a mobile-only exposure condition must not exceed the limits stipulated in Table 8-1.
4. The HL7900/HL7900E may transmit simultaneously with other collocated radio transmitters within a host product, provided the following conditions are met:
   - Each collocated radio transmitter has been certified by FCC/ISED for mobile application.
   - At least 20 cm separation distance between the antennas of the collocated transmitters and the user’s body must be maintained at all times.
   - The radiated power of a collocated transmitter must not exceed the EIRP limit stipulated in Table 8-2.

Table 8-1: HL7900/HL7900E Antenna Gain Specifications

Device	Technology	Band	Frequency (MHz)	Maximum antenna gain (dBi)	
				Standalone	Collocated
HL7900/HL7900E	LTE[a]	B2	1850–1910	8.5	6.5
		B4	1710–1755	5.5	5.5
		B5	824-829	6.5	4.0
		B12	699-716	6.1	3.6
		B13[b]	777-787	6.4	4.0
		B25	1850-1915	8.5	6.5
		B26	814-849	6.5	4.0
		B66	1710-1780	5.5	5.5
		B70	1695-1710	5.5	5.5
		B85	698-716	5.5	3.6

a. The isolation between LTE and GNSS antenna is at least 15dB.
b. The antenna gain at 1560MHz suggests less than 3dBi for FCC radiation spurious.

Table 8-2: HL7900/HL7900E Collocated Radio Transmitter Specifications

Device	Technology	Frequency (MHz)	EIRP Limit (dBm)
Collocated transmitters[a]	WLAN 2.4 GHz	2400–2500	30
	WLAN 5 GHz	5150–5850	30
	BT	2400–2500	16

a. Valid collocated transmitter combinations: WLAN+BT; WiGig+BT. (WLAN+WiGig+BT is not permitted.)

5. A label must be affixed to the outside of the end product into which the HL7900/HL7900E is incorporated, with a statement similar to the following:
    - **HL7900: This device contains FCC ID: N7NHL79/ IC: 2417C-HL79**
    - **HL7900E: This device contains FCC ID: N7NHL79E/ IC: 2417C-HL79E**
6. A user manual with the host product must clearly indicate the operating requirements and conditions that must be observed to ensure compliance with current FCC/ISED RF exposure guidelines.

Note: Host product manufacturers are responsible for the overall compliance of the host products including, where applicable, all additional equipment authorization and testing not covered by the modular approval (e.g., unintentional radiator FCC Part 15 Subpart B requirements, ISED's Interference-Causing Equipment Standards, and RF exposure requirements for host products intended for use within 20 cm of the user's body.)

8.2.2 Japan Radio and Telecom Approval

The HL7900/HL7900E modules have been granted Japan radio and telecom approvals with the approval numbers shown below:

- **HL7900**
    - with SRD

      R 003-240246
      T D240038003
    - without SRD

      R 003-250287
      T P250250003
- **HL7900E**

  R 003-260023
  T P260020003

8.2.2.1 Transmission restriction note and carrier sense requirement for Sub-GHz regulation

Note: Wi-SUN(SRD) support is hardware SKU-dependent. For details, contact your Semtech account representative.

2 Transmitters				Reference	
Rated Output	Type and Frequency Range of transmittable radio wave		Modulation		
0.02 W	F1D	920.6–928.0 MHz (200 kHz interval 38 channels)	Modulation: FSK Data rate: Up to 50 kbps	Wi-SUN FAN 1B, Juta, HAN	n=1 (200 kHz)

2 Transmitters				Reference	
Rated Output	Type and Frequency Range of transmittable radio wave		Modulation		
0.02 W	F1D	920.7–927.9 MHz (200 kHz interval 37 channels)	Modulation: FSK Data rate: Up to 100 kbps	Wi-SUN FAN 2B, Juta, HAN	n=2 (400 kHz)
0.02 W	F1D	920.8–927.8 MHz (200 kHz interval 36 channels)	Modulation: FSK Data rate: Up to 200 kbps	Wi-SUN FAN 4B	n=3 (600 kHz)

Transmission Time restriction (on application side, i.e., on the host product)

- Transmission ON: ≤ 0.4 s; Transmission OFF: > 0.002 s
- Total transmission time: ≤ 720 s/h (each radio channel: ≤ 360 s/h)
- Note: The integrator must implement this restriction on the host product.

Carrier Sensing Function

- Carrier sense decision time: ≥ 128 µs
- Carrier sense implementation level: ≥ -80 dBm

Note: Please contact our distributor if you have any questions.

8.3 Industry Certifications

The HL7900/HL7900E module complies with the mandatory requirements described in the following standards. The exact set of requirements supported is network operator-dependent.

Table 8-3: Standards Compliance

Technology	Standards
5G NR	3GPP Release 17
LTE	3GPP Release 14
WCDMA	3GPP Release 99

The following industry certifications have been obtained, where applicable:

- GCF
- PTCRB

8.4 Disposing of the Product

This electronic product is subject to the EU Directive 2012/19/EU for Waste Electrical and Electronic Equipment (WEEE). As such, this product must not be disposed of at a municipal waste collection point. Please refer to local regulations for directions on how to dispose of this product in an environmentally friendly manner.

A: Appendix

For more details, several references can be consulted, as detailed below.

A.1 Website Support

Check source.sierrawireless.com for the latest documentation available for HL7900/HL7900E modules.

A.2 List of References

[1] HL7900 AT Command Reference Guide (Doc# 41114811)

[2] HL7900/HL7900E Migration Guide (Doc# 41114810)

[3] Semtech Ready-to-Connect Module Integration Guide (Doc# 41113385)

[4] HL79 Customer Process Guidelines (Doc# 41114868)

[5] HL79 Wi-Fi User Guide (Doc# 41114970)

A.3 Terms and Abbreviations

Table A-1: Terms and Abbreviations

Term / Abbreviation	Definition
Active state	All sub-systems, including the MAP process, are up and running. User can access module via UART (e.g. to configure/query module settings/states, and send/receive data.
ADC	Analog to Digital Converter
AT	Attention (prefix for modem commands)
AT-READY	Module is initialized and ready to accept AT commands
Cat-M1	LTE enhanced Machine Type Communication (eMTC) Category M1 (3GPP Release 14)
Cat-NB1	LTE Narrowband Internet of Things (NB-IoT) Category NB1 (3GPP Release 14)
CF3	Common Flexible Form Factor
CLK	Clock
DTR	Data Terminal Ready
DRX	Discontinuous Reception
eDRX	Extended DRX
EIRP	Equivalent Isotropically Radiated Power
EMC	Electro-Magnetic Compatibility
EMI	Electro-Magnetic Interference
EN	Enable
ESD	Electro-Static Discharges
ETSI	European Telecommunications Standards Institute
GLONASS	Global Navigation Satellite System
GND	Ground
GNSS	Global Navigation Satellite System
GPIO	General Purpose Input Output
GPRS	General Packet Radio Service
GPS	Global Positioning System
GSM	Global System for Mobile communications
Hi-Z	High impedance (Z)
IC	Industry Canada
I/O	Input/Output
LED	Light Emitting Diode
MAX	Maximum

Table A-1: Terms and Abbreviations (Continued)

Term / Abbreviation	Definition
MIN	Minimum
N/A	Not Applicable
PA	Power Amplifier
PC	Personal Computer
PCB	Printed Circuit Board
PCL	Power Control Level
periodic TAU	See TAU
PSM	Power Save Mode
PTW	Paging Transmission Window
PWM	Pulse Width Modulation
RF	Radio Frequency
RST	Reset
RTC	Real Time Clock
RX	Receive
SHUB	Sensor Hub
SIM	Subscriber Identification Module
SINR	Signal to Interference plus Noise Ratio
SPI	Serial Peripheral Interface
SRD	Short Range Device
SW	Software
TAU	Tracking Area Update ▪ TAU—An update sent when the PSM parameters are changed or when the module changes location. ▪ periodic TAU—Sent by the module to notify its availability to the network.
TBC	To Be Confirmed
TBD	To Be Determined To Be Defined
TP	Test Point
TX	Transmit
TYP	Typical
UART	Universal Asynchronous Receiver-Transmitter
UICC	Universal Integrated Circuit Card
UIM	User Identity Module

Table A-1: Terms and Abbreviations (Continued)

Term / Abbreviation	Definition
UMTS	Universal Mobile Telecommunications System
USIM	UMTS Subscriber Identity Module
VBAT_BB	Main Supply Voltage from Battery or DC Adapter
VSWR	Voltage Standing Wave Ratio

A.4 Ordering Information

Table A-2: Ordering Information

Model Name	Description	Part Number
HL7900/HL7900E	HL7900/HL7900E embedded module	Contact Semtech for the latest SKU.
DEV-KIT	HL781x Development Kit	6001458