Configuring I2S on Melody

Application Note

SIERRA WIRELESS®

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Revision History

Revision number	Release date	Changes
1	March 22, 2017	Initial revision in SWI template.

Contents

1: Introduction

The BC127 and Melody Audio support a configurable and I2S specification compliant digital audio interface.

Melody exposes a wide range of configuration parameters for the I2S interface that allow customers to re-configure the bus to work with their existing hardware and with non-I2S standard configurations.

This document aims to give a quick overview of the I2S standard. The full specification can be found on the Internet.

This document also aims at explaining the relevant audio interface settings for Melody and well as the full set of I2S configuration parameters.

Finally, this document provides a set of example configurations that aim to explain how the configurations work for different pre-defined scenarios.

2: The I2S Standard

The I2S standard in short:

- Time multiplexed serial protocol
- There are two main types of device roles
  - Transmitter - sends audio data
  - Receiver - receives audio data
  - A device can be both by sharing clock lines and having separate serial lines or by implementing them on different busses
- There are two types of bus roles
  - Master - supplies SCL and WCL
  - Slave - receives SCL and WCL
  - No implication regarding data transfer direction
  - A device that is both transmitter and receiver by using shared clock lines, may not have different bus roles for the two device roles.
- Requires three signals for one directional transfer
  - SCL (or Bit clock) the serial clock - supplied by master at the rate bits are transferred over the data line
  - WCL (or LRCLK) the word clock, supplied by master, indicating if the left or right channel data is currently being sent - this is set to the sampling rate of the signal
  - SDA - the serial data line
- SDA requirements
  - MSbit transmitted first
  - MSbit transmitted 1 SCL after WCL transition
  - Word length independent, line must be low when no data is transmitted. All received bits after the receiver word length should be ignored.
  - Data must be valid on rising edge of SCL
  - SDA data during WS Low (0) is Channel 1 (Left)
  - Data is 2's complement

3: Melody I2S Configurations Overview

The Melody Audio interface is configured via several separate configurations commands.

`AUDIO=mode` -> used to select Master I2S bus mode (3) or Slave I2S mode (4)

`CODEC=X Fs stereo X X` -> used to set the sample rate and mono/stereo mode for audio output/input

`BPS=bps` -> used to set the bits per sample for audio.

Please note that the BC127 native word size is 16 and values larger than that will result in the extra bits (on the leas significant side) being padded with 0 at the output.

For I2S receiver (input) resolution, please look at Justify Resolution of Data in the I2S configuration below, to set appropriate input resolution. Also, for resolutions higher than 16 bps, please look at the receiver crop and attenuation configurations and the section below that explains the difference and goes through what needs to be considered to ensure the best audio quality.

`I2S=I2S_CONFIG` -> this is used to set I2S specific settings, described in more detail below.

4: Melody I2S configuration Overview

The I2S configuration is an 11-bit value represented by the 11 LSB of a 4-digit hexadecimal number with the following bit positions setting the following I2S driver specific settings:

- **Bit [0]: Justification Format with respect to WCL transition:**
  - 0 – Left justified (MSbit of data occurs after WCL transition as specified In Left Justify Delay, if more than 16 SCL per word slot are issued, remaining LS bits are padded with 0);
  - 1 – Right justified (the LSbit of data is sent in SCL immediately before WCL transition, MSbits are padded with 0s if more than 16 SCL per word slot are issued). For the bus to be I2S compliant, this needs to be 0.
- **Bit [1]: Left Justify Delay:**
  - 0 – MSbit of SD data occurs in the first SCLK period following WS transition;
  - 1 – MSbit of SD data occurs in the second SCLK period. For the bus to be I2S compliant, this needs to be 1.
- **Bit [2]: Channel polarity:**
  - 0 – SD data is left channel when WS is high;
  - 1 – SD data is right channel. For the bus to be I2S compliant, this needs to be 1.
- **Bit [3]: Audio attenuation enable (On SD_IN):**
  - 0 – 17-bit SD data is rounded down to 16 bits;
  - 1 – The audio attenuation defined in bits [7:4] is applied over 24 bits with saturated rounding. This setting requires Bit [10] to be 0. This is used when the I2S bus is used at input BPS larger than 16 and crop is disabled.
- **Bits [7:4]: Audio attenuation: in 6dB steps:**
  - If the crop enable bit is set to 0, and Audio attenuation is set to 1, then this audio attenuation is applied to the received data word (on 24bits with saturated rounding) before it is passed internally as a 16-bit values. This scales down any input larger than 16 bits so that it fits the native word size. This feature is useful when the input word size does not use the full dynamic range of a 24-bit word and therefore cropping the LSB would result in very poor performance.
- **Bits [9:8]: Justify resolution of data on SD_IN:**
  - This is used to set the input resolution and is a mandatory configuration for right justified mode or if the input SCL will provide more clocks per WCL that the sample bit depth transmitted.
  - 00 – 16-bit
  - 01 – 20-bit
  - 10 – 24-bit
  - 11 – Reserved.
- **Bit [10]: 16 bit crop enable:**
  - 0 – 17-bit SD_IN data is rounded down to 16bits;
  - 1 – Only the most significant 16bits of data are received. The simplest way to convert input data larger than 16-bit into 16-bit input for the module. This results in loss of precision and detail, and may result in the softer parts of received audio being interpreted as silence. (Lowest 8 bits from 24-bit input word will be discarded).

5: I2S Receiver Crop and Attenuation

The Melody audio sub-system operates natively at 16-bit resolution.

The I2S receiver interface can be configured to operate at 16, 20, and 24 BPS through the *I2S_CONFIG* configuration.

When operating at bit resolutions higher than 16 bits, the receiver behaviour can be configured.

By default, the receiver operates in compliance with the I2S specification, and crops (truncates) values to the native audio interface bit resolution by taking the most significant 16 bits of the signal.

Additionally, the user can configure attenuation which operates on 24 bits.

Which of the two approaches produces better results depends entirely on the input signal characteristic. Details and considerations are discussed below:

Attenuation is going to take the 24-bit number and perform attenuation in 6dB steps (amplitude division by 2) with saturated rounding to a 16-bit value on the result.

> e.g. For a maximum amplitude sent over I2S of 0x7FFFFF attenuated by 6dB would be 0x3FFFFF, which would then be saturation rounded to 0x7FFF (max positive for the 16bit word); This means that if you are sending values as high as 0x7FFFFF (max positive for 24bit word) you will be introducing a lot of saturation, which would lead to severely degraded audio quality.

If your source signal is strong and the topmost 16 bits are used, I would suggest using truncation. That will discard the lowest 8 bits, so you will lose some precision from your 24-bit source but that is unfortunately inevitable, but no saturations would occur.

e.g. For a maximum value sent over I2S of 0x7FFFFF, truncation results in a value of 0x7FFF and no saturation artifacts.

If your input signal, while in 24 bits is not using some of the higher bits, because signal amplitude is low, it is worthwhile using attention to extract as much precision as you can from your signal.

> e.g. For a maximum signal amplitude sent over I2S of 0x01FFFF attenuated by 12dB would give 0x7FFF which would be saturation rounded to 0x7FFF; If truncation was used the value would be 0x01FF, thus removing 7 bits of precision.

6: Example Configurations

The configurations are provided as explain to illustrate how the different settings are applied to the Melody audio interface.

The configurations below need to be supplied to Melody as per the Melody manual using the *SET* command. All configurations can be then permanently stored as per Melody Manual using the *WRITE* command and applied on next boot by typing *RESET* command.

Regardless of permanent status, the changes will take effect on next audio interface activation.

Please note that for the digital audio interface to be operational on the BC127 board, the SPI/PCM# pin on the module or switch on the Development/Discovery Kit has to be de-asserted/in PCM# mode. Otherwise, the SPI lines will be multiplexed on the PCM header and no digital audio output will be possible.

1. 16-bit, 48000Hz, stereo, as I2S Master, SBC only, I2S compliant

```
AUDIO=3 // I2S master
BPS=16 // 16 bits per sample
CODEC=0 48000 1 // SBC 48kHz Stereo
I2S=0406 // Crop input to 16 bit, WS low for L channel,
// 1 clock delay
```

2. 16-bit, 44100Hz, stereo, as I2S Slave, SBC only, I2S compliant

```
AUDIO=4 // I2S slave
BPS=16 // 16 bits per sample
CODEC=0 44100 1 // SBC 44.1kHz Stereo
I2S=0406 // Crop input to 16 bit, WS low for L channel,
// 1 clock delay
```

3. 16-bit, 48000Hz, stereo audio, as I2S Master, SBC only, reversed channel polarity, no MSB delay

```
AUDIO=3 // I2S master
BPS=16 // 16 bits per sample
CODEC=0 48000 1 // SBC 48kHz Stereo
I2S=0400 // Crop input to 16 bit, WS high for L channel,
// no left justify delay
```

4. 16-bit, 48000Hz, stereo audio, as I2S Master, SBC only, reversed channel polarity, no MSB delay, right justified

```
AUDIO=3 // I2S master
BPS=16 // 16 bits per sample
CODEC=0 48000 1 // SBC 48kHz Stereo
I2S=0401 // Crop input to 16 bit, right justify resolution,
// 16 bit, reverse channel polarity, right justify
```

5. 24-bit, 48000, stereo audio, as I2S Master, SBC only, I2S compliant, 12dB attenuation

```
AUDIO=3 // I2S master
BPS=24 // 24 bits per sample
CODEC=0 48000 1 // SBC 48kHz Stereo
I2S=022E // justify resolution 24bit, 12dB attenuation,
// attenuation enabled, WS low for L channel,
// 1 clock delay
```

7: Change Log

- **R40**
  - Added clarifications on I2S receiver truncation and attenuation concepts
  - Added description of number representation format used by the interface
- **R30**
  - Updated examples for I2S WS polarity compliance
  - Added Change Log and TOC
  - Expanded introduction
  - Minor layout changes
- **R20**
  - Clarified how settings are stored and applied on Melody
  - Added note about SPI/#PCM select switch
- **R10**
  - Initial release