



Product Technical Specification/ Customer Design Guidelines

AirPrime Q26Elite Module



SIERRA
WIRELESS

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>> 1. Overview

This document presents the details regarding the product technical specifications, design, and features of the AirPrime Q26Elite Intelligent Embedded Module and all derivatives, enabling the customer to understand the functions, capabilities and interfaces of the module and how to integrate it into a viable product or application.

This document applies to the AirPrime Q26Elite and all software variations available for this product.

1.1. References

1.1.1. Reference Documents

Ref	Doc No	Name
[1]	WI_DEV_Q26EL_UGD_001	AirPrime Q26Elite Software Users Guide and AT Commands Interface Specification
[2]	WM_PRJ_Q2686_PTS_004	Q26 Series Process Customer Guidelines
[3]	WM_BBD_Q26_UGD_001	Q26 Series Development Kit User Guide
[4]	WI_PGM_Q24x8_PTS_001	Q24X8 CDMA RoHs Product Technical Specification

1.1.2. Abbreviations

Abbreviation	Definition
ADC	Analog to Digital Converter
A/D	Analog to Digital conversion
AF	Audio-Frequency
AGC	Automatic Gain Control
AT	ATtention (prefix for modem commands)
AUX	AUXiliary
CAN	Controller Area Network
CBS	Cell Broadcast Service
CDMA	Code Division Multiple Access
CEP	Circular Error Probable
CLK	Clock
CMOS	Complementary Metal Oxide Semiconductor
CODEC	COder DECoder
CPU	Central Processing Unit
CS	Coding Scheme
CSD	Circuit Switched Data
CTS	Clear To Send
DAC	Digital to Analog Converter
DAI	Digital Audio Interface

Abbreviation	Definition
dB	Decibel
DC	Direct Current
DCD	Data Carrier Detect
DCE	Data Communication Equipment
DR	Dynamic Range
DSR	Data Set Ready
DTE	Data Terminal Equipment
DTR	Data Terminal Ready
EMC	ElectroMagnetic Compatibility
EMI	ElectroMagnetic Interference
EMS	Enhanced Message Service
EN	Enable
ESD	ElectroStatic Discharges
ETSI	European Telecommunications Standards Institute
FIFO	First In First Out
GND	GrouND
GPI	General Purpose Input
GPIO	General Purpose Input Output
GPO	General Purpose Output
GPRS	General Packet Radio Service
GPS	Global Positioning System
GPSI	General Purpose Serial Interface
GSM	Global System for Mobile communications
Hi Z	High impedance (Z)
IC	Integrated Circuit
IF	Intermediate Frequency
IMEI	International Mobile Equipment Identification
I/O	Input / Output
LCD	Liquid Crystal Display
LED	Light Emitting Diode
LNA	Low Noise Amplifier
LSB	Less Significant Bit
MAX	MAXimum
MIC	MICrophone
MIN	MINimum
MMS	Multimedia Message Service
MO	Mobile Originated
MS	Mobile Station
MT	Mobile Terminated
NF	Noise Factor
NMEA	National Marine Electronics Association
NOM	NOMinal
PA	Power Amplifier

Abbreviation	Definition
Pa	Pascal (for speaker sound pressure measurements)
PC	Personal Computer
PCB	Printed Circuit Board
PCL	Power Control Level
PCM	Pulse Code Modulation
PWM	Pulse Width Modulation
RAM	Random Access Memory
RF	Radio Frequency
RFI	Radio Frequency Interference
RHCP	Right Hand Circular Polarization
RI	Ring Indicator
RMS	Root Mean Square
RST	ReSeT
RTC	Real Time Clock
RTS	Request To Send
RX	Receive
SCL	Serial CLock
SDA	Serial Data
SIM	Subscriber Identification Module
SMD	Surface Mounted Device/Design
SMS	Short Message Service
SPI	Serial Peripheral Interface
SPL	Sound Pressure Level
SPK	SpeaKer
SRAM	Static RAM
TBC	To Be Confirmed
TDMA	Time Division Multiple Access
TP	Test Point
TTL	Transistor to Transistor Logic
TU	Typical Urban fading profile
TUHigh	Typical Urban, High speed fading profile
TX	Transmit
TYP	TYPical
UART	Universal Asynchronous Receiver-Transmitter
UBX	µ-blox proprietary protocol (NE DOIT PAS APPARAITRE)
USB	Universal Serial Bus
VSWR	Voltage Standing Wave Ratio
WAP	Wireless Application Protocol

2. CDMA Introduction

Code Division Multiple Access (CDMA), a cellular technology also known as IS-95, competes with GSM technology for dominance in the cellular world. There are now different variations, but the original CDMA is now known as cdmaOne. Developed originally by Qualcomm and enhanced by others, CDMA is characterized by high capacity and small cell radius, employing spread-spectrum technology and a special coding scheme. The Telecommunications Industry Association (TIA) adopted CDMA, in 1993.

In 1999 a new third generation (3G) standard was accepted, of which CDMA2000 is one of three operating modes (WCDMA and TD-SCDMA are the other two).

The module provides peak data rates of up to 153 kbps, without sacrificing voice capacity for data capabilities. It allows for extended battery life in the product, and twice the system capacity for the Carrier over earlier products. The module detailed in this document is based on this CDMA 2000/1XRTT technology.

3. Product Description

Designed for fast and easy integration, the AirPrime Q26Elite Intelligent Embedded Module is a Dual Band (800/1900 MHz) product. The module provides end application devices with wireless connectivity, high-speed data transfer, and advanced features such as gpsOne, TCP/IP, and voice. The AirPrime Q26 Series is designed to target the vertical applications market space such as automotive applications, Telematics, Machine-to-Machine Interfaces and Mobile Professional Applications. This module is also designed for integration in Dual Processor applications.

3.1. Product Features

3.1.1. Wireless Interface

- CDMA2000 1XRTT (IS-2000) - (Dual Band)
- Band class 0 (TX: 824 ~ 849 MHz/ RX: 869 ~ 894 MHz)
- Band class 1 (TX: 1850 ~ 1910 MHz/ RX: 1930 ~ 1990 MHz)
- Data rates up to 153 kbps forward and reverse
- GPS L1 support

3.1.2. Hardware

- Operating Voltage: 3.8V to 4.2V (4.0V nominal)
- Output Power: 0.25W CDMA
- Audio Interfaces
 - Two Differential Analog audio paths
 - PCM
- USB 2.0 Full Speed (Peripheral-only)
- Two UARTs (Only one UART if RUIM is supported)
- Two ADC Channels
- 20 GPIOs
 - Four - 1.8V I/Os
 - 16 - 2.6V I/Os
- Battery Charging
- Network Status LED sink
- HW Features not currently supported by Software
 - Keypad (5x5 matrix)
 - I2C Interface
 - Vibration Motor
 - RTC

3.1.3. Software

- CDMA2000 Release A
- IS-637: Short Message Service (Mobile Originated and Mobile Terminated)

- Async data service
- Circuit-switched data
- Packet Data (Mobile IP, Simple IP)
- EIA-683A: OTASP, OTAPA
- gpsOne position location capabilities
- RUIM (for Asia Pacific countries)
- TCP/IP
- 3GPP 27.010 Multiplexing
- Carrier Support Software
- Provisioning for Carrier Requirements

3.1.4. Mechanical

- Dimensions: 40 x 32.2 x 6.63 (mounting height)
- Weight: 11 grams
- 100 pin System Connector
- Coaxial RF Connector (Coax Cable to application not included)
- RF Shielding

3.1.5. Environmental

- Operating Temperature: -40°C to +85°C Maximum Rating
- Storage Temperature: -40°C to +85°C
- RoHs Compliance
- Lead Free Compliance

3.2. Part Number

WM21662 PRODUCT WCPU < WMQuik > Q26 Series, 1xRTT QSC

3.3. Functional Architecture

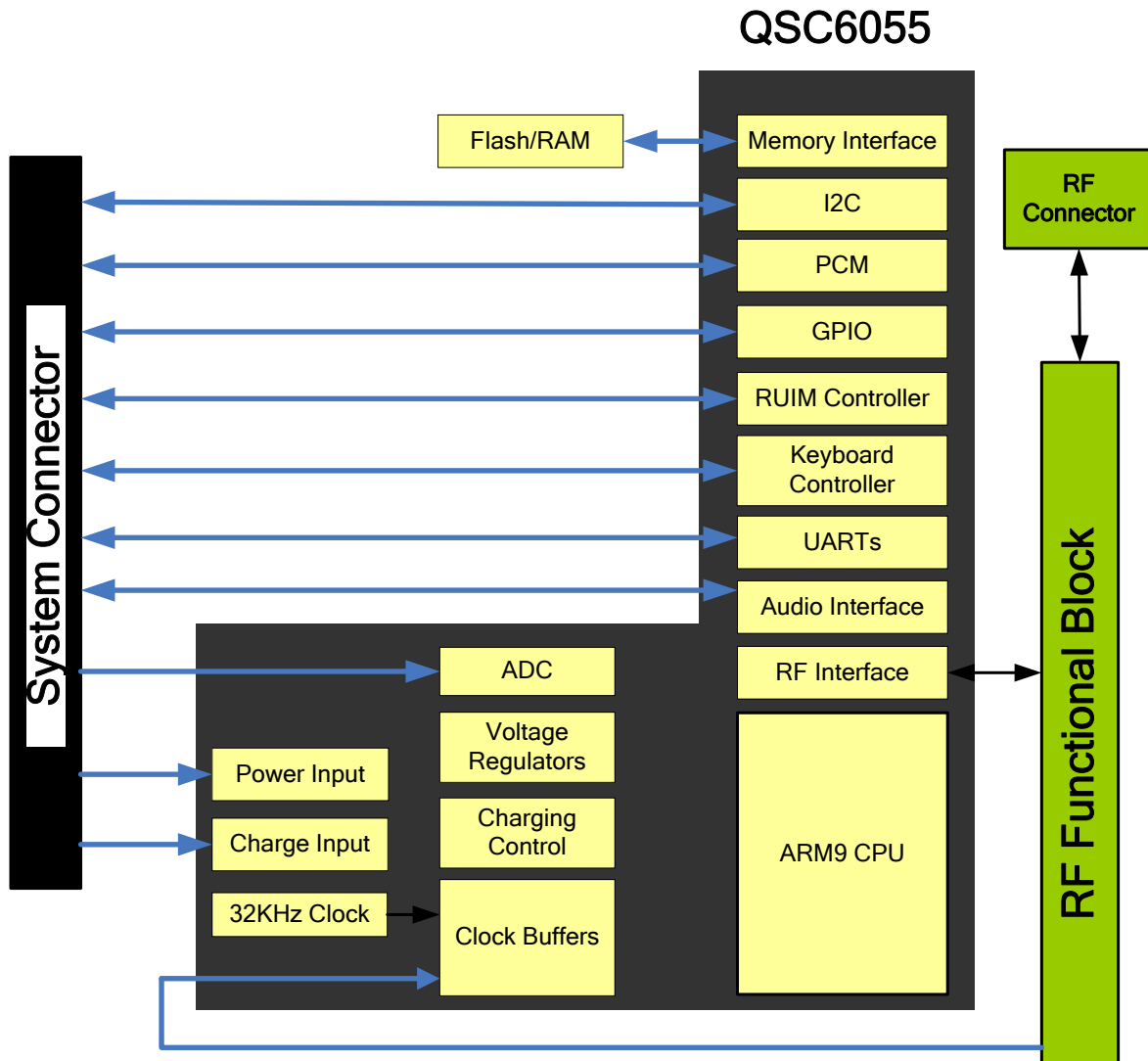


Figure 1. Functional architecture

3.4. Absolute Maximum Ratings

The table below defines the Absolute Maximum Ratings for the AirPrime Q26Elite module.

Table 1: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units
To	Operating Temperature	-40	+85	°C
Ts	Storage Temperature	-40	+85	°C
VBATT	Power Supply input	-0.5	4.2	V
VUSB	VPAD_USB	-0.5	7.0	V
CHG_IN	Charger Input	-0.5	18	V
VI/O	Voltage on any non power supply pin	-0.3	VXX + 0.3	V
VESD-ANT	Voltage Air Discharge to Antenna		15	kV
VESD-INT	Voltage Contact Discharge to Surface		6	kV
VESD-I/O	Voltage Contact Discharge to I/O Connector		2	kV

3.5. Recommended Operating Conditions

The table below defines the Recommended Operating Conditions for the AirPrime Q26Elite module.

Table 2: Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
To	Operating Temperature (Class A) ¹	-30		+70	°C
	Operating Temperature (Class B) ^{2,3}	-40		+85	°C
Ts	Storage Temperature	-40		+85	°C
VBATT	Power Supply input	3.8	4.0	4.2	V
VUSB	VPAD_USB	4.4	5.0	5.6	V
CHG_IN	Charger Input	4.5	4.7	4.9	V
VI/O	Voltage on any non power supply pin	0		VXX + 0.2	V
VCOIN	Coin cell voltage (backup)	1.5	3.0	3.25	V

¹ Fully functional and meets radio performance criteria as defined by 3GPP2 C.S0011-A over the specified temperature range.

² Fully functional with degraded radio performance.

³ A heat sink is recommended for use above +75°C.

4. Hardware Interfaces

4.1. Power and Ground

4.1.1. Power Supply

The VBATT power supply input provides power to the entire AirPrime Q26Elite module. The system connector pins are identified in the table below.

Table 3: Power Supply Input Pins

Pin Number	Signal Name	Voltage	I/O*	Description
1	VBATT	VBATT	I	Power Supply
2	VBATT	VBATT	I	Power Supply
3	VBATT	VBATT	I	Power Supply
4	VBATT	VBATT	I	Power Supply

The input power supply voltage requirements can be found in the table below.

Table 4: Power Supply Voltage Specification

Supply	Vmin	Vnom	Vmax	Units
VBATT	3.8	4.0	4.2	V

4.1.2. Ground

There are no Ground (GND) pins defined in the system connector. The application must ensure that the four mounting tabs of the AirPrime Q26Elite are soldered to GND and this is common to the GND of the Power Supply.

4.1.3. Current Consumption

The input power supply current requirements can be found in the table below.

Table 5: Power Supply Current Specification

Parameter		Typical	Max	Units
On Call	Maximum TX Output	-	700	mA
	+0dBm TX Output	157	-	mA
Idle	Registered	45	-	mA
	Searching	100	-	mA
Sleep Mode	Average current, SCI=2	-	5	mA
Off Mode Current		-	10	μA

Note: The Power Supply Current Specification assumes no loads on the GPIOs.

Tip: *When designing a host power supply, it is recommended that it be designed to source 2x the Maximum TX Output Power current in Power Supply Current Specification.*

4.1.3.1. Sleep mode

The AirPrime Q26Elite supports a low power mode in which the device is registered on the CDMA network and sleeps in between wake intervals where it listens for pages. The period of the wake interval is defined by the Slot Cycle Index.

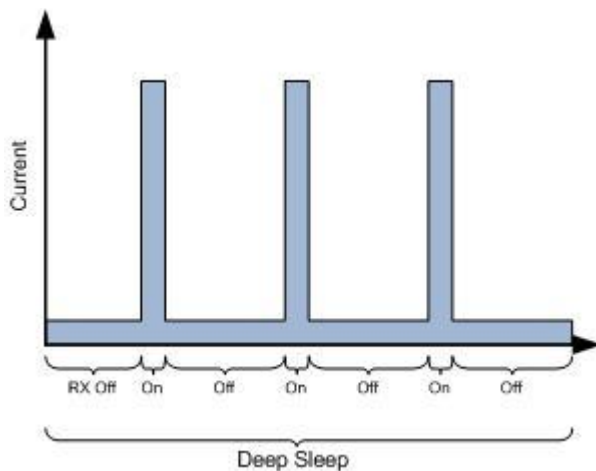


Figure 2. Power mode diagram

The Slot Cycle Index is the lower of the values stored in the AirPrime Q26Elite or the value being broadcast by the wireless network that the AirPrime Q26Elite is registered on.

While in Deep Sleep mode the functions of the AirPrime Q26Elite are limited as defined the following table.

Table 6: Deep Sleep function availability

Function	Availability	Conditions
Paging	Required	
GPS	Not Available	GPS is powered down
USB	Not Available	USB_VBUS is not applied
UART	Not Available	
Digital IO	Not Available	Digital IO pins are high-Z

Events that will cause the AirPrime Q26Elite to wake-up from Deep Sleep mode include:

- Incoming call
- USB_VBUS is applied to the AirPrime Q26Elite
- Interrupt on GPIO40
- DTR is asserted, if AT+W32K=1,1 is used to enter sleep mode

4.1.4. Logic Reference Voltages

Logic Reference Voltage outputs are provided to ensure that incoming signals are within the limits of the AirPrime Q26Elite.

Table 7: Logic Reference Voltages

Pin Number	Signal Name	Voltage	I/O*	Description
5	VCC_1V8	VCC_1V8	O	1.8V Supply Output
10	VCC_2V6	VCC_2V6	O	2.6V Supply Output

These signals should be used to gate communication with the AirPrime Q26Elite from an external application. They are low when the AirPrime Q26Elite is in the OFF state.

Table 8: VCC_Out Pin Specifications

	VCC_1V8	VCC_2V6
Voltage (V)	1.8 Vdc	2.6 Vdc
Tolerance	+/- 3%	+/- 3%
Max Current (I)	15 mA	15 mA

4.1.5. VCOIN

Used as an analog input from the 3 V coin cell for SMPL, RTC, and 32 kHz crystal oscillator backup; a capacitor (rather than a coin cell) can be used if only SMPL is supported. Used as an analog output for coin cell or capacitor charging. This interface cannot be used as an auxiliary power source for the AirPrime Q26Elite in normal operation.

Table 9: VCOIN Pin

Pin Number	Signal Name	Voltage	I/O*	Description
7	VCOIN	VCOIN	I/O	Backup battery for SMPL, RTC and 32kHz oscillator.

VBATT is the source for the charge current for VCOIN.

4.1.5.1. Component selection information

If only the SMPL feature is required a 6.8 uF capacitor to GND must be placed on the VCOIN pin in the application.

If the RTC function is required and VBATT will be removed then a coin cell connected to VCOIN is required in the application. Coin cell charging is provided by the AirPrime Q26Elite. Lithium manganese dioxide rechargeable coin cells are supported. The coin cell charger is implemented using an internal voltage regulator and series resistor, both programmable as defined in the table below.

Table 10: VCOIN Charger settings

	Value(s)	Units
Voltage	3.0, 3.1, 3.2	V
Resistance	800, 1200, 1700, or 2100	Ohms

4.1.6. Charging

The CHG_IN power supply input provides power to the built-in charging circuitry. The system connector pins are identified in the table below.

Table 11: Charging Supply Input Pins

Pin Number	Signal Name	Voltage	I/O*	Description
6	CHG_IN	CHG_IN	I	Charge Supply
8	CHG_IN	CHG_IN	I	Charge Supply

The input charging supply voltage requirements can be found in the table below.

Table 12: Charging Supply Voltage Specification

Supply	Vmin	Vnom	Vmax	Units
CHG_IN	4.5	4.7	4.9	V

The input charging supply current requirements can be found in the table below.

Table 13: Charging Supply Current Specification

Supply	I _{max}	Units
CHG_IN	1000	mA

The built-in charging algorithm in AirPrime Q26Elite supports charging of Li-ion batteries. It utilizes up to four types of charging; trickle, constant current, constant voltage, and pulse charging. Trickle charging is only used on a severely depleted battery. This mode provides a user settable constant current (0 to 80 mA in 10mA steps) and is replaced by constant current charging when the Li-ion battery reaches a user settable threshold. The constant current charging (or fast charging) is used until the battery reaches its target value, after which it is topped of using either constant voltage or pulse charging until it is considered fully charged.

The battery temperature must be monitored. A battery thermistor must be implemented by the application on ADC0. The thermistor map must be generated by the application and stored in AirPrime Q26Elite using the AT+WBTM command.

4.2. Control and Status

4.2.1. ON/OFF Signal

The ON/OFF signal provides external control to initiate a power-up and/or power-down.

Table 14: ON/OFF Pin

Pin Number	Signal Name	Voltage	I/O*	Description
19	ON/~OFF	VBATT	I	ON / ~OFF Control

[Figure 3](#) illustrates the normal Power-ON sequence for the AirPrime Q26Elite.

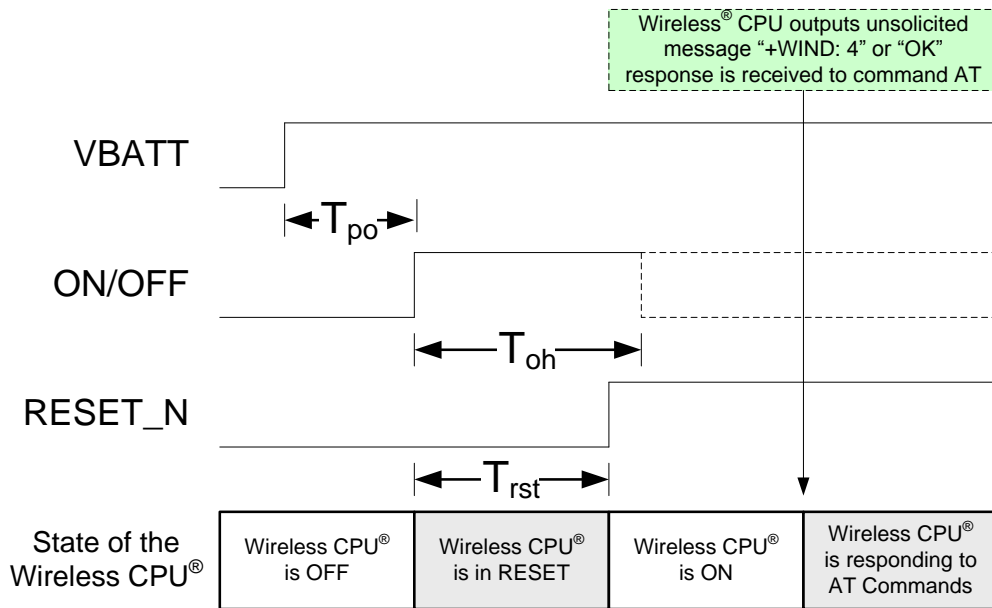


Figure 3. Power-ON Sequence

Table 15: Power-ON Sequence Symbol Definitions

Symbol	Parameter	Min	Typ	Max
T_{po}	Time between when VBATT is stable and ON/OFF signal is asserted	0 s		-
T_{oh}	Duration ON/OFF asserted	4 s		∞
T_{rst}	Duration of Power-ON Reset	50 ms		

The ON/OFF signal can be used as logic level input or as a pulsed input. The AirPrime Q26Elite begins to power-up when the rising edge of the ON/OFF signal. This signal may be left in the high state, used as a logic level input. The preferred method is to transition this signal low after T_{oh} time, pulsed input. This will ensure that it is possible to power-down the unit with either another pulse or an AT command.

The ON/OFF input circuit is shown below in Figure 4. The host should be designed to allow for proper drive strength into the module.

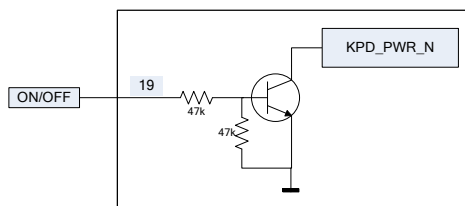


Figure 4. ON/OFF Input Circuit

The table below defines the voltage level characteristics of the ON/OFF signal.

Table 16: ON/OFF Pin Levels

	Min	Max	Units
High Level	3.0	VBATT	V
Low Level		0.8	V

4.2.2. RESET_N Signal

The RESET_N signal is an input signal. This signal is pulled up inside the AirPrime Q26Elite and can be pulled low externally to generate a reset of the AirPrime Q26Elite. It is possible to use this signal to reset the AirPrime Q26Elite but this should be used only when absolutely necessary.

Caution: Use of this signal to RESET the AirPrime Q26Elite could result in memory corruption if used inappropriately. This signal should only be used if the module has become unresponsive and it is not possible to perform a power cycle.

Table 17: RESET pin

Pin Number	Signal Name	Voltage	I/O*	Description
18	RESET_N	VCC_2V6	I	Reset status

An external open drain transistor is recommended in the application to pull the RESET_N low

Table 18: External Open Drain Transistor Recommendations

	Min	Max
Current application must be able to sink	10mA	
Voltage level to generate a Reset		200 mV

4.3. Digital Interfaces

The module Digital Interfaces consists of 6 sub-sections. The sub-sections are UARTs, I2C, PCM, GPIO, Keypad, and Activity Indicators. Each sub-section will be described in detail below. Refer to the [System Connector Pin-out](#) section for details on the connector pin-out and pin type (drive strength, pull up or pull down, etc). Recommendations for the design of interface circuitry are also provided.

4.3.1. Input /Output DC Characteristics

The tables below define the I/O characteristics for the digital I/O signals.

Table 19: Digital I/O characteristics

Parameter	Comments	Min	Max	Unit	
VIH	High-level Input Voltage	CMOS/Schmitt	0.65 x VCC_x.x	VCC_x.x + 0.3	V
VIL	Low-level Input Voltage	CMOS/Schmitt	-0.3	0.35 x VCC_x.x	V
IIH	Input High Leakage Current	No Pull-Downs		1	µA
IIL	Input Low Leakage Current	No Pull-Ups	-1		µA
VOH	High-level Output Voltage	CMOS, at pin rated drive strength	VCC_x.x - 0.45	VCC_x.x	V
VOL	Low-level Output Voltage	CMOS, at pin rated drive strength	0	0.45	V
CIN	Input Capacitance			7	pF

4.3.2. UARTs

The AirPrime Q26Elite provides up to two Universal Asynchronous Receiver Transmitters (UARTs) that communicates with serial data conforming to the RS-232 interface protocol. Each UART requires an external signal level shifter to comply with the RS232 electrical specification. Each UART is dedicated to its specific function. UART1 is for serial communication with the host. UART2 is used for communication with a PC running the Qualcomm Diagnostic Monitor or for communication with an RUIM or SIM card. UART2 and R-UIM are mutually exclusive.

Refer to the following sections for details.

Note: To eliminate the possibility of latch-up, in general all inputs and outputs to the module must be tri-stated or driven LOW by the host when the module is turning OFF. This is particularly true of the serial interface pins, which connect directly to the module processor with no buffering.

Note: All signals on the System Connector are 1.8V or 2.6V logic unless stated otherwise.

4.3.2.1. UART1

The AirPrime Q26Elite UART1 is the main command and control interface. It is the interface where AT commands are sent, unsolicited messages are received and data is transferred.

HW Flow Control is enabled by default. This is the recommended configuration and requires RTS1 and CTS1 to be connected between the AirPrime Q26Elite and the external UART or RS-232 transceiver. If RTS1 and CTS1 are not connected externally a pull-down resistor on RTS1 is required if HW Flow Control has not been disabled in the AirPrime Q26Elite. Consult the AirPrime Q26Elite AT Command Manual for the syntax of the command AT+IFC if, disabling HW Flow Control is desired.

[UART1 Pins](#) defines the UART1 pins available at the system connector. The characteristics such as buffer size, reference voltage and maximum baud-rate supported are listed in [UART1 Specifications](#).

Table 20: UART1 Pins

Pin Number	Signal Name	Voltage	I/O*	Description
69	RI1	VCC_2V6	O	Main RS232 Ring Indicator
70	DCD1	VCC_2V6	O	Main RS232 Data Carrier Detect
71	TXD1	VCC_2V6	I	Main RS232 Transmit
72	RTS1	VCC_2V6	I	Main RS232 Request To Send
73	RXD1	VCC_2V6	O	Main RS232 Receive
74	DSR1	VCC_2V6	O	Main RS232 Data Set Ready
75	CTS1	VCC_2V6	O	Main RS232 Clear To Send
76	DTR1	VCC_2V6	I	Main RS232 Data Terminal Ready

Table 21: UART1 Specifications

UART1 Aspect	Value
Voltage	2.6 Vdc
Size of TX and RX FIFO Buffers	512 bytes
Maximum Operating Speed	230.4 kbps

4.3.2.2. UART2

UART2 is used for software download and provisioning.

[UART2 Pins](#) defines the UART2 pins available at the system connector. The characteristics such as buffer size, reference voltage and maximum baud-rate supported are listed in [UART2 Specifications](#).

Table 22: UART2 Pins

Pin Number	Signal Name	Voltage	I/O*	Description
30	RXD2	VCC_1V8	O	Auxiliary RS232 Receive
31	TXD2	VCC_1V8	I	Auxiliary RS232 Transmit
32	CTS2	VCC_1V8	O	Auxiliary RS232 Clear To Send
33	RTS2	VCC_1V8	I	Auxiliary RS232 Request To Send

Table 23: UART2 Specifications

UART2 Aspect	Value
Voltage	1.8 Vdc
Size of TX and RX FIFO Buffers	64 byte
Maximum Operating Speed	115.2 kbps

4.3.3. General Purpose Inputs/Outputs (GPIO)

There are 20 GPIO pins available on the system connector of the AirPrime Q26Elite.

Table 24: GPIO Pins

Pin Number	Signal Name	Voltage	Drive Strength (mA)	Pull State	Default Direction
12	GPIO2	VCC_1V8	2	Pull-Down	Input
22	GPIO32	VCC_2V6	2	Pull-Down	Input
23	GPIO33	VCC_2V6	2	Pull-Down	Input
24	GPIO34	VCC_2V6	2	Pull-Down	Input
25	GPIO35	VCC_2V6	2	Pull-Down	Input
26	GPIO36	VCC_2V6	2	Pull-Down	Input
27	GPIO37	VCC_2V6	2	Pull-Down	Input
28	GPIO38	VCC_2V6	2	Pull-Down	Input
29	GPIO39	VCC_2V6	2	Pull-Down	Input
43	GPIO40	VCC_2V6	2	Pull-Down	Input
45	GPIO41	VCC_2V6	2	Pull-Down	Input
47	GPIO42	VCC_2V6	2	Pull-Down	Input
48	GPIO43	VCC_2V6	2	Pull-Down	Input
49	GPIO44	VCC_2V6	2	Pull-Down	Input
50	GPIO7	VCC_1V8	2	Pull-Down	Input
51	GPIO51	VCC_1V8	6	No Pull	Input
53	GPIO50	VCC_1V8	2	Pull-Down	Input

Pin Number	Signal Name	Voltage	Drive Strength (mA)	Pull State	Default Direction
55	GPIO45	VCC_2V6	2	Pull-Down	Input
57	GPIO46	VCC_2V6	2	Pull-Down	Input
58	GPIO49	VCC_2V6	2	Pull-Up	Input

4.3.4. PCM Audio Interface

The AirPrime Q26Elite provides a PCM audio interface. This interface consists of four signals: PCM_CLK, PCM_SYNC, PCM_DOUT and PCM_DIN. The AirPrime Q26Elite PCM interface is configured as a master and therefore drives PCM_CLK and PCM_SYNC to an external codec device.

Table 25: PCM Audio Interface Pins

Pin Number	Signal Name	Voltage	I/O	Description
77	PCM_SYNC	VCC_1V8	O	PCM Frame Synchronize
78	PCM_DIN	VCC_1V8	I	PCM Data Input
79	PCM_CLK	VCC_1V8	O	PCM Clock
80	PCM_DOUT	VCC_1V8	O	PCM Data Output

4.3.4.1. PCM Data format

The PCM data is 8 kHz and 16 bits with the following PDM bit format:

- PCM_DIN – SDDD DDDD DDDD DDVV
- PCM_DOUT – SDDD DDDD DDDD DDVV

Where:

- S – Signed bit
- D – Data
- V – Volume padding

4.3.4.2. PCM Timing

The AirPrime Q26Elite PCM interface runs at 2.048 MHz with an 8 kHz short sync. The following figures and table illustrate the timing and parameters of the PCM interface.

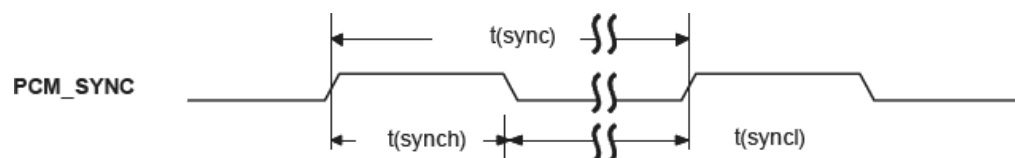


Figure 5. PCM Timing - AirPrime Q26Elite Sync Output

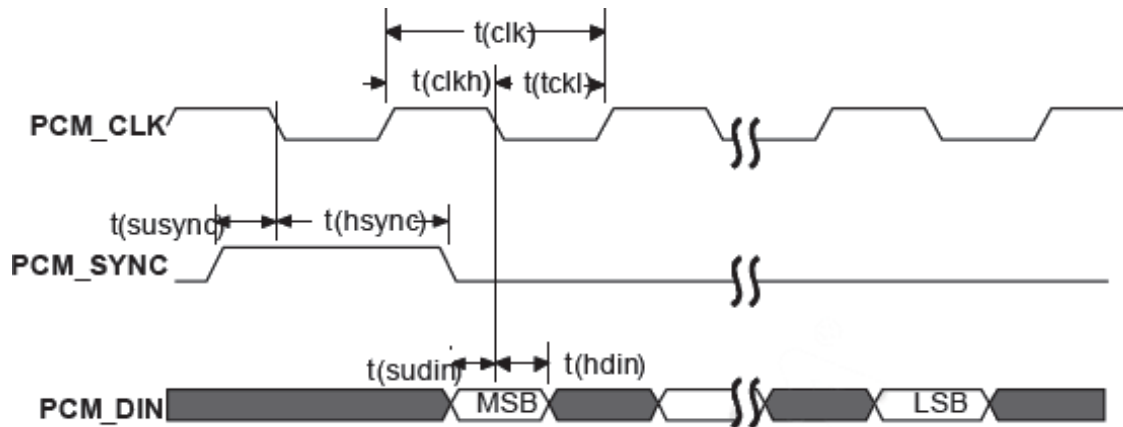


Figure 6. PCM Timing - Ext Codec to AirPrime Q26Elite

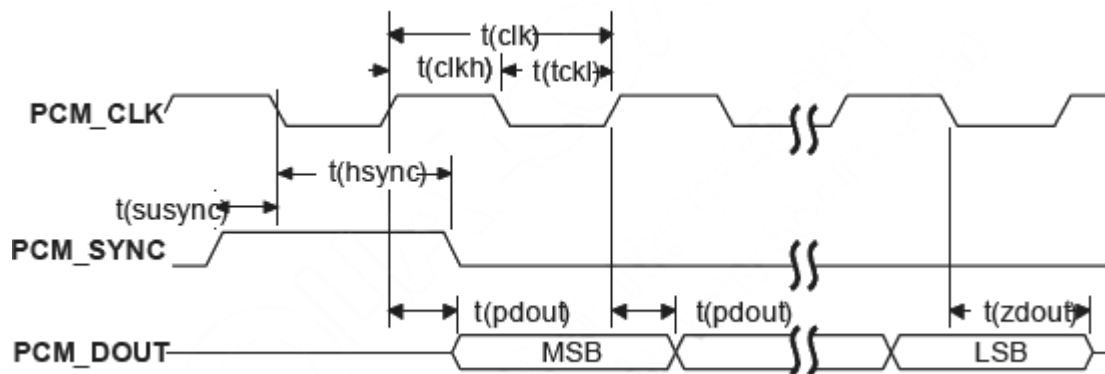


Figure 7. PCM Timing - AirPrime Q26Elite to External Codec

Table 26: PCM Timing Parameters

Parameter	Min	Typ	Max	Units
T(sync)		125		µs
T(synch)	400	500		ns
T(sync)		124.5		µs
T(clk)		488		ns
T(clkh)		244		ns
T(tckl)		244		ns
T(susync)	60			ns
T(hsync)	60			ns
T(sudin)	50			ns
T(hdin)	10			ns
T(pdout)			350	ns
T(zdout)		160		ns

4.3.5. I2C Interface

The AirPrime Q26Elite provides an I2C interface. This interface consists of a clock and data signal. These signals are open drain outputs and are pulled-up to VCC_2V6 through 2.2K resistors in the AirPrime Q26Elite.

Table 27: I2C Interface Pins

Pin Number	Signal Name	Voltage	I/O	Description
44	SCL	VCC_2V6	O	I2C Clock Output
46	SDA	VCC_2V6	I/O	I2C Bidirectional Data

Note: If level shifting is needed, chose a device that is designed for I2C interfaces such as the NXP GTL2002.

4.3.6. Interface Circuit Recommendations

Using open-drain non-inverting buffers with pull-ups to the appropriate voltage reference is the recommended interface implementation. This will allow a host processor operating at a different voltage to communicate with the AirPrime Q26Elite using the appropriate voltage levels.

The figure below is a reference circuit for a digital input signal to the AirPrime Q26Elite.

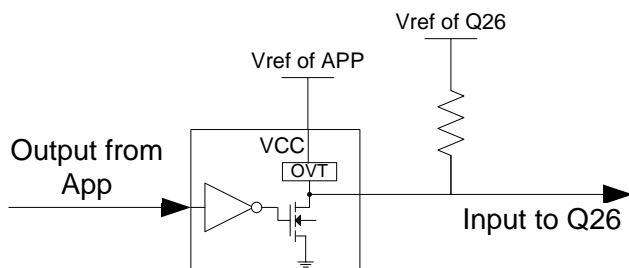


Figure 8. AirPrime Q26Elite Input Reference Circuit

The figure below is a reference circuit for a digital output signal from the AirPrime Q26Elite.

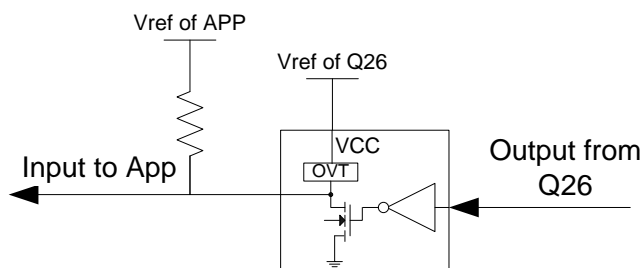


Figure 9. AirPrime Q26Elite Output Reference Circuit

Refer to the [Power and Ground](#) sections and subsections to identify the appropriate reference voltage and direction of the specific signals.

The open-drain non-inverting buffer used in the reference circuits above is the OnSemi NL17SZ07.

Tip: *The NL17SZ07 is over-voltage tolerant on the inputs. It may be possible to power all the buffers from the 1.8V reference voltage output. Review the Digital output characteristics of the applications drivers and the Input characteristics of the buffer selected to determine if this work in your application.*

If a Digital IO signal is used bidirectional in the application then a bidirectional buffer or bidirectional level translator will be needed.

4.4. Analog Interfaces

4.4.1. Analog to Digital Converter

The module includes a multi-input Analog to Digital Converter. Two external inputs, along with four internal inputs, are multiplexed into one converter within the module and can be queried with the appropriate AT Command. The specifications for the external inputs can be found in the following tables.

Table 28: DC Pins

Pin Number	Signal Name	Voltage	I/O*	Description
20	ADC_0	Analog	I	Analog to Digital Input
21	ADC_1	Analog	I	Analog to Digital Input

Table 29: ADC Analog Input Specification

Parameter	Conditions	Min.	Typ.	Max.	Units
Channel to channel isolation	f = 1KHz	50			dB
Resolution			8		bits
Input voltage range	ADC0	0		2.1	V
	ADC1	0		2.5	V
Input resistance	Parallel RC	3M			Ohm
	ADC0, ADC1		1.04M		
Input capacitance	Parallel RC	3		10	pF
Input Bandwidth	-3dB	1kHz			KHz
Full scale error				±3	%
Offset error				5	LSB
Sampling clock freq.	From internal RC oscillator		2.4		MHz
Conversion timing		5 ⁴		25.4 ⁵	µsec

ADC0 should be used for the battery thermistor if charging is implemented in the application.

4.4.2. Audio Interface

The AirPrime Q26Elite provides analog audio input and output on the System Connector. The System Connector provides for two microphones and two speakers to be connected, with either pair being selectable via AT Commands.

⁴With $T_{\text{sampling}}=3$ and 8bit resolution

⁵With $T_{\text{sampling}}=48$ and 12bit resolution

Table 30: Analog Audio Interface Pins

Pin Number	Signal Name	Voltage	I/O*	Description
34	MIC2N	Analog	I	Microphone 2 Input Negative
35	HPH_OUT_L_P	Analog	O	Speaker 1 Output Positive, 32 Ohm Output
36	MIC2P	Analog	I	Microphone 2 Input Positive
37	HPH_OUT_R_N	Analog	O	Speaker 1 Output Negative, 32 Ohm Output
38	LINE_IN_R_N	Analog	I	Microphone 1 Input Negative
39	SPKR_OUT_P	Analog	O	Speaker 2 Output Positive, 8 Ohm Output
40	LINE_IN_L_P	Analog	I	Microphone 1 Input Positive
41	SPKR_OUT_N	Analog	O	Speaker 2 Output Negative, 8 Ohm Output

Note: The microphone and speaker must be selected as a pair (LINE_IN with HPH_OUT; MIC2 with SPKR_OUT).

4.4.2.1. Microphone

The System Connector provides two microphone interfaces to the main board. Both the primary interface (LINE_IN) and secondary (MIC2) are mono differential interfaces. Either can of course be used in a single-ended application (such as for a headset) however the differential configuration is recommended to help reduce noise. The MIC2 interface is internally biased to 1.8V. The LINE_IN interface requires external bias if used with a microphone element.

Table 31: Input audio settings

Parameter	Test Conditions	Min	Typ	Max	Unit	
Transmit reference-signal level (0dBm0)	Differential analog input	0dB	0.89	1.00	1.12	Vrms
		24dB	56.2	61.3	70.8	mVrms

Figure 10 is an example of a differential microphone in a typical handset application using the LINE_IN interface pins.

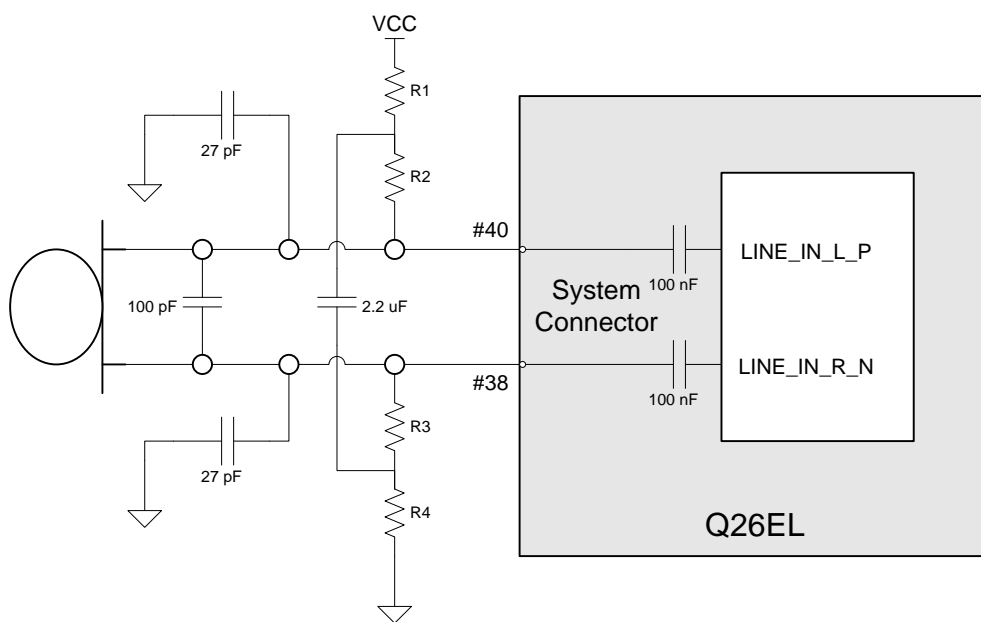


Figure 10. LINE_IN Differential Interface

The bias level (VCC) and the resistance values of R1, R2, R3 and R4 are dependent on the microphone element chosen for the application. For a typical handset application the value of VCC = 1.8 – 2.5 V; R1 = R4 = 1.2 kΩ and R2 = R3 = 1 kΩ. The source for the bias is recommended to be a regulated supply.

Figure 11 is an example of a differential microphone in a typical handset application using the MIC2 interface pins.

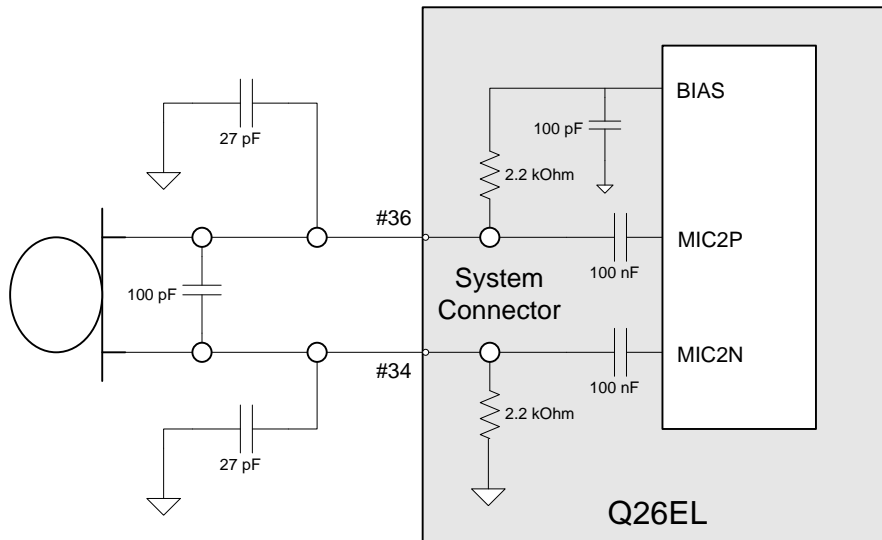


Figure 11. MIC2 Differential Interface

Figure 12 is an example of a single-ended microphone in a typical handset application using the LINE_IN interface pins.

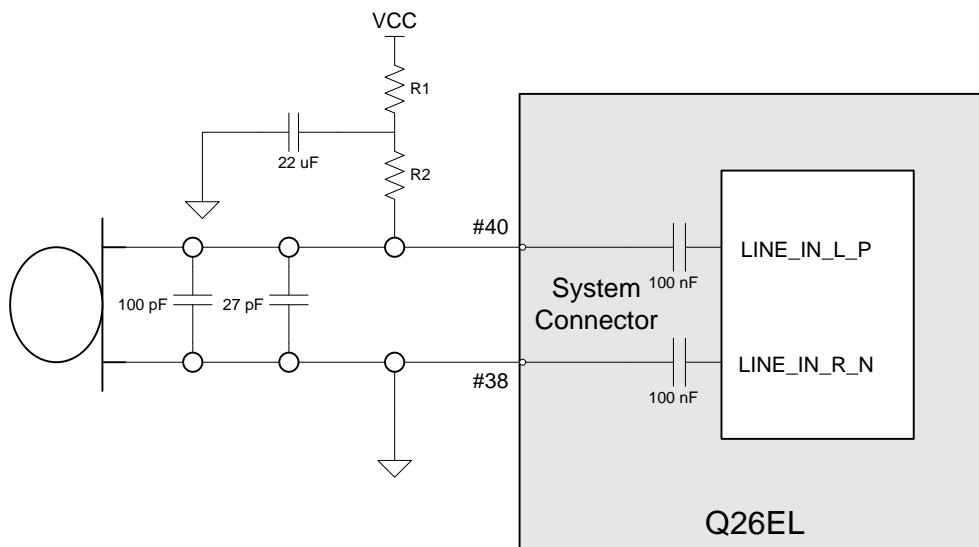


Figure 12. LINE_IN Single-Ended Interface

The bias level (VCC) and the resistance values of R1 and R2 are dependent on the microphone element chosen for the application. For a typical handset application the value of VCC = 1.8 – 2.5 V; R1 = 1.2 kΩ and R2 = 1 kΩ. The source for the bias is recommended to be a regulated supply.

Figure 13 is an example of a single-ended microphone in a typical handset application using the MIC2 interface pins.

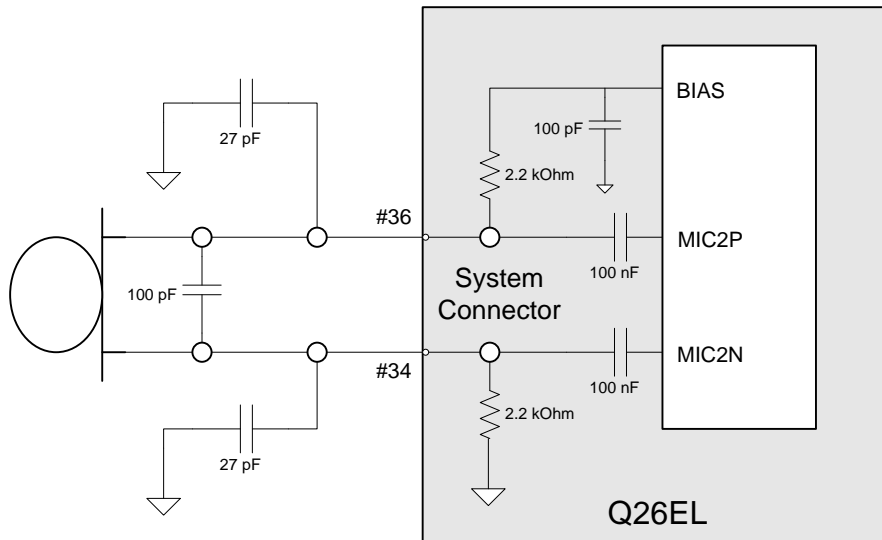


Figure 13. MIC2 Single-Ended Interface

4.4.2.2. Speaker

The System Connector provides two speaker interfaces to the main board. Both the primary (HPH_OUT) and secondary (SPKR_OUT) interfaces are mono differential. Either can of course be used in a single-ended application (such as for a headset) however the differential configuration is recommended to help reduce noise.

Table 32: Speaker Differential Recommendations

Parameter	Test Conditions	Min	Typ	Max	Unit	
HPH_OUT Full Scale	Differential Output	32 Ω Load	1.048	1.176	1.319	Vrms
SPKR_OUT Full Scale	Differential Output	8 Ω Load	2.0			Vrms

Figure 14 and Figure 15 are examples of a differential speaker in a typical handset application.

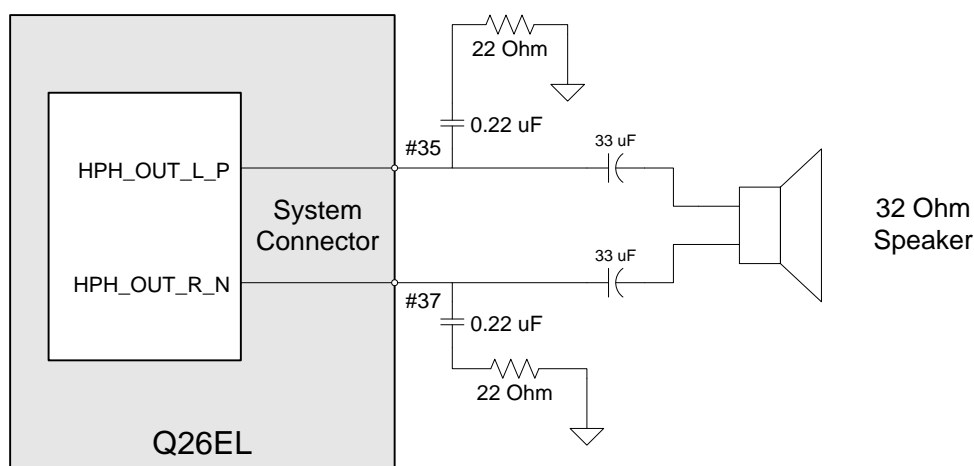


Figure 14. HPH_OUT Differential Interface

Note: The 33uF in series on both HPH_OUT_L_P and HPH_OUT_R_N in Figure 14 can be omitted if desired.

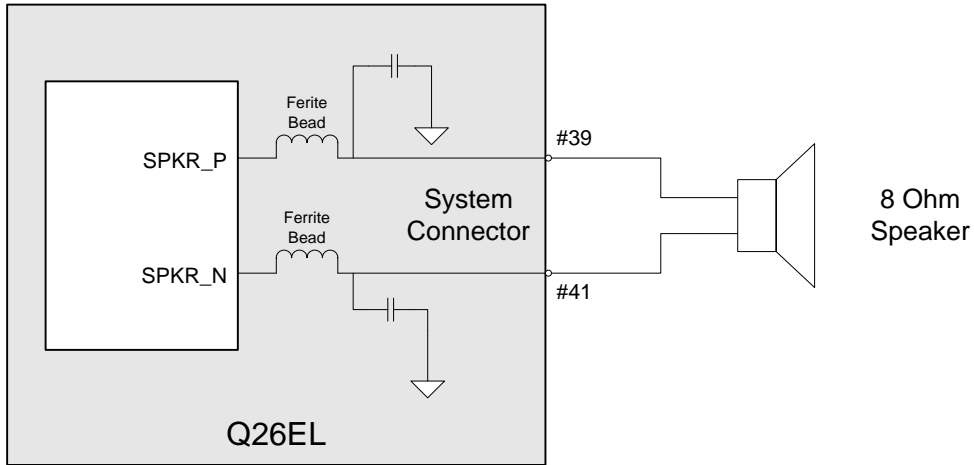


Figure 15. SPKR Differential Interface

Figure 16 and Figure 17 are examples of a single-ended speaker in a typical handset application.

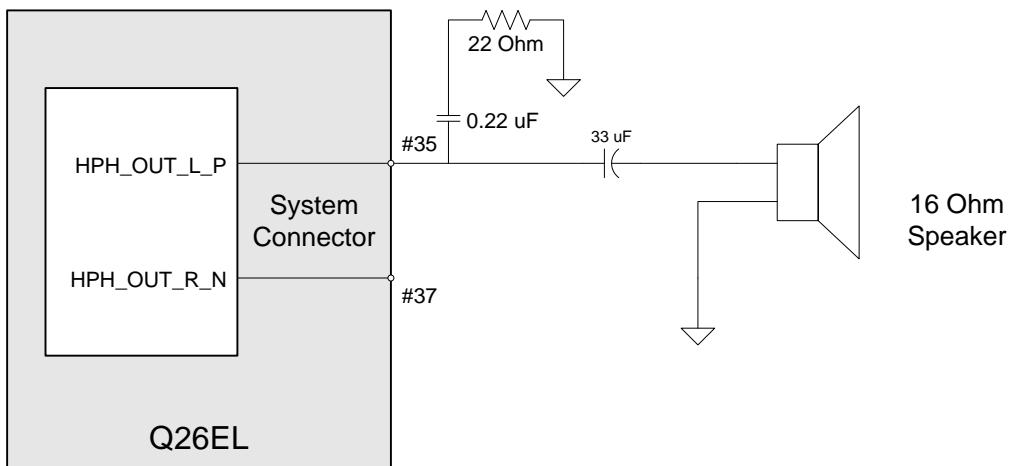


Figure 16. HPH_OUT Single-Ended Interface

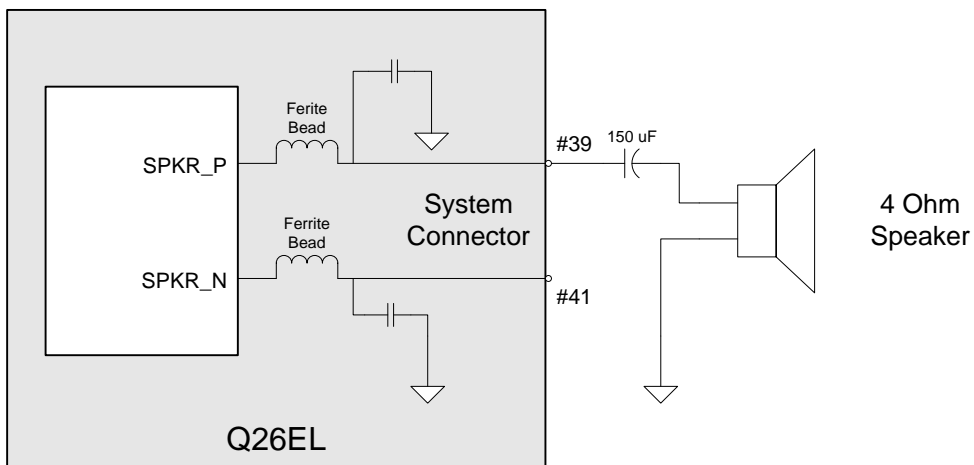


Figure 17. SPKR Single-Ended Interface

4.5. Vibration Motor Driver

A Vibration Motor Driver is provided to support silent incoming call alarms.

Pin number	Signal	Voltage	I/O	Description
15	VIB_DRV_N	VBATT	O	Vibration Motor Driver

The vibration driver is a programmable voltage output that is referenced to VBATT; when off, its output voltage is VBATT. The motor is connected between VBATT and the VIB_DRV_N pin.

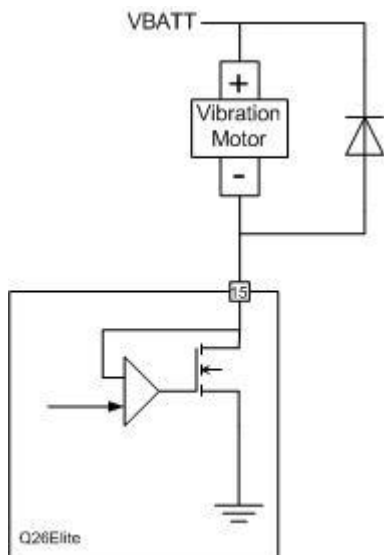


Figure 18. Vibration motor driver circuit diagram

Performance specifications for the vibration motor driver circuit are listed in the table below:

Table 33: Vibration motor driver circuit specifications

Parameter	Comments	Min	Typ	Max	Units
Output voltage (V_m) error	$VBATT > 3.2\text{ V}$; $I_m = 0\text{ to }175\text{ mA}$; V_m setting = 1.2 to 3.1 V		-		
• Gain error		-6		+6	%
• Offset error		-60		+60	mV
Short circuit current	$VIB_DRV_N = VBATT$	225	-	500	mA
Driver bias current	$I_m = 175\text{ mA}$	-	78	-	uA
Driver leakage current		-	-	100	nA

4.6. USB 2.0 interface

A 4-wire USB slave interface is available that is USB 2.0 specification-compliant. The AirPrime Q26Elite is a self powered peripheral device that operates at USB full speed.

The USB circuits are powered by the USB_VBUS node and therefore may draw up to one unit load (100 mA) from this supply, VPAD-USB.

The USB interface signals are VPAD-USB, USB-DP, USB-DM and GND.

Table 34: USB interface Pins

Pin number	Signal	Voltage	I/O	Description
52	VPAD-USB	VPAD_USB	I	USB Power Supply
54	USB-DP	VPAD_USB	I/O	Differential data interface positive

Pin number	Signal	Voltage	I/O	Description
56	USB-DM	VPAD_USB	I/O	Differential data interface negative

4.7. R-UIM Interface

A version of the Q26Elite supporting R-UIM is available for markets that require it. This version does not have a second UART.

Table 35: R-UIM interface Pins

Pin number	Signal	Voltage	I/O	Description
9	UIM_PWR	1V8 or 3V	O	UIM Power Supply
11	UIM_DATA	1V8 or 3V	I/O	UIM Data
13	UIM_RESET	1V8 or 3V	O	UIM reset Output
14	UIM_CLK	1V8 or 3V	O	UIM Clock

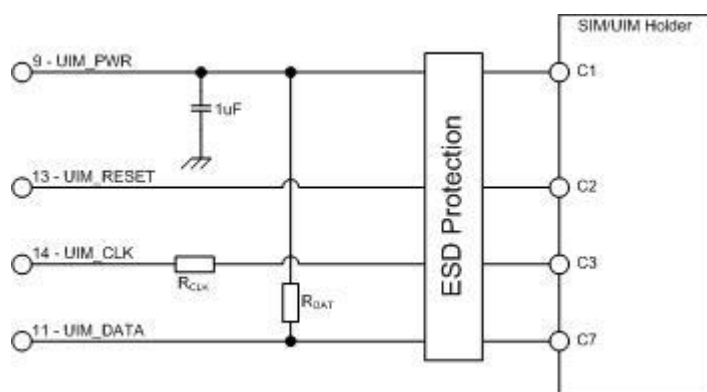


Figure 19. R-UIM Interface Reference Drawing

The above drawing illustrates the recommended connections for R-UIM card support.

The capacitor and two resistors should be added as placeholders to compensate for potential layout issues. Route the UIM_DATA signal away from the UIM_CLK signal. Keep distance from Q26Elite to SIM-Holder as short as possible.

Note: All signals must be ESD-protected.

4.8. Hardware Features

4.8.1. RTC

The AirPrime Q26Elite has an internal Real-Time Clock function. This block is powered from the VBATT supply. If the VBATT supply is removed, a coin cell connected to the VCOIN pin will continue to power this function.

4.8.2. SMPL

The AirPrime Q26Elite supports a Sudden Momentary Power Loss feature. This feature initiates a power-on sequence without software intervention if the monitored phone voltage (VBATT) drops out-of-range then returns in-range within a defined interval. SMPL achieves immediate and automatic recovery from momentary power loss.

Table 36: SMPL Characteristics

Parameter	Value	Unit
SMPL threshold	2.55	V
SMPL drop-out interval	2.0	s

In order to use the SMPL feature a coin cell or capacitor must be connected to the VCOIN pin. Otherwise, the AirPrime Q26Elite will remain shutdown and remain in the off state due to the momentary power disruption.

4.8.3. UVLO

The AirPrime Q26Elite has an Under Voltage Lockout feature. The UVLO feature is a hardware feature that continually monitors the input supply (VBATT) and automatically turns off the device at severely low input conditions. An ON/OFF pulse is required to power the unit up once VBATT is in the valid supply range.

Table 37: UVLO Characteristics

UVLO	Min	Nom	Max	Unit
Falling threshold	2.423	2.55	2.678	V
Hysteresis	120	165	210	mV
UVLO detection interval		1		us

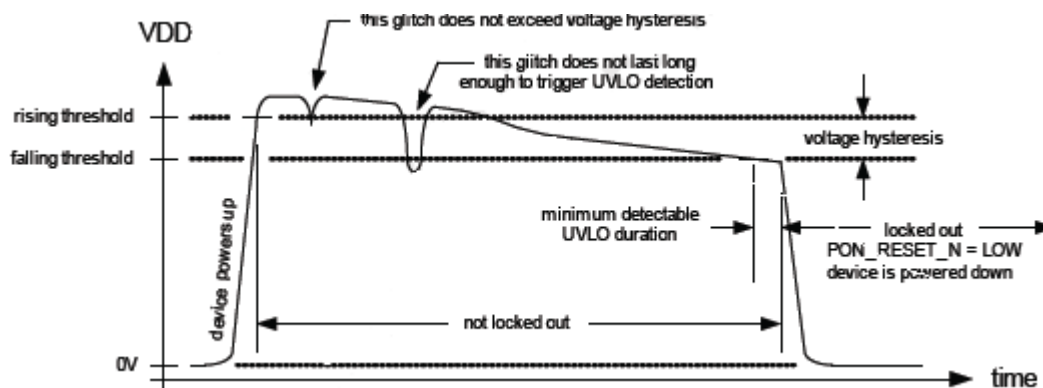


Figure 20. UVLO feature

4.9. RF Interfaces

The AirPrime Q26Elite operates in Band Class 0 and 1 for CDMA 1xRTT operation. The table below defines the performance characteristics of the radio.

Table 38: RF Parametrics

	BC0 (Power Class III)	BC1 (Power Class II)	Units
Max TX RF Output Power	+24 (+2/-1)	+24 (+2/-1)	dBm
Minimum RX Sensitivity	-104	-104	dBm

Note: The values in the table above are valid at the RF connectors of the AirPrime Q26Elite into a 50 Ohm load.

The AirPrime Q26Elite module has two antenna connections; CDMA and GPS. These paths are separate internally and must be provided via their respective antenna ports.

4.9.1. CDMA Antenna Specifications

A dual-band, tri-band or quad-band antenna may be used, depending on customer applications. The antenna must have the following characteristics:

Table 39: CDMA Antenna Characteristics

Characteristics		US Cellular (BC0)	US PCS (BC1)
Frequency (MHz)	TX	824-849	1850-1910
	RX	869-894	1930-1990
Impedance	RF	50 Ohm	
	DC ⁶	10 kOhm	
VSWR max	RX	1.5: 1	
	TX	1.5: 1	
Polarization		Linear, vertical	
Typical radiated gain		0 dBi in one direction at least	

Note: Sierra Wireless recommends a VSWR max of 1.5:1 for the Rx and Tx bands. Nevertheless, all aspects of this specification will be fulfilled even with a max. VSWR of 2:1.

4.9.2. GPS Antenna Specification

The AirPrime Q26Elite module is designed to provide a 5V bias to power an active GPS antenna. For applications in which an active antenna is used, a diagnostic function to detect OPEN, SHORT or OK status is available.

Table 40: GPS Antenna Characteristics

Characteristics		GPS L1
Frequency (MHz)	RX	1575.42
Impedance	RF	50 Ohm
VSWR max	RX	1.5: 1

⁶ For antenna diagnostic feature

Characteristics	GPS L1
LNA Bias Voltage	5V
LNA Current Consumption	40 mA Max
Polarization	Right Hand Circular Polarization
Typical radiated gain	0 dBi in one direction at least

4.9.3. Antenna Implementation

The CDMA and GPS antennas must be placed such that there is at least 10 dB of isolation between them to ensure that the CDMA transmitter does not desensitize the GPS receiver.

The antennas should be isolated to the greatest extent possible from analog & digital circuitry (including interface signals).

On applications with an embedded antenna, poor shielding could dramatically affect the receiving sensitivity. Moreover, the power radiated by the antenna could affect the application.

As a general recommendation, all components or chips operated at high frequencies (microprocessors, memories, DC/DC converter), or other active RF parts shall not be placed too close to the module. In such a case, correct power supply layout and shielding shall be designed and validated. Components near RF connections or unshielded feed lines are prohibited.

RF lines must be kept as short as possible and impedance controlled to minimize losses.

>> 5. Mechanical

The AirPrime Q26Elite module is a member of the AirPrime Q26 Series of Intelligent Embedded Modules. It therefore has common length and width dimensions as the other AirPrime Q26 Series modules. The system connector physical attributes are identical as well as its placement. The primary RF connector and placement are also consistent with the rest of the family.

Three drawings are provided to aid in integrating the AirPrime Q26Elite into the application:

- Mechanical Drawing – identifies the mechanical dimensions of the AirPrime Q26Elite
- Customer PCB Drawing – defines the footprint need on the application to mount the AirPrime Q26Elite. This drawing includes the drill template for the four pads to be soldered on the application board
- Component Location Drawing – Dimensions the connectors and mounting features of the AirPrime Q26Elite.

It is strongly recommended that the area immediately around the module be kept free of component placements in order to facilitate removal/reassembly of the module on the application board.

5.1. Thermal Behavior

Be aware that, when transmitting, the AirPrime Q26Elite will heat up (largely due to the internal Power Amplifier). This heating will generate a temperature increase that may warm the application board on which the AirPrime Q26Elite is soldered.

5.2. Heat sink

For applications operating above +75°C a heat sink is recommended. A 6 x 8mm contact pad is available on the bottom side of the AirPrime Q26Elite directly below the Power Amplifier.

The application board should be designed such that the top layer is solid copper below the AirPrime Q26Elite when it is mounted. This would allow a similar 6 x 8mm contact pad to be defined directly below the one on the AirPrime Q26Elite. Thermal gap filler could then be used to provide heat sinking. See the [Thermal Gap Filler](#) section for a suggested supplier.

Table 41: Heat sink thermal efficiency

Heat sink Characteristics	
Thermal efficiency	5°C/W

5.4. Customer PCB Drawing

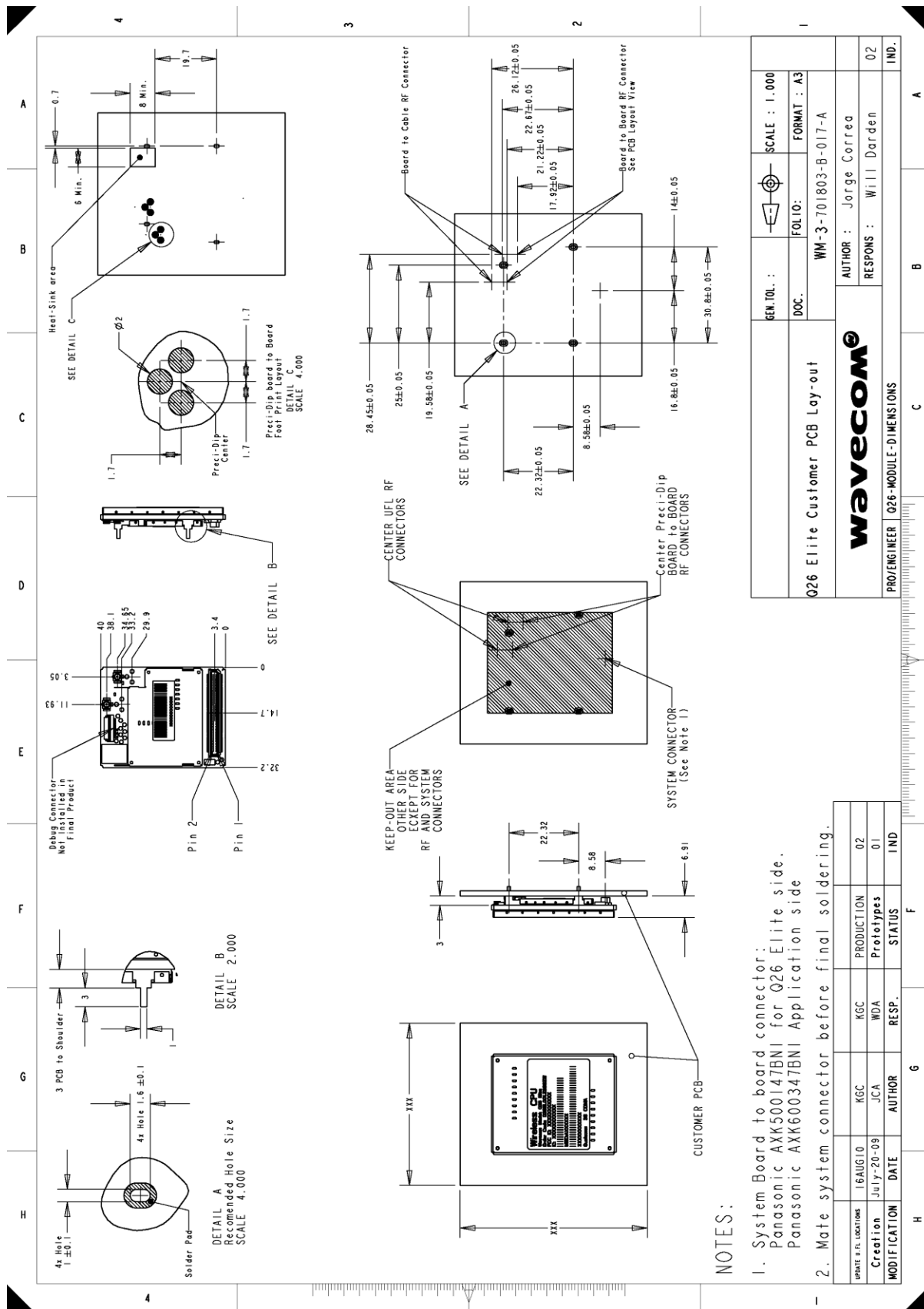


Figure 22. Customer PCB Drawing

5.5. Component Location Drawing

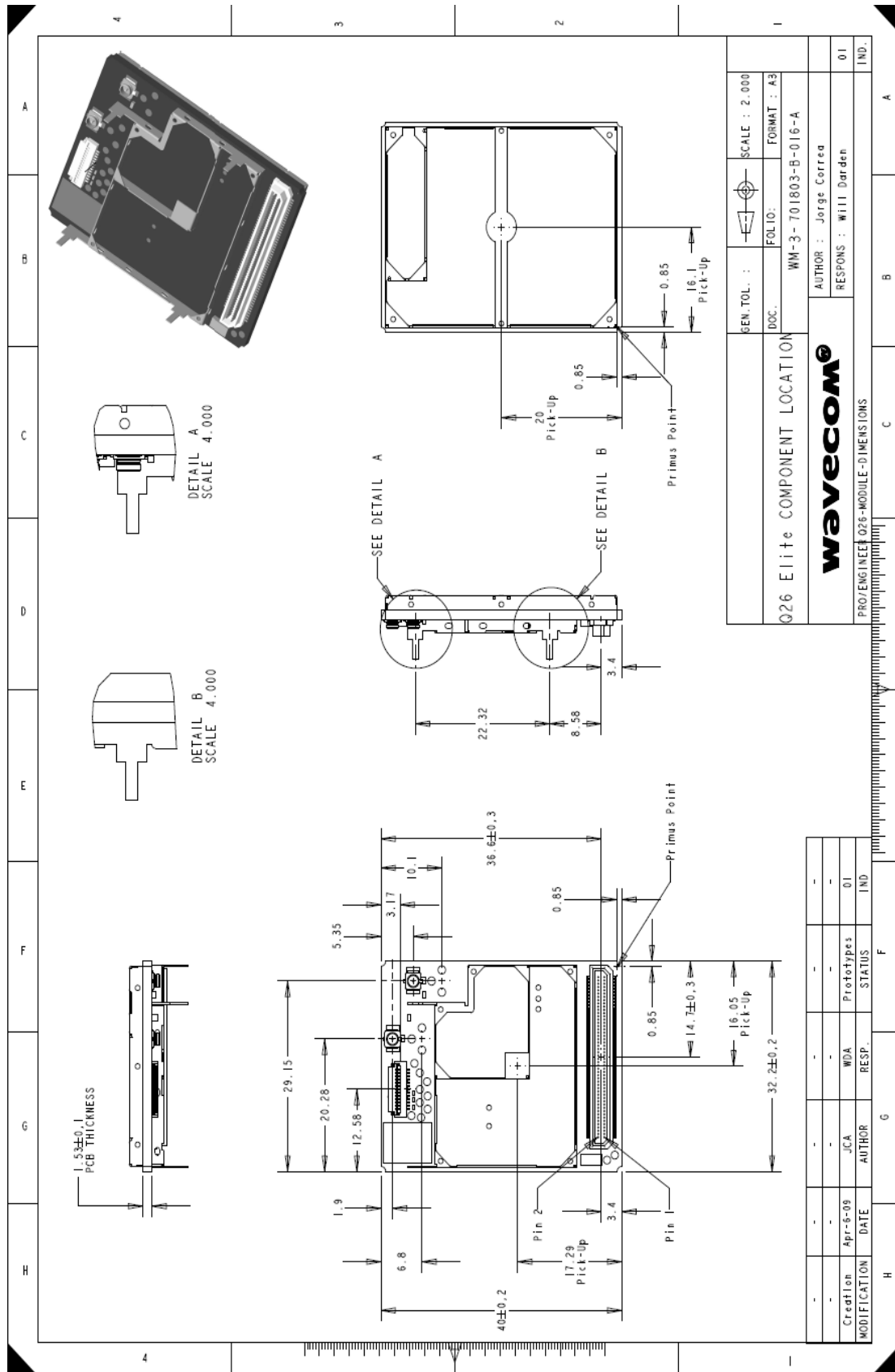


Figure 23. Component Location Drawing

6. PCB Design

6.1. General Rules and Constraints

On the application board, it is strongly recommended to avoid routing any signals under the module. Clock and other high frequency digital signals (e.g. serial buses) should be routed as far as possible from the module analog signals.

If the application design allows, all analog signals should be separated from digital signals by a ground line on the PCB.

6.2. Specific Routing Constraints

6.2.1. System Connector

- Refer to the reference of the 100-pin receptacle (from Panasonic Electric Works) given in paragraph 9, "Manufacturers and suppliers".
- More detailed information is also available at the following internet address: <http://panasonic-denko.co.jp/ac/e/>.

6.2.1.1. Application Ground Plane and Shielding connection

The AirPrime Q26Elite module shielding case is linked to the ground. The ground must be connected to the mother board through a complete layer on the PCB.

A ground plane must be available on the application board to provide efficient connection to the module shielding:

- The bottom side shielding of the module is achieved through the top folded tin cover connected to the internal ground plane of the module. The module ground plane is connected through the shielding to the application ground plane.

Best shielding performance will be achieved if the application ground plane is a complete layer of the application PCB:

- To ensure good shielding of the module, a complete ground plane layer on the application board must be available with no trade-off. Connections between other ground planes shall be made with vias.

Without this ground plane, external Tx spurious or Rx De-sense could appear.

6.2.2. Audio circuit routing constraints

To get better acoustic performance, the basic recommendations are as follows:

- The speaker lines must be routed as a differential pair without any signals between them.
- The microphone lines must be routed as a differential pair without any signals between them.

All the filtering components (RLC) must be placed as close as possible to the associated analog audio input and output pins.

6.2.3. RF circuit routing constraints

6.2.3.1. General recommendations

If RF signals need to be routed on the application board, the following recommendations must be observed for PCB layout:

The RF signals must be routed using tracks with a $50\ \Omega$ characteristic impedance.

Basically, the characteristic impedance depends on the dielectric, track width and ground plane spacing.

In order to respect this constraint, Sierra Wireless recommends that a MicroStrip or StripLine structure be used and track width be computed with a simulation tool (such as AppCad, shown in the figure below and available free of charge at <http://www.avagotech.com>).

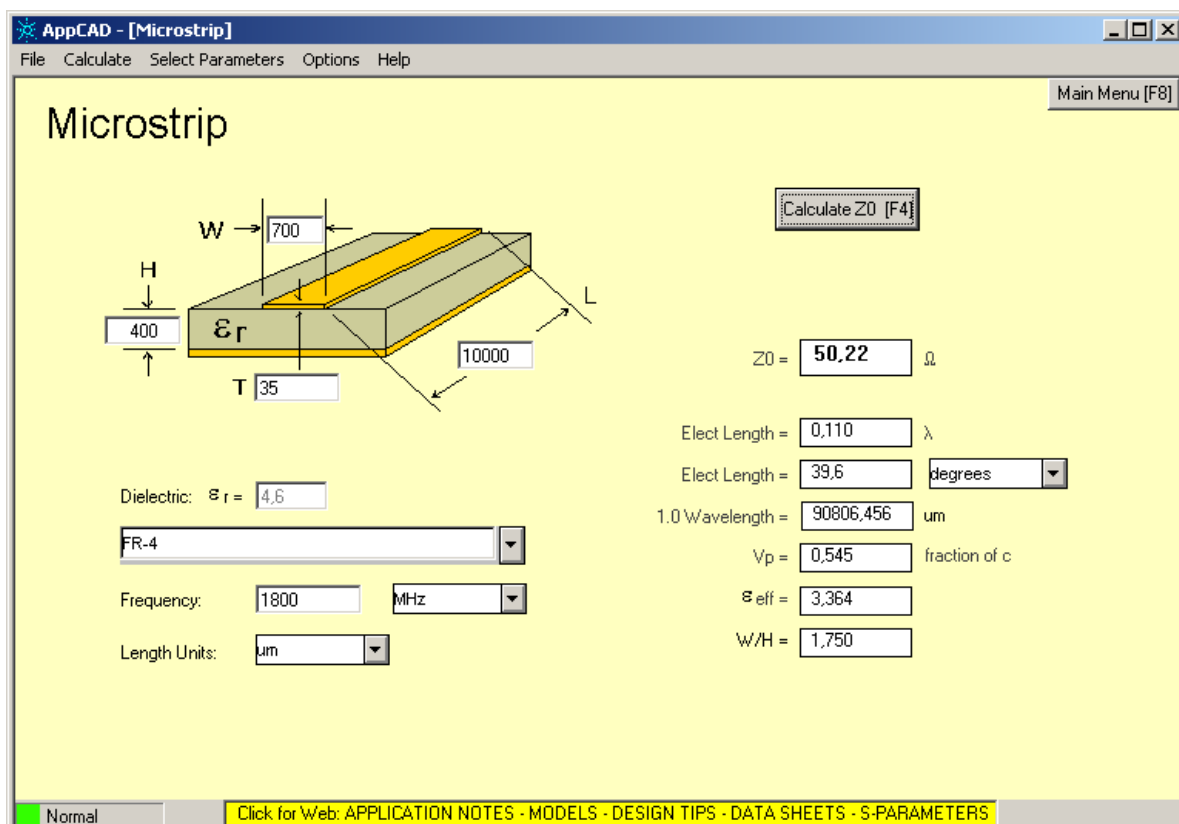


Figure 24. AppCad Screenshot for MicroStrip design

If a multi-layer PCB is used, the RF path on the board must not cross any signals (digital, analog or supply).

If necessary, use a StripLine structure and route the digital line(s) “outside” the RF structure, as shown in the figure below.

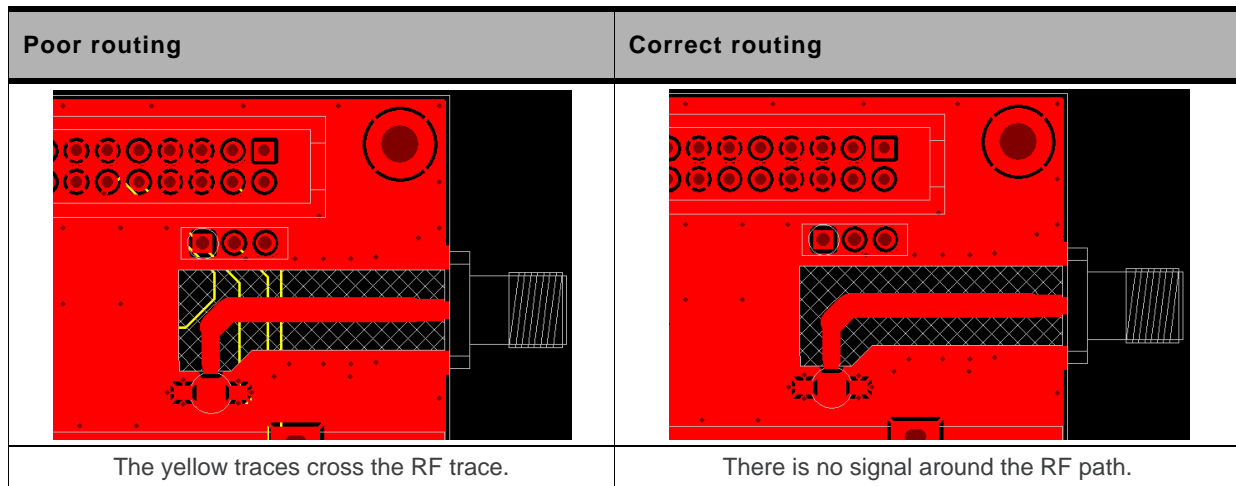


Figure 25. Routing examples

- Stripline and Coplanar designs require a correct ground plane on both sides. Consequently, some vias must be added along the RF path.
- It is recommended to use a Stripline design if the RF path is fairly long (more than 3 cm), since the MicroStrip design is not shielded. Consequently, the RF signal (when transmitting) may interfere with the neighboring electronics (AF amplifier...). In similar manner, the neighboring electronics (micro-controller) may degrade reception performance.

6.2.3.2. Connection possibilities

If the CDMA and/or GPS RF connections need to be implemented on the application board (for mechanical purposes for instance), there are two connection possibilities:

- via UFL/SMA cable
- via Preci-dip connector

6.2.3.2.1. UFL/SMA connector

The antenna can be connected to the module via the UFL connector present on the Wavecom module.

- Insert the plug in the receptacle

This step is performed prior to module mounting.

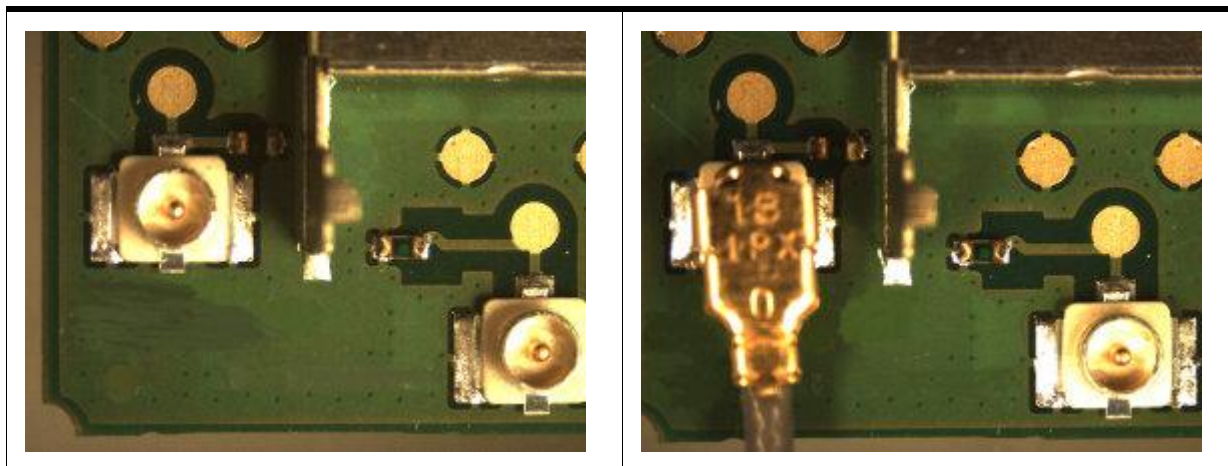


Figure 26. UFL Connectors

6.2.3.3. Via Preci-dip connector

The antenna can be connected to the module through a Preci-dip compression connector that must be assembled on the customer board.

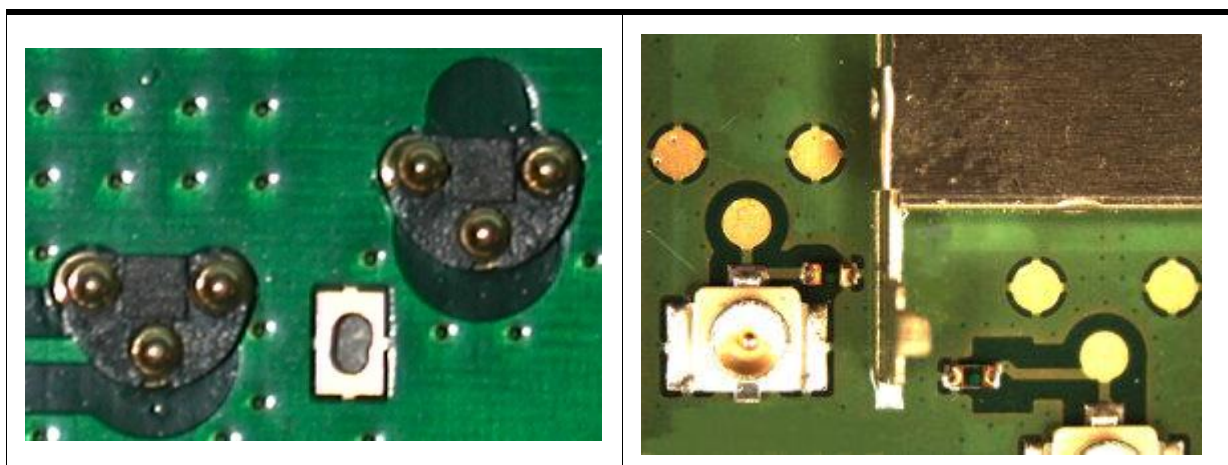


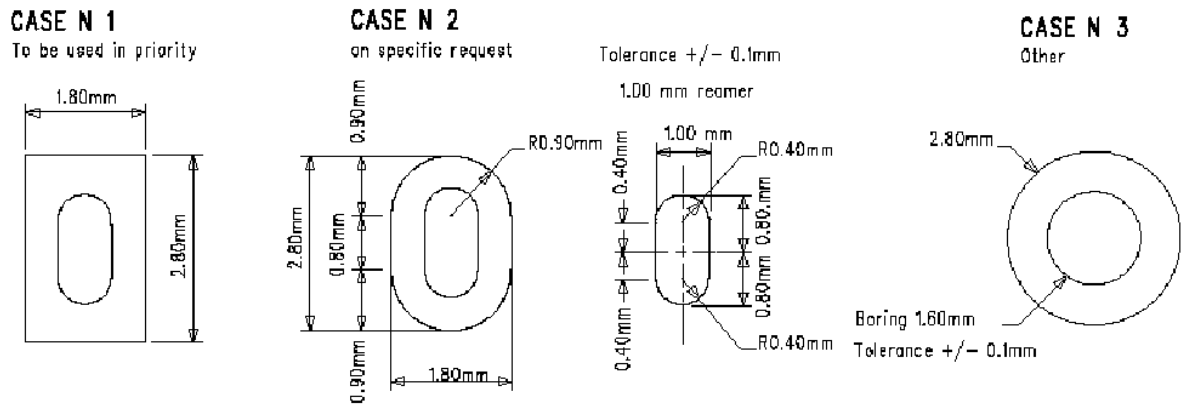
Figure 27. Preci-dip Connectors

For information on the mounting, assembly and handling of this component, please contact the supplier, Preci-dip, directly. Sierra Wireless cannot provide customer support for use of this connector.

6.2.3.4. RF circuit for CDMA function

The CDMA connector is intended to be directly connected to the 50Ω antenna. No matching need.

6.3. Pad Design



THERMAL BRAKES DEFINITION

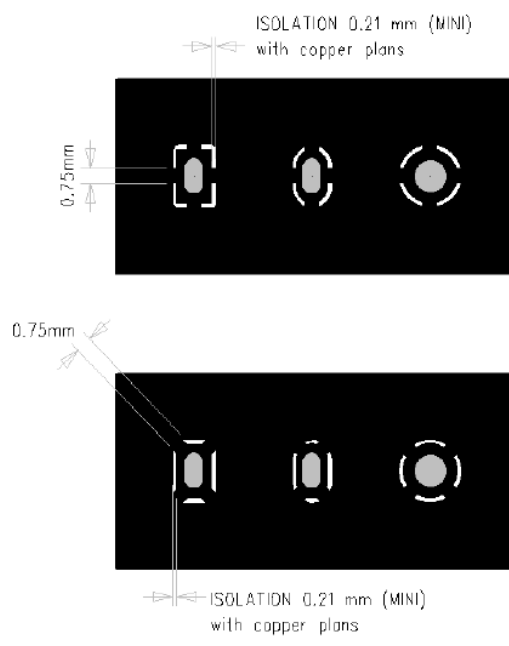


Figure 28. Ground Pad design recommendations

It is strongly recommended to use through-hole pads for the 4 leads of the AirPrime Q26Elite. If the holes are internally connected to the ground plane, please use thermal brakes.

7. FCC Compliance

The AirPrime Q26Elite is FCC certified as a 'mobile device', which requires a minimum distance of 20 cm between the application's antenna and the human body.

Per FCC Section 15.21, any changes or modifications to the AirPrime Q26Elite not expressly approved by Sierra Wireless could void the user's authority to operate the equipment.

Users and installers must be provided with antenna installation instructions and transmitter operating conditions for satisfying RF exposure compliance.

The Sierra Wireless FCC ID may be used by the integrator if the following conditions are followed:

1. The application must be implemented as a "mobile device" and not a "portable device."
2. The application's user and installation manuals must include a statement that a minimum distance of 20 cm between the antenna and the human body is required.
3. The antenna system gain must be within the following constraints:
 - a. 850 MHz Band: the antenna system gain must not exceed 5.76 dBd gain.
 - b. 1900 MHz PCS Band: the antenna system gain must not exceed 7.01 dBi gain.
4. The license module will have a FCC ID label on the module itself. The FCC ID label must be visible as defined by the FCC (visible through an open access door is permissible), or a separate label must be similarly visible that conveys the message: "Contains Transceiver Module FCC ID: O9EQ26ELITE."



8. EMC and ESD Recommendations

The EMC tests must be performed on the application as early as possible to detect any potential problems.

When designing, special attention should be paid to:

- Possible spurious emission radiated by the application to the RF receiver in the receiver band
- ESD protection is mandatory on all signals which have external accessibility (typically human accessibility).
 - Typically, ESD protection is mandatory for the:
 - RUIM (if accessible from outside)
 - Serial link, etc.
- Length of the RUIM interface lines (preferably <10cm)
- EMC protection on audio inputs/outputs
- Ground plane: Sierra Wireless recommends a common ground plane for analog / digital / RF grounds
- A metallic case or plastic casing with conductive paint is recommended

Note: The module does not include any protection against over voltage.



9. Serial Communications

The AirPrime Q26Elite module has two UARTs and a USB interface.

- UART1 is used for AT commands and Unsolicited messages to and from the AirPrime Q26Elite.
- UART2 is used with WPST to perform firmware download and provisioning of the AirPrime Q26Elite.
- USB is used to support diagnostic logging.

9.1. Software Download and Provisioning

WPST is a software application that runs on a PC and allows software download and provisioning of a AirPrime Q26Elite.

In order to connect the UART2 signals of the AirPrime Q26Elite to a PC an RS-232 Transceiver is required. Refer to the [UART2](#) section for pin assignments and characteristics of UART2. The implementation below uses a Linear Technology LTC2804 RS-232 Transceiver.

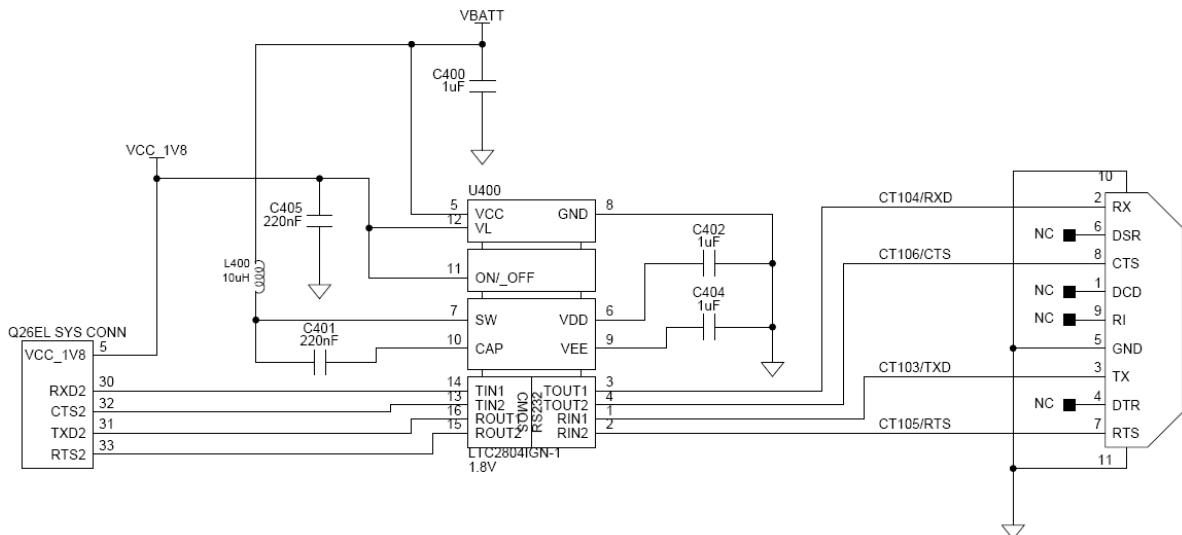


Figure 30. UART2 serial port access

For applications that do not want to implement the ability to download/provision the AirPrime Q26Elite while it is in the application, this circuitry is not required.

9.2. Diagnostic Logging

It is possible to perform diagnostic logging of the AirPrime Q26Elite. This function is only supported over the USB interface and requires Qualcomm QxDM to be installed on a host PC. This tool cannot be provided by Sierra Wireless. If desired, the customer is required to procure this tool directly from Qualcomm.



10. Manufacturers and Suppliers

This section contains a list of recommended manufacturers and suppliers of the peripheral devices that may be used with the AirPrime Q26Elite module.

10.1. System Connector

The system connector is a 100-pin connector with 0.5mm pitch from the Panasonic Electric Works Co., Ltd. group P5K series with the following reference:

AXK600347BN1

The mating connector reference is:

AXK500147BN1

The stacking height is 3.0 mm.

Sierra Wireless recommends that you use the **AXK500147BN1** connector for your application to benefit from Sierra Wireless prices. For more information, contact Sierra Wireless, specifying the Wavecom connector reference **WM17077**.

For further details see the GPC data sheets in the appendix. More information is also available from <http://panasonic-denko.co.jp/ac/e/>

10.2. RF Cable

A wide range of cables fitted with UF-L connectors is offered by HIROSE:

- UF-L pigtails
- UF-L cable assemblies
- Between series cable assemblies

More information is also available from <http://www.hirose-connectors.com/>.

10.3. RF Board to Board Connector

Preci-dip (<http://www.Preci-dip.com>) is the supplier of the RF compression contact connector. The part number is: 9PM-SS-0003-02-248

10.4. Thermal Gap Filler

Laird Technologies (<http://www.lairdtech.com/thermal/>) is a supplier of thermal gap filler that may be used with the AirPrime Q26Elite. The part number is: T-Flex 700 Series, 3.5mm thick

11. Frequently Asked Questions

This section is intended to provide answers to commonly asked questions.

Table 42: Frequently Asked Questions

Q:	In the event of a AirPrime Q26Elite failure (loss of communication, etc.), should we toggle the reset pin, or should we power off and power on the Q26?
A:	Power cycling the AirPrime Q26Elite via the ON/OFF signal should be the first step, if this does not resolve the issue then a reset may be generated using the RESET_N signal.
Q:	How many wire serial interfaces are supported by the AirPrime Q26Elite?
A:	UART1 is a full 8-wire interface (RXD1, TXD1, RTS1, CTS1, DTR1, DSR1, DCD1, and RI1). UART2 is a 4-wire interface (RXD2, TXD2, RTS2 and CTS2). UART1 can also be used as a 4-wire interface. Neither UART1 nor UART2 is recommended to be used as a 2-wire interface (RXD and TXD).
Q:	Is Hardware Flow control enabled by default?
A:	Yes, HW flow control is enabled by default, hence a 2-wire interface implementation is not recommended.
Q:	Can the UF-L and Preci-dip connectors be utilized simultaneously for CDMA?
A:	No, this will degrade the CDMA performance. Either may be used for CDMA radio interface.
Q:	Can the UF-L and Preci-dip connectors be utilized simultaneously for GPS?
A:	No, this will degrade the GPS performance. Either may be used for GPS radio interface.
Q:	What are the four posts on the bottom side shield fence?
A:	These posts are the ground connections for the AirPrime Q26Elite and must be soldered to the common ground of the power supply for the AirPrime Q26Elite and the application ground. All four posts should be soldered. See the Pad Design section for more details on how to provision for these in the application.



12. System Connector Pin-out

Table 43: System Connector Pin-out

Pin #	Signal Name	Voltage	I/O*	Pin Type	If Unused	Description
1	VBATT	VBATT	I	AI	Must be used	Power Supply
2	VBATT	VBATT	I	AI		Power Supply
3	VBATT	VBATT	I	AI		Power Supply
4	VBATT	VBATT	I	AI		Power Supply
5	VCC_1V8	VCC_1V8	O	AO	Leave Open	1.8V Supply Output
6	CHG-IN	CHG-IN	I	AI	Leave Open	Charger input
7	VCOIN	VCOIN	I/O	AI, AO	Leave Open	RTC Battery connection
8	CHG-IN	CHG-IN	I	AI	Leave Open	Charger input
9	UIM_PWR	1V8 or 3V	O	AO	Leave Open	UIM Power Supply
10	VCC_2V6	VCC_2V6	O	AO	Leave Open	2.6V Supply Output
11	UIM_DATA	1V8 or 3V	I/O	B6	Leave Open	UIM Data
12	GPIO2	VCC_1V8	I/O	BS-PD2	Leave Open	
13	UIM_RESET	1V8 or 3V	O	DO2	Leave Open	UIM reset Output
14	UIM_CLK	1V8 or 3V	O	DO2	Leave Open	UIM Clock
15	VIB_DRV_N	Open Drain	O		Leave Open	Buzzer Output
16	BOOT	VCC_1V8	I		Leave Open	Not Used
17	LED	Open Drain	O		Leave Open	Flash Led Output
18	RESET_N	VCC_1V8	I		Leave Open	RESET Input
19	ON/~OFF	VBATT	I		Must be used	ON / ~OFF Control
20	ADC_0	Analog	I	AI	Ground	Analog to Digital Input
21	ADC_1	Analog	I	AI	Ground	Analog to Digital Input
22	GPIO32	VCC_2V6	I/O	BS-PD2	Leave Open	
23	GPIO33	VCC_2V6	I/O	BS-PD2	Leave Open	
24	GPIO34	VCC_2V6	I/O	BS-PD2	Leave Open	
25	GPIO35	VCC_2V6	I/O	BS-PD2	Leave Open	
26	GPIO36	VCC_2V6	I/O	BS-PD2	Leave Open	
27	GPIO37	VCC_2V6	I/O	BS-PD2	Leave Open	
28	GPIO38	VCC_2V6	I/O	BS-PD2	Leave Open	
29	GPIO39	VCC_2V6	I/O	BS-PD2	Leave Open	
30	RXD2	VCC_1V8	O	DO6	Leave Open	Auxiliary RS232 Receive
31	TXD2	VCC_1V8	I	DI	Leave Open	Auxiliary RS232 Transmit
32	CTS2	VCC_1V8	O	DO2	Leave Open	Auxiliary RS232 Clear To Send
33	RTS2	VCC_1V8	I	DI	Leave Open	Auxiliary RS232 Request To Send
34	MIC2N	Analog	I	AI	Leave Open	Micro 2 Input Negative
35	HPH_OUT_L_P	Analog	O	AO	Leave Open	Speaker 1 Output Positive, 32 Ohm Output
36	MIC2P	Analog	I	AI	Leave Open	Micro 2 Input Positive

Pin #	Signal Name	Voltage	I/O*	Pin Type	If Unused	Description
37	HPH_OUT_R_N	Analog	O	AO	Leave Open	Speaker 1 Output Negative, 32 Ohm Output
38	LINE_IN_R_N	Analog	I	AI	Ground	Micro 1 Input Negative
39	SPKR_OUT_P	Analog	O	AO	Leave Open	Speaker 2 Output Positive, 8 Ohm Output
40	LINE_IN_L_P	Analog	I	AI	Ground	Micro 1 Input Positive
41	SPKR_OUT_N	Analog	O	AO	Leave Open	Speaker 2 Output Negative, 8 Ohm Output
42	EBI2_LB_N	VCC_1V8	O	DO10	Leave Open	Lower Byte select
43	GPIO40	VCC_2V6	I/O	BS-PD2	Leave Open	
44	SCL	VCC_2V6	O	B2	Leave Open	I ² C Clock
45	GPIO41	VCC_2V6	I/O	BS-PD2	Leave Open	
46	SDA	VCC_2V6	I/O	B2	Leave Open	I ² C Data
47	GPIO42	VCC_2V6	I/O	BS-PD2	Leave Open	
48	GPIO43	VCC_2V6	I/O	BS-PD2	Leave Open	
49	GPIO44	VCC_2V6	I/O	BS-PD2	Leave Open	
50	GPIO7	VCC_1V8	I/O		Leave Open	
51	GPIO51	VCC_1V8	I/O	BS-NP6	Leave Open	
52	VPAD-USB	VPAD-USB	I	AI	Leave Open	USB Power supply input
53	GPIO50	VCC_1V8	I/O	BS-PD2	Leave Open	
54	USB-DP	VPAD-USB	I/O	AI, AO	Leave Open	USB Data
55	GPIO45	VCC_2V6	I/O	BS-PD2	Leave Open	
56	USB-DM	VPAD-USB	I/O	AI, AO	Leave Open	USB Data
57	GPIO46	VCC_2V6	I/O	BS-PD2	Leave Open	
58	GPIO49	VCC_2V6	I/O	BS-PU2	Leave Open	
59	COL0	VCC_1V8	I/O	BS2	Leave Open	Keypad column 0
60	COL1	VCC_1V8	I/O	BS2	Leave Open	Keypad column 1
61	COL2	VCC_1V8	I/O	BS2	Leave Open	Keypad column 2
62	COL3	VCC_1V8	I/O	BS2	Leave Open	Keypad column 3
63	COL4	VCC_1V8	I/O	BS2	Leave Open	Keypad column 4
64	ROW4	VCC_1V8	I/O	DO2	Leave Open	Keypad Row 4
65	ROW3	VCC_1V8	I/O	DO2	Leave Open	Keypad Row 3
66	ROW2	VCC_1V8	I/O	DO2	Leave Open	Keypad Row 2
67	ROW1	VCC_1V8	I/O	DO2	Leave Open	Keypad Row 1
68	ROW0	VCC_1V8	I/O	DO2	Leave Open	Keypad Row 0
69	RI1	VCC_2V6	O	BS-PD2	Leave Open	Main RS232 Ring Indicator
70	DCD1	VCC_2V6	O	BS-PD2	Leave Open	Main RS232 Data Carrier Detect
71	TXD1	VCC_2V6	I	DI	Must be used	Main RS232 Transmit
72	RTS1	VCC_2V6	I	DI	Must be used	Main RS232 Request To Send
73	RXD1	VCC_2V6	O	DO4	Must be used	Main RS232 Receive
74	DSR1	VCC_2V6	O	BS-PD2	Leave Open	Main RS232 Data Set Ready
75	CTS1	VCC_2V6	O	DO4	Must be used	Main RS232 Clear To Send

Pin #	Signal Name	Voltage	I/O*	Pin Type	If Unused	Description
76	DTR1	VCC_2V6	I	BS-PD2	Leave Open	Main RS232 Data Terminal Ready
77	PCM_SYNC	VCC_1V8	O	B2	Leave Open	PCM Frame Synchronize
78	PCM_DIN	VCC_1V8	I	B2	Leave Open	PCM Data Input
79	PCM_CLK	VCC_1V8	O	B2	Leave Open	PCM Clock
80	PCM_DOUT	VCC_1V8	O	B2	Leave Open	PCM Data Output
81	EBI2_OE_N	VCC_1V8	O	DO10	Leave Open	Output Enable/ Read not write
82	Reserved				Leave Open	Reserved
83	EBI2_CS0_N	VCC_1V8	O	DO10	Leave Open	Chip Select
84	EBI2_WE_N	VCC_1V8	O	DO10	Leave Open	Write Enable
85	EBI2_AD0	VCC_1V8	I/O	B-K10	Leave Open	Data for Peripheral
86	EBI2_AD15	VCC_1V8	I/O	B-K10	Leave Open	Data for Peripheral
87	EBI2_AD1	VCC_1V8	I/O	B-K10	Leave Open	Data for Peripheral
88	EBI2_AD14	VCC_1V8	I/O	B-K10	Leave Open	Data for Peripheral
89	EBI2_AD2	VCC_1V8	I/O	B-K10	Leave Open	Data for Peripheral
90	EBI2_AD13	VCC_1V8	I/O	B-K10	Leave Open	Data for Peripheral
91	EBI2_AD3	VCC_1V8	I/O	B-K10	Leave Open	Data for Peripheral
92	EBI2_AD12	VCC_1V8	I/O	B-K10	Leave Open	Data for Peripheral
93	EBI2_AD4	VCC_1V8	I/O	B-K10	Leave Open	Data for Peripheral
94	EBI2_AD11	VCC_1V8	I/O	B-K10	Leave Open	Data for Peripheral
95	EBI2_AD5	VCC_1V8	I/O	B-K10	Leave Open	Data for Peripheral
96	EBI2_AD10	VCC_1V8	I/O	B-K10	Leave Open	Data for Peripheral
97	EBI2_AD6	VCC_1V8	I/O	B-K10	Leave Open	Data for Peripheral
98	EBI2_AD9	VCC_1V8	I/O	B-K10	Leave Open	Data for Peripheral
99	EBI2_AD7	VCC_1V8	I/O	B-K10	Leave Open	Data for Peripheral
100	EBI2_AD8	VCC_1V8	I/O	B-K10	Leave Open	Data for Peripheral

*NOTE: I = Inputs to the AirPrime Q26Elite and O = Outputs from the AirPrime Q26Elite.

Table 44: Pin Type Definition

Symbol	Description
Pad type	
AI	Analog input
AO	Analog output
B, BS	Bidirectional, bidirectional with Schmitt trigger
DI, DIS	Digital CMOS input, digital input with Schmitt trigger
DO	Digital output
Pad type - pull/keep details for digital I/Os	
PU	Contains an internal pull-up device
PD	Contains an internal pull-down device
K	Contains an internal weak keeper device (keepers cannot drive external buses)
#	Drive Strength for digital I/Os



SIERRA
WIRELESS