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Modules

Product Technical Specification

HL780x

June 2025

41113770 Rev. 12

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Revision History

Revision number	Release date	Changes
1	August 2020	Merged HL7800/HL7800-M PTS (Doc#41111094) and HL7802 PTS (Doc#41112974)) into common document; overall content update
2	September 2020	Updated topic VGPIO Monitoring and Buffer Control — removed recommended circuit
3	October 2020	Restored Japan certification details
4	March 2021	Updated Table 2-2 (Isolate required; footnotes) Updated topic Digital I/O Characteristics (description) Updated topic VGPIO (description) Updated topic I/O Behavior in Hibernate Mode (description) Updated Table 4-7 (Default State) Added topic UART1_RTS/UART1_CTS Updated Table 4-10 (T4, T7 timing) Added topic Power Down, Off, and VBAT Removal Updated Table 4-11 (Active) Updated Table 4-31 (timing values) Updated topic Hibernate — Isolation Requirements
5	February 2022	Updated footnote e under Table 4-7 Changed 3GPP Release 13 to 3GPP Release 14 Added note for GNSS under Table 1-4
6	August 2022	Added new note under Current Consumption
7	December 2022	Updated Current Consumption (test conditions note) Updated Tables 3-6, 3-7, 3-8, 3-9
8	February 2023	Updated pin definition for C21 on Table 2-2 Removed Backup Battery for Real Time Clock (BAT_RTC) feature definition Added Table 1-7

Revision number	Release date	Changes
9	April 2023	Removed BAT_RTC from Figure 1-2 and Interfaces and
10	June 2024	Removed note under 4.6.2 Host-Managed POWER_ON_N Updated 8.3 Compliance Acceptance and Certification
11	September 2024	Updated step 1 under 4.7.1 Software Power Off in Unmanaged Mode
12	June 2025	Updated Preface Updated Table 1-7: Values for ATEX Compliance Updated Table 3-6: HL7800 / HL7800-M LPM Current Consumption — Cat-M1 Updated Table 3-7: HL7800 / HL7800-M LPM Current Consumption — Cat-NB1 Updated Table 3-8: HL7802 LPM Current Consumption — Cat-M1 Updated Table 3-9: HL7802 LPM Current Consumption — Cat-NB1a Added Figure 3-5: Floor current range of Lite hibernate mode based on chip sets variation distribution Updated C46 under Table 4-6: GPIO Pin Descriptions Updated 6.6.1 Antenna Matching Circuit

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1: Introduction

This document defines the high-level product features and illustrates the interfaces for HL780x Essential Connectivity Modules (HL7800, HL7800-M, HL7802), designed for M2M and Internet of Things (IoT) markets. It covers the hardware aspects of the product series, including electrical and mechanical. For additional documentation (e.g. Firmware Customer Release Notes, AT Command Reference, etc.), refer to the module page at source.sierrawireless.com.

Note: 'HL780x' collectively identifies HL7800, HL7800-M, and HL7802. Variant-specific content is identified where applicable.

The HL780x supports a variety of interfaces such as USB FS, UART, ADC, GPIOs, and also supports the low power consumption hibernation modes to provide customers with flexibility in implementing high-end solutions.

Note:

- *The key differentiators between HL780x variants are regulatory and industrial approvals/certifications, and supported radio access technologies (RATs)—HL7800 supports Cat-M1/NB-IoT, HL7800-M supports Cat-M1, and HL7802 supports Cat-M1/NB-IoT/2G.*
- *Semtech modules are shipped factory-programmed with industry or mobile operator approved firmware, according to the specific SKU ordered. Periodically, newer firmware versions become available and can include new features, bug fixes, or critical security updates. Semtech strongly recommends that customers establish their own production capability for updating module firmware on their assembled end platform, in the event that a newer firmware must be installed before deployment. Semtech also recommends customers design their products to support post-deployment FOTA upgrades using the AirVantage cloud platform.*

1.1 Supported RF Bands/Connectivity

The HL780x is a Ready-to-Connect (R2C) module that supports the use of its embedded SIM (eSIM) or an external SIM for global data connectivity on the RF bands detailed in the following module-specific tables.

For details about using the HL780x's eSIM with Sierra Smart Connectivity, refer to the Sierra Wireless Ready-to-Connect Module Integration Guide. For additional information on Sierra Smart Connectivity, explore www.sierrawireless.com or contact Semtech.

Table 1-1: HL780x Supported RF Bands/Connectivity

Module	RF Band	Transmit (TX) Frequency (MHz)	Receive (Rx) Frequency (MHz)	Cat-M1	Cat-NB1[a]	2G
HL7800 HL7800-M[a] HL7802	LTE B1	1920–1980	2110–2170	Y	Y	
	LTE B2	1850–1910	1930–1990	Y	Y[b]	
	LTE B3	1710–1785	1805–1880	Y	Y	
	LTE B4	1710–1755	2110–2155	Y	Y[b]	
	LTE B5	824–849	869–894	Y	Y[b]	
	LTE B8	880–915	925–960	Y	Y	
	LTE B9	1749.9–1784.9	1844.9–1879.9	See [c]	See [c]	
	LTE B10	1710–1770	2110–2170	See [c]	See [c]	
	LTE B12	699–716	729–746	Y	Y[b]	
	LTE B13	777–787	746–756	Y	Y[b]	
	LTE B17	704–716	734–746	See [c]	Y	
	LTE B18	815–830	860–875	Y	Y	
	LTE B19	830–845	875–890	Y	Y	
	LTE B20	832–862	791–821	Y	Y	
	LTE B25	1850–1915	1930–1995	Y	Y[b]	
	LTE B26	814–849	859–894	Y	Y[b]	
	LTE B27	807–824	852–869	Y	See [c]	
	LTE B28	703–748	758–803	Y	Y	
	LTE B66	1710–1780	2110–2200	Y	Y[b]	
HL7802	GSM 850	824–849	869–894			Y
	E-GSM 900	880–915	925–960			Y
	DCS 1800	1710–1785	1805–1880			Y
	PCS 1900	1850–1910	1930–1990			Y

a. Cat-NB1 supported by HL7800/HL7802 only; not supported by HL7800-M
b. To ensure FCC compliance near NB band edges, Cat-NB1 supported TX channel ranges do not include outer channels. Supported channels ranges are:
   - B2: 18602–19198
   - B4: 19952–20398
   - B5: 20402–20648
   - B12: 23012–23178
   - B13: 23182–23278
   - B25: 26042–26688
   - B26: 26692–27038
   - B66: 131974 - 132670
c. Will be supported in a future release.

1.2 Common Flexible Form Factor (CF3)

The HL780x belongs to Semtech's Common Flexible Form Factor (CF3) family of WWAN modules. These modules share the same mechanical dimensions (same width and length with varying thicknesses) and footprint. The CF3 form factor provides a unique solution to a series of problems faced commonly in the WWAN module space as it:

- Accommodates multiple radio technologies (from GSM to LTE advanced) and band groupings
- Supports bit-pipe (Essential Module Series, such as the HL780x) and value-add (Smart Module Series) solutions
- Offers electrical and functional compatibility
- Provides direct mount, as well as socket mount (depending on customer needs, e.g. for use in development kits or for prototype development)

1.3 Physical Dimensions and Connection Interface

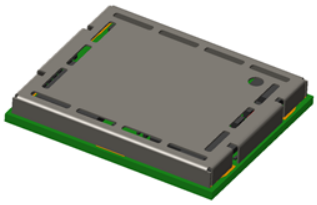
HL780x modules are compact, robust, fully shielded industrial-grade embedded modules with the dimensions noted in Table 1-2.

Table 1-2: Module Dimensions[a]

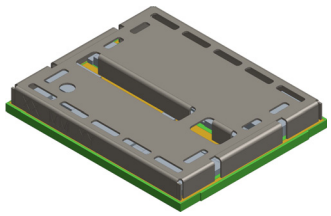
Parameter	Nominal	Tolerance	Units
Length	18.0	±0.10	mm
Width	15.0	±0.10	mm
Thickness	2.4	±0.20	mm
Weight	1.17	±0.24	g

a. Typical dimensional values, accurate as of the release date of this document.

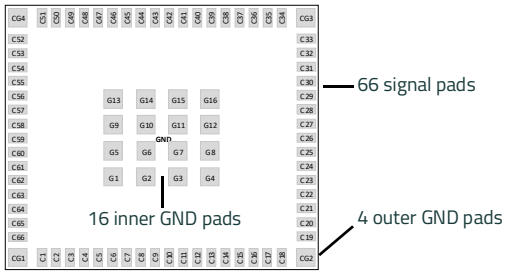
All electrical and mechanical connections to the HL780x module are made through the 86 Land Grid Array (LGA) pads on the bottom side of the PCB.



HL7800/HL7800-M Top View



HL7802 Top View



Bottom View

Figure 1-1: Mechanical Overview

Table 1-3 describes the LGA pads.

Table 1-3: LGA Pad Types / Distribution

Pad Type	Quantity	Dimensions	Pitch
Signal pads	66 pads	1.0×0.5 mm	0.8 mm
Ground pads	16 inner pads	1.0×1.0 mm	1.825 mm / 1.475 mm
	4 outer corner pads	0.85×0.97 mm	-

1.4 General Features

Table 1-4 summarizes the HL780x's features.

Table 1-4: General Features

Feature	Description
Physical	▪ Small form factor (86-pad solderable LGA pad). See Physical Dimensions and Connection Interface for details. ▪ Metal shield can ▪ RF connection pads (RF_MAIN and RF_GNSS) ▪ Baseband signals connection
Power supply	3.2–4.35 V supply voltage (VBAT_BB, VBAT_RF) ▪ Single supply (recommended) — VBAT (VBAT_BB tied to VBAT_RF) or ▪ Dual supplies — Single supply each for VBAT_BB and VBAT_RF
RF	▪ 2G (HL7802 only) · 850/900 Power Class 4 (33 dBm), GPRS Class 10 · 1800/1900 Power Class 1 (30 dBm), GPRS Class 10 ▪ Cat-M1 · Power Class 3 (23 dBm) ▪ Cat-NB1 (HL7800/HL7802 only) · Power Class 3 (23 dBm) ▪ GNSS · GPS — 1575.42 MHz · GLONASS — 1589.0625–1605.375 MHz See GNSS for details. *Note:* · The GNSS receiver and LTE/GSM receiver share the same RF resources, therefore GNSS can only be used when the module is not actively connected on LTE/GSM. An example of a suitable implementation of GNSS in an end product would be the use of GNSS positioning for asset management applications where infrequent and no real-time position updates are required. · The GNSS feature is not supported in NB-IoT mode.

Table 1-4: General Features (Continued)

Feature	Description
SIM interface	▪ 1.8V support ▪ SIM extraction / hot plug detection ▪ SIM/USIM support ▪ Conforms with ETSI UICC Specifications ▪ Supports SIM application tool kit with proactive UICC commands
Application interface	▪ AT command interface — 3GPP 27.007 standard, plus proprietary extended AT commands ▪ CMUX multiplexing over UART ▪ USB Full Speed (FS)
Protocol stack	▪ 2G (HL7802 only) · GPRS Class 10 ▪ Cat-M1 · 3GPP Rel. 13 · Half-duplex · Channel bandwidth — 1.4 MHz · LTE carrier bandwidth — 1.4/3/5/10/15/20 MHz · Up to 375 kbit/s uplink, 300 kbit/s downlink · Extended Coverage Mode A · PSM (Power Save Mode) · I-DRX (Idle Mode Discontinuous Reception) · C-DRX (Connected Mode Discontinuous Reception) · Idle mode mobility · Connected mode mobility · eDRX (Extended Discontinuous Reception) · Control Plane CIoT Optimization (Data over NAS) ▪ Cat-NB1 (HL7800/HL7802 only) · 3GPP Rel. 13 · Half-duplex · Channel bandwidth — 180 kHz · LTE carrier bandwidth — 1.4/3/5/10/15/20 MHz · Up to 100 kbit/s in downlink · Operational mode — In-band, Guard band, Standalone · Control Plane CIoT Optimization (Data over NAS) · NIDD over SGi tunneling · NIDD over SCEF · Extended coverage · PSM (Power Save Mode) · I-DRX (Idle Mode Discontinuous Reception) · C-DRX (Connected Mode Discontinuous Reception) · Idle mode mobility · eDRX (Extended Discontinuous Reception) ▪ Flexible selection · Manual system selection across RATs · Dynamic system selection across RATs (preferred RAT)[a]

Table 1-4: General Features (Continued)

Feature	Description
SMS	▪ SMS over SG ▪ MO/MT ▪ SMS storage to SIM card or ME storage
Connectivity	▪ Multiple cellular packet data profiles ▪ Sleep mode for minimum idle power draw ▪ Mobile-originated PDP context activation / deactivation ▪ Static and Dynamic IP address. The network may assign a fixed IP address or dynamically assign one using DHCP (Dynamic Host Configuration Protocol). ▪ PDP context type (IPv4, IPv6, IPv4v6) ▪ RFC1144 TCP/IP header compression
Environmental	Operating temperature ranges · Class A: -30°C to +70°C · Class B: -40°C to +85°C
RTC	Real Time Clock (RTC)

a. Available in a future release.

1.5 Architecture

Figure 1-1 presents an overview of the HL780x's internal architecture and external interfaces.

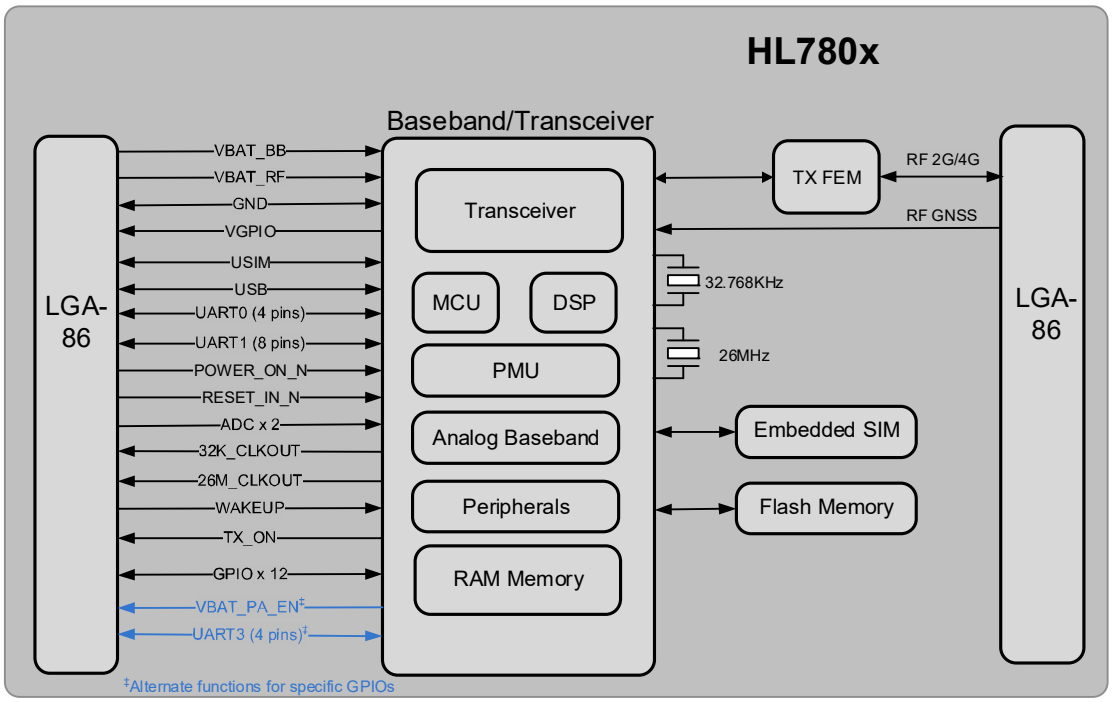


Figure 1-2: Architecture Overview

1.6 Interfaces

The HL780x provides the following interfaces and peripheral connectivity:

- (1) VGPIO (1.8V) — See VGPIO.
- (1) 1.8V USIM — See USIM Interface.
- (1) USB 2.0 FS — See USB Interface.
- (12) GPIOs — See General Purpose Input/Output (GPIO).
- (1) 8-wire UART — See Main Serial Link (UART1).
- (1) Active low power on signal (will be available in a future firmware release) — See Power On Signal (POWER_ON_N).
- (1) Active low reset signal — See Reset Signal (RESET_IN_N).
- (2) ADC — See Analog to Digital Converter (ADC).
- (2) System clock out (32.768 kHz and 26 MHz) — See Clock Interface.
- (1) 4-wire UART for debug interface only — See Debug Interfaces.
- (1) Wake up signal — See Wake Up Signal (WAKEUP).
- (1) Main RF Antenna — See RF Interface.
- (1) TX_ON indicator — See TX Burst Indicator (TX_ON).
- (1) GNSS Antenna — See GNSS.
- (1) External PA Voltage Control Indicator — See Tx/Rx Activity Indicator; External RF Voltage Control.

Table 1-5: ESD Specifications [a]

Category	Connection	Specification
Operational	▪ Power supply (C61, C62, C63) ▪ RF ports (C38, C49)	IEC-61000-4-2 (Electrostatic Discharge Immunity Test) · ±6 kV Contact · ±8 kV Air
Non-operational	All pins	Unless otherwise specified: ▪ JESD22-A114 ± 250 V Human Body Model ▪ JESD22-C101C ± 250V Charged Device Model

a. ESD protection is highly recommended on customer platform. For details, see Design Guidelines.

1.7 Environmental Specifications

The environmental specifications for operation and storage of the HL780x are defined in Table 1-6.

Table 1-6: Environmental Specifications

Parameter	Range	Operating Class
Ambient Operating Temperature	-30°C to +70°C	Class A
	-40°C to +85°C	Class B
Ambient Storage Temperature	-40°C to +85°C	-

Class A is defined as the operating temperature range within which the device:

- Shall exhibit normal function during and after environmental exposure.
- Shall meet the minimum requirements of 3GPP or appropriate wireless standards.

Class B is defined as the operating temperature range within which the device:

- Shall remain fully functional during and after environmental exposure
- Shall exhibit the ability to establish any of the device's supported call modes (SMS, Data, and emergency calls) at all times even when one or more environmental constraint exceeds the specified tolerance.
- Unless otherwise stated, full performance should return to normal after the excessive constraint(s) have been removed.

1.7.1 ATEX Compliance

The following table lists the inductor and capacitor values to be considered for ATEX certification of the system hosting the HL7800 and HL7800-M modules. All supplies in the modules are linear LDO except for one 1.3V DC/DC step-down.

Table 1-7: Values for ATEX Compliance

Module	Parameter	Value	Tolerance
HL7800	Total Inductance	2.21 µH	30%
	Total Capacitance	43.64 µH	20%
HL7802	Total Inductance	2.29 µH	30%
	Total Capacitance	57.56 µH	20%

2: Pad Definition

HL780x pins are divided into three categories.

- Core functions and associated pins — Cover all the mandatory features for M2M connectivity and will be available by default across the Essential Connectivity CF3 module family. These Core functions are always available and always at the same physical pad locations. A customer platform using only these functions and associated pads is guaranteed to be forward and/or backward compatible with the next generation of CF3 Essential Connectivity modules.
- Extension functions and associated pins — Bring additional capabilities to the customer. Whenever an Extension function is available on a module, it is always at the same pad location.
- Custom functions and associated pins — Module-specific functionality. If a custom function is available on another module, there is no guarantee that it will be at the same pad location.

For example:

- UART1 interface is a "Core" function on pins C2–C9 that is available on all CF3 Essential Connectivity modules (including HL780x).
- USB interface is an "Extension" function on pins C12–C13 that is available on HL780x modules, but may not be available on certain other CF3 Essential Connectivity modules.
- UART0 signals are "Custom" functions on pins C57 and C58. These signals may or may not be available on other CF3 Essential Connectivity modules and, if available, may be on different pins.

Pins marked as "Not connected" should not be used.

2.1 Pin Types

Table 2-1 lists a series of codes used to identify pin characteristics throughout this document.

Table 2-1: Pin Type Codes

Code	Definition	Code	Definition
AI	Analog Input	O	Digital Output
ANT	Antenna	PD	Pull-down enabled
GND	Ground	PI	Power In
I	Digital Input	PO	Power Out
I/O	Digital Input/Output	PU	Pull-up enabled
N/A	Not applicable		

Table 2-2: Pin Definitions

Pin	Signal Name	Group	I/O	Voltage Supply Domain	Function	Recommendation for unused pads	Isolate required [a]	CF3 Category
C1	GPIO1	GPIO[b]	I/O	1.8V (VGPIO)	General purpose input/output	Leave open	Yes	Extension
C2	UART1_RI[c]	UART1[b]	O	1.8V (VGPIO)	UART1 Ring Indicator	Leave open	Yes	Core
C3	UART1_RTS	UART1[b]	I	1.8V (VGPIO)	UART1 Request To Send	Mandatory connection	Yes	Core
C4	UART1_CTS	UART1[b]	O	1.8V (VGPIO)	UART1 Clear To Send	Mandatory connection	Yes	Core
C5	UART1_TX	UART1[b]	I	1.8V (VGPIO)	UART1 Transmit Data	Mandatory connection	Yes	Core
C6	UART1_RX	UART1[b]	O	1.8V (VGPIO)	UART1 Receive Data	Mandatory connection	Yes	Core
C7	UART1_DTR	UART1[b]	I	1.8V (VGPIO)	UART1 Data Terminal Ready	Leave open	Yes	Core
C8	UART1_DCD	UART1[b]	O	1.8V (VGPIO)	UART1 Data Carrier Detect	Leave open	Yes	Core
C9	UART1_DSR	UART1[b]	O	1.8V (VGPIO)	UART1 Data Set Ready	Leave open	Yes	Core
C10	GPIO2	GPIO[b]	I/O	1.8V (VGPIO)	General purpose input/output	Leave open	Yes	Core
C11	RESET_IN_N	H/W Control[d]	I	Internal Bias	Input reset signal	Leave open	No	Core
C12	USB_D-	USB	I/O	3.3V	USB Data Negative (Full Speed)	Leave open	No	Extension
C13	USB_D+	USB	I/O	3.3V	USB Data Positive (Full Speed)	Leave open	No	Extension
C14	NC	Not connected			Not Connected	See footnote[e]	No	Not connected
C15	NC	Not connected			Not Connected	See footnote[e]	No	Not connected
C16	USB_VBUS	USB	PI	5V	USB VBUS	If USB is: ▪ Not used — Leave open ▪ Used — Mandatory connection	No	Extension
C17	NC	Not connected			Not Connected	See footnote[e]	No	Not connected
C18	NC	Not connected			Not Connected	See footnote[e]	No	Not connected
C19	NC	Not connected			Not Connected	See footnote[e]	No	Not connected
C20	NC	Not connected			Not Connected	See footnote[e]	No	Not connected

Table 2-2: Pin Definitions (Continued)

Pin	Signal Name	Group	I/O	Voltage Supply Domain	Function	Recommendation for unused pads	Isolate required [a]	CF3 Category
C21	NC	Not Connected			Not connected	Leave open	No	Not connected
C22	26M_CLKOUT	Clock[b]	O	1.8V (VGPIO)	26 MHz System Clock Output	Leave open	Yes	Extension
C23	32K_CLKOUT	Clock[b]	O	1.8V (VGPIO)	32.768 kHz System Clock Output	Leave open	Yes	Extension
C24	ADC1	ADC[b]	AI	1.8V (VGPIO)	Analog to digital converter	Leave open	Yes	Extension
C25	ADC0	ADC[b]	AI	1.8V (VGPIO)	Analog to digital converter	Leave open	Yes	Extension
C26	UIM1_VCC	UIM[b]	PO	1.8V	USIM1 Power supply	Leave open	No	Core
C27	UIM1_CLK	UIM[b]	O	1.8V (VGPIO)	USIM1 Clock	Leave open	No	Core
C28	UIM1_DATA	UIM[b]	I/O	1.8V (VGPIO)	USIM1 Data	Leave open	No	Core
C29	UIM1_RESET	UIM[b]	O	1.8V (VGPIO)	USIM1 Reset	Leave open	No	Core
C30	RF_DIV_GND_1	Ground	GND	Ground	Ground	Mandatory connection	No	Extension
C31	NC	Not connected			Not Connected	See footnote[e]	No	Not connected
C32	RF_DIV_GND_2	Ground	GND	Ground	Ground	Mandatory connection	No	Extension
C33	Reserved	Reserved			Reserved	Leave open[f]	No	Extension
C34	Reserved	Reserved			Reserved	Leave open[f]	No	Extension
C35	Reserved	Reserved			Reserved	Leave open[f]	No	Extension
C36	Reserved	Reserved			Reserved	Leave open[f]	No	Extension
C37	RF_GNSS_GND_1	Ground	GND	Ground	Ground (RF_GNSS)	Mandatory connection	No	Core
C38	RF_GNSS	Antenna	ANT		GNSS antenna input	Leave open	No	Extension
C39	RF_GNSS_GND_2	Ground	GND	Ground	Ground (RF_GNSS)	Mandatory connection	No	Core
C40	GPIO7	GPIO[b]	I/O	1.8V (VGPIO)	General purpose input/output	Leave open	Yes	Core
C41	GPIO8	GPIO[b]	I/O	1.8V (VGPIO)	General purpose input/output	Leave open	Yes	Core
	VBAT_PA_EN		O		Tx/Rx activity indicator/External RF voltage control			Custom

Table 2-2: Pin Definitions (Continued)

Pin	Signal Name	Group	I/O	Voltage Supply Domain	Function	Recommendation for unused pads	Isolate required [a]	CF3 Category
C42	NC	Not connected			Not Connected	See footnote[e]	No	Not connected
C43	Reserved	Reserved			Reserved	Leave open[f]	No	Extension
C44	WAKEUP	H/W Control[d]	I	1.8V	Wake up signal	Mandatory connection	No	Extension
C45	VGPIO	Power	PO	1.8V (VGPIO)	GPIO voltage output (reference voltage)	Leave open	No	Core
C46	GPIO6	GPIO[b]	I/O	1.8V (VGPIO)	General purpose input/output	Leave open	Yes	Core
C47	NC	Not connected			Not Connected	Leave open[e]	No	Not connected
C48	RF_MAIN_GND_1	Ground	GND	Ground	Ground (RF_MAIN)	Mandatory connection	No	Core
C49	RF_MAIN	Antenna	ANT		Main RF antenna input/output (Rx/Tx)	Mandatory connection	No	Core
C50	RF_MAIN_GND_2	Ground	GND	Ground	Ground (RF_MAIN)	Mandatory connection	No	Core
C51	GPIO14	GPIO[b]	I/O	1.8V (VGPIO)	General purpose input/output	Leave open	Yes	Extension
	UART3_CTS	UART3[b]	O		(MLI debug) UART3 Clear To Send			Custom
C52	GPIO10	GPIO[b]	I/O	1.8V (VGPIO)	General purpose input/output	Leave open	Yes	Extension
	UART3_TX	UART3[b]	I		(MLI debug) UART3 Transmit data			Custom
C53	GPIO11	GPIO[b]	I/O	1.8V (VGPIO)	General purpose input/output	Leave open	Yes	Extension
	UART3_RTS	UART3[b]	I		(MLI debug) UART3 Request To Send			Custom
C54	GPIO15	GPIO[b]	I/O	1.8V (VGPIO)	General purpose input/output	Leave open	Yes	Extension
	UART3_RX	UART3[b]	O		(MLI debug) UART3 Receive data			Custom
C55	UART0_RX	UART0[b]	O	1.8V (VGPIO)	Debug Receive data	Leave open	Yes	Extension
C56	UART0_TX	UART0[b]	I	1.8V (VGPIO)	Debug Transmit data	Leave open	Yes	Extension
C57	UART0_CTS	UART0[b]	O	1.8V (VGPIO)	Debug Clear To Send	Leave open	Yes	Custom
C58	UART0_RTS	UART0[b]	I	1.8V (VGPIO)	Debug Request To Send	Leave open	Yes	Custom

Table 2-2: Pin Definitions (Continued)

Pin	Signal Name	Group	I/O	Voltage Supply Domain	Function	Recommendation for unused pads	Isolate required [a]	CF3 Category
C59	POWER_ON_N	H/W Control[d]	I	Internal Bias	Active-low Power On control signal	Leave open	No	Core
C60	TX_ON	Indication[b]	O	1.8V (VGPIO)	TX transmission indication	Leave open	Yes	Extension
C61	VBAT_RF	Power	PI	3.2V (min) 3.7V (typ) 4.35V (max)	Power supply	Mandatory connection	No	Core
C62	VBAT_RF	Power	PI	3.2V (min) 3.7V (typ) 4.35V (max)	Power supply	Mandatory connection	No	Core
C63	VBAT_BB	Power	PI	3.2V (min) 3.7V (typ) 4.35V (max)	Power supply	Mandatory connection	No	Core
C64	UIM1_DET	UIM1[b]	I	1.8V (VGPIO)	UIM1 Detection	Leave open	Yes	Core
	GPIO3	GPIO[b]	I/O		General purpose input/output			Extension
C65	GPIO4	GPIO[b]	I/O	1.8V (VGPIO)	General purpose input/output	Leave open	Yes	Extension
C66	GPIO5	GPIO[b]	I/O	1.8V (VGPIO)	General purpose input/output	Leave open	Yes	Extension
CG1–CG4	GND	Ground	GND	Ground	Ground	Mandatory connection	No	Core
G1–G16	GND	Ground	GND	Ground	Ground	Mandatory connection	No	Core

a. The host platform should isolate these signals during module Hibernate mode to prevent back-powering the module. For details, see Hibernate — Isolation Requirements.
b. By default, signals in group (GPIO, UART, UIM1, ADC, Clock, Indication) are hardware-configured as inputs and are in an undefined state during OFF, reset, and Hibernate modes. The host should ignore all activity on these signals until the module has initialized and reached AT-READY (UART1_CTS transitions from high to low (and stays low) and VGPIO is high, indicating the UART and USB interfaces are ready). For timing details, see Unmanaged POWER_ON_N (Default) and Wakeup from OFF Mode.
For further information regarding pre- and post-AT-READY signal states, contact Sierra Wireless.
c. UART1_RI cannot be used in Hibernate mode. A GPIO (GPIO2 by default) can be configured as an alternate ring indicator. For details, see Ring Indicator (UART1_RI or Alternative).
d. Hardware Control signals are available in all module operational modes and determine module behavior. For recommendations on managing these signals, see associated signal topics in Detailed Interface Specifications.
e. Pin is not connected internally, but is reserved for future use. Leave unconnected to ensure compatibility with other SemtechCF3 modules.
f. Pin is connected internally, leave open.

Pad Configuration

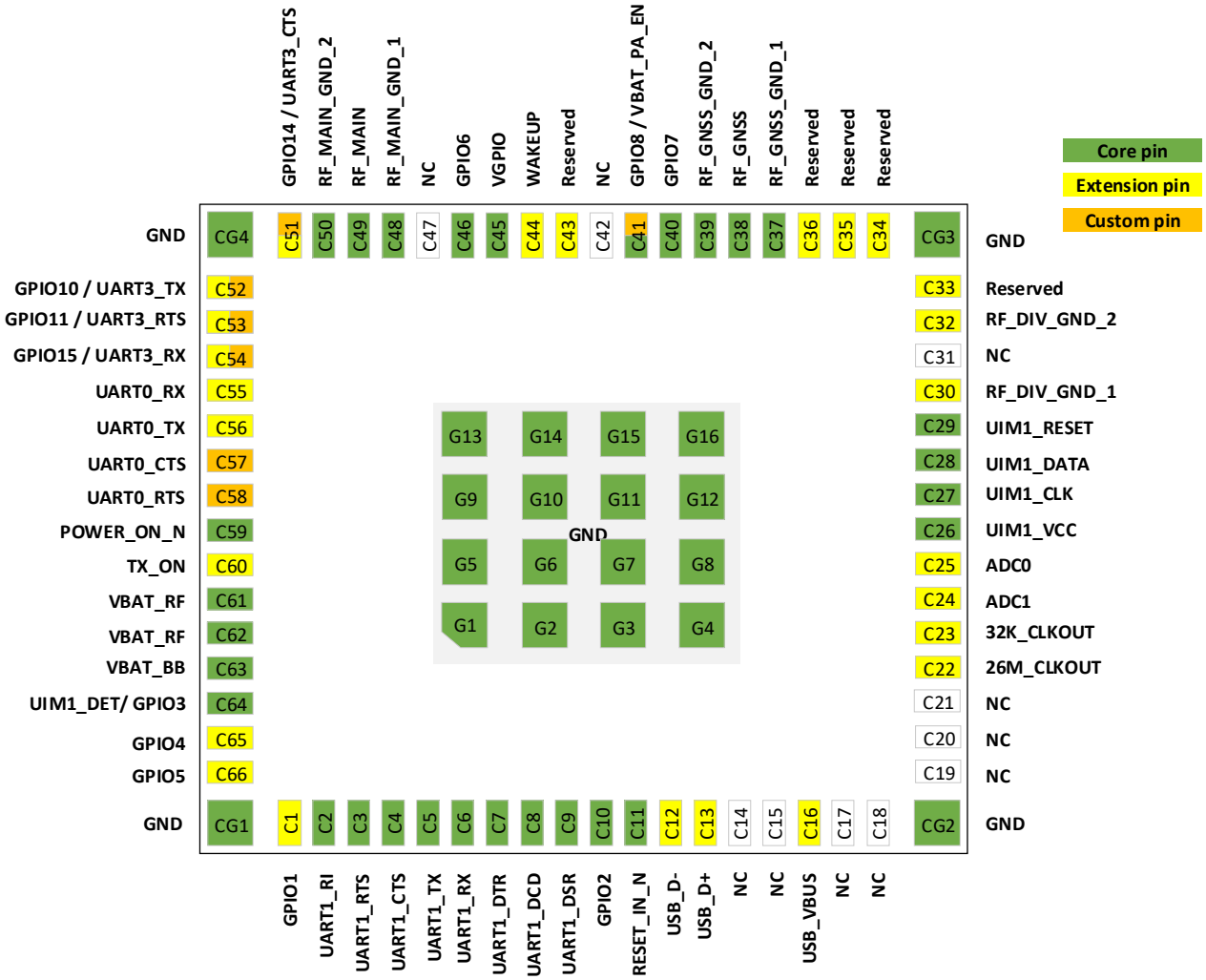


Figure 2-1: Pad Configuration (Top View through Module)

3: Power Specifications

Note: If not specified, all electrical values are given for VBAT_BB and VBAT_RF = 3.7V, operating temperature of 25 °C. and with conducted 50Ω load on RF port(s).

3.1 Power Supply

The module is supplied through the VBAT_BB and VBAT_RF signals.

For standard applications, VBAT_BB and VBAT_RF must be tied externally to the same power supply. For some specific applications (e.g. applications requiring a lower VBAT_RF), the module supports separate VBAT_BB and VBAT_RF connection as per Table 3-1.

Table 3-1 and Table 3-2 describe the Power Supply interface.

Table 3-1: Power Supply Pin Description

Pad #	Signal Name	I/O	Description
C63	VBAT_BB	PI	Power supply (baseband)
C61, C62	VBAT_RF	PI	Power supply (radio frequency)
C30, C32, C37, C39, C48, C50, CG1–CG4, G1–G16		GND	Ground

Caution: *Operation outside the minimum/maximum specified operating voltage (Table 3-2) is not recommended, and functional operation of the device and specified typical performance are neither implied nor guaranteed.*

Table 3-2: Power Supply Current Requirements

Parameter	Min	Typ	Max	Unit	Notes
VBAT_BB voltage	3.2	3.7	4.35	V	Must be within min/max values over all operating conditions (including voltage ripple, droop, and transient)
VBAT_RF voltage Full Specification	3.2	3.7	4.35	V	
VBAT_RF voltage Extended Range	2.8[a]	3.7	4.35	V	
Power Supply Ripple	-	-	100[b]	mVpp	

Table 3-2: Power Supply Current Requirements (Continued)

Parameter		Min	Typ	Max	Unit	Notes
Max Supply Current	VBAT_BB	-	–	300	mA	
	VBAT_RF (LTE)	-	–	▪ (HL7800/HL7800-M) 350 ▪ (HL7802) 400	mA	
	(HL7802 only) VBAT_RF (2G) Peak Current	-	1.9	2.5	A	

a. 3GPP performance is not guaranteed for VBAT_RF from 2.8–3.2V. Note that operation in this range requires a separate VBAT_RF supply.
b. Measured at nominal supply voltage (3.7V), nominal ambient temperature (25°C), and with conducted 50Ω load on RF port(s).

Note: The host power supply should be capable of supplying the following while meeting the min/max operating conditions of Table 3-2:
- *HL7800/HL7800-M: 650 mA ($VBAT\_BB_{max}$ + $VBAT\_RF_{max}$)*
- *HL7802: 2.8 A ($VBAT\_BB_{max}$ + $VBAT\_RF_{2Gpeak}$)*

3.2 Electrical Specifications

3.2.1 Digital I/O Characteristics

The I/O characteristics for supported digital interfaces/signals are described in Table 3-3. These interfaces/signals include:
- UARTs
- GPIOs
- Clock output signals
- UIM1
- TX_ON
- External PA voltage control indicator

These signals are not available in Hibernate mode since VGPIO is OFF.

Note: The host platform should isolate these signals during module Hibernate mode to prevent back-powering the module. For details, see Hibernate — Isolation Requirements.

Table 3-3: Digital I/O Electrical Characteristics (1.80V)[a]

Parameter	Description	Min	Max	Unit
V_{IH}	Logic High Input Voltage	0.7 × VGPIO	VGPIO	V
V_{IL}	Logic Low Input Voltage	0	0.3 × VGPIO	V
V_{OH}	Logic High Output Voltage	0.8 × VGPIO		V
V_{OL}	Logic Low Output Voltage		0.2 × VGPIO	V

Table 3-3: Digital I/O Electrical Characteristics (1.80V)[a] (Continued)

Parameter	Description	Min	Max	Unit
I_O	Output Current	2	4	mA
IR_{PD}	Internal Pull-Down Resistor current	11	43	µA
IR_{PU}	Internal Pull-Up Resistor current	11	44	µA
R_{PU}	Internal Pull-Up Resistor	13	45	kΩ
R_{PD}	Internal Pull-Down Resistor	13.6	45	kΩ

a. VGPIO = 1.8V (See VGPIO.)

3.3 3GPP Power Saving Features

This section describes 3GPP power saving features (PSM, eDRX) that are supported by the HL780x module. Per 3GPP specifications, these features pertain to the module's cellular communication.

The HL780x also features low power modes that contribute to power savings by selectively limiting or turning off other elements of the module, such as memory states, I/O states, etc. (For details, see HL780x Low Power Modes.)

3.3.1 Power Saving Mode (PSM)

Power Saving Mode (PSM) is a 3GPP feature that allows the HL780x to minimize power consumption by registering on a PSM-supporting LTE network and then entering PSM state for a configured duration.

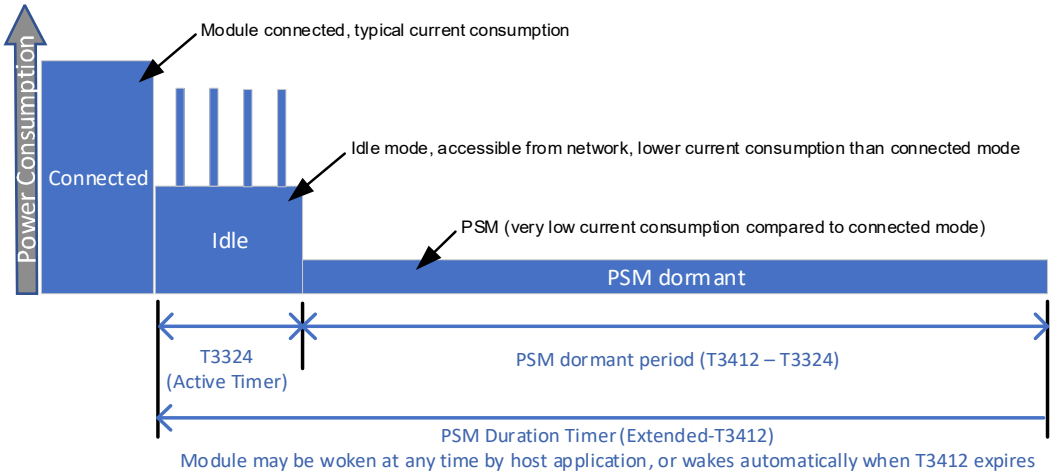


Figure 3-1: PSM — Timers

When the module enters the PSM state:

1. The module remains active (accessible from the network) in a lower-power idle state for a short period (T3324 Active Timer).
2. The module then drops to a very-low power 'dormant' state for the remainder of the PSM duration or until the host platform wakes the module to initiate a network contact. During this dormant period, the module is not accessible **from** the network.
3. After the module contacts the network (for either reason), the process repeats.

Using PSM, an HL780x-based host platform can reduce power consumption significantly because:

- It can enter a very low power state (~1.8 µA) during a very long PSM dormant period.
- The platform can wake the HL780x at any time to initiate data transaction immediately with minimal overhead (signaling/procedure) since the network keeps the module registered during the entire PSM period.

Typical candidates for PSM are systems (such as monitors and sensors) that:

- Require long battery life (low power consumption)
- Infrequently send mobile originated data (every few hours, days, weeks, etc.), with optional reply data from the network
- Tolerate modules being inaccessible for long periods of time
- Do not use mobile-terminated voice/data/SMS. If the host platform needs the module to be able to receive mobile-terminated data, eDRX is a more suitable option.

Figure 3-2 describes an example of a module operating in PSM. In a typical application, the module will always be woken from the dormant state to transmit data (illustrated in the 'Typical MO Use Case' portion of the figure). This is accomplished by setting the T3412 timer much longer than anticipated transmission frequency.

However, if the module is not woken by the host, a TAU will be sent when T3412 expires (illustrated in the 'Default PSM Use Case' portion of the figure). By setting the T3412 longer, unnecessary TAU transmissions can be avoided.

For a more detailed explanation of PSM, refer to the HL78xx Low Power Modes Application Note.

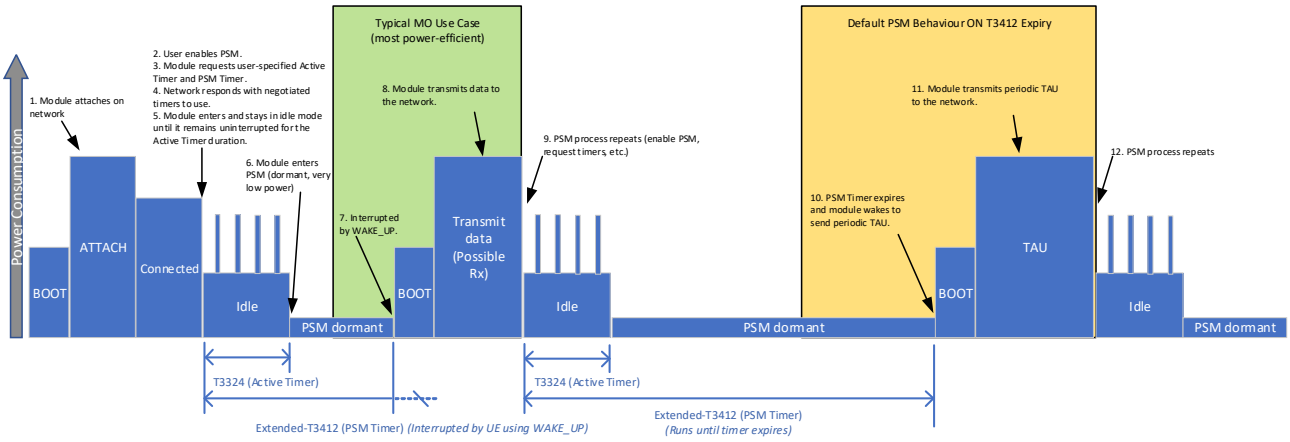


Figure 3-2: Power Saving Mode — Use Cases Example

3.3.2 Extended DRX (eDRX)

3.3.2.1 eDRX Overview

Extended Idle DRX (I-eDRX) is a 3GPP-specified extension of the Discontinuous Reception (DRX) low power consumption feature. This extension reduces the number of paging opportunities (PO) the module must monitor while in idle state, resulting in a corresponding decrease in power consumption.

Many data module applications are tolerant to delays in downlink data packets so extending the period between paging opportunities would allow for current consumption savings for these applications.

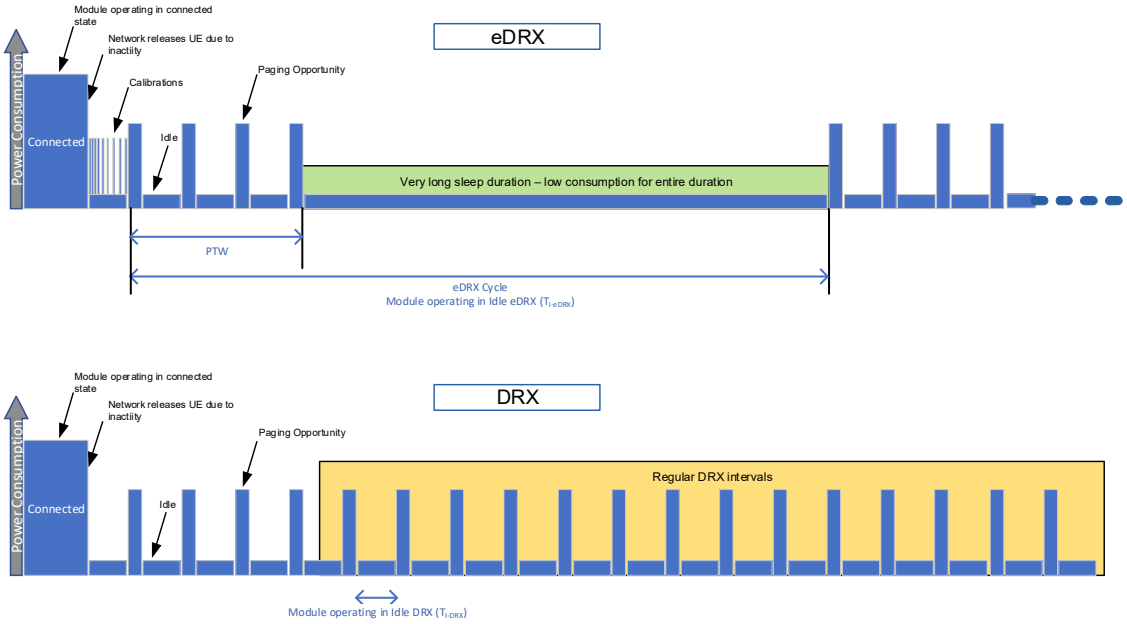


Figure 3-3: eDRX vs DRX

As shown in Figure 3-3, the HL780x supports eDRX, taking advantage of the feature by monitoring a set number of paging opportunities in a Paging Time Window (PTW) and then entering a low power state between PTWs. This sequence (PTW followed by low power state) comprises a single eDRX cycle. The size of the PTW and the length of the eDRX cycle (T_{I-eDRX}) are negotiated between the module (which submits desired values when enabling eDRX) and the network (which indicates the values that will actually be used).

The module remains in I-eDRX until it detects a page from the network during a PO or needs to access the network (e.g. to make a data connection, send a mobility TAU or periodic TAU, etc.), at which time it returns to the connected state.

Note that for a short period of time immediately after the module is released from connected state by the network and enters idle state, it has a few extra short wake ups for clock calibration (shorter than a single PO). Figure 3-4 on page 28 shows an eDRX power consumption profile with a periodic TAU event. Notice that after the TAU, the eDRX 81.92s cycle is restored slowly by several iterations from 10s to 20s then to 40s before reaching the 81.92s wake. This behavior is an HL780x design feature and cannot be modified.

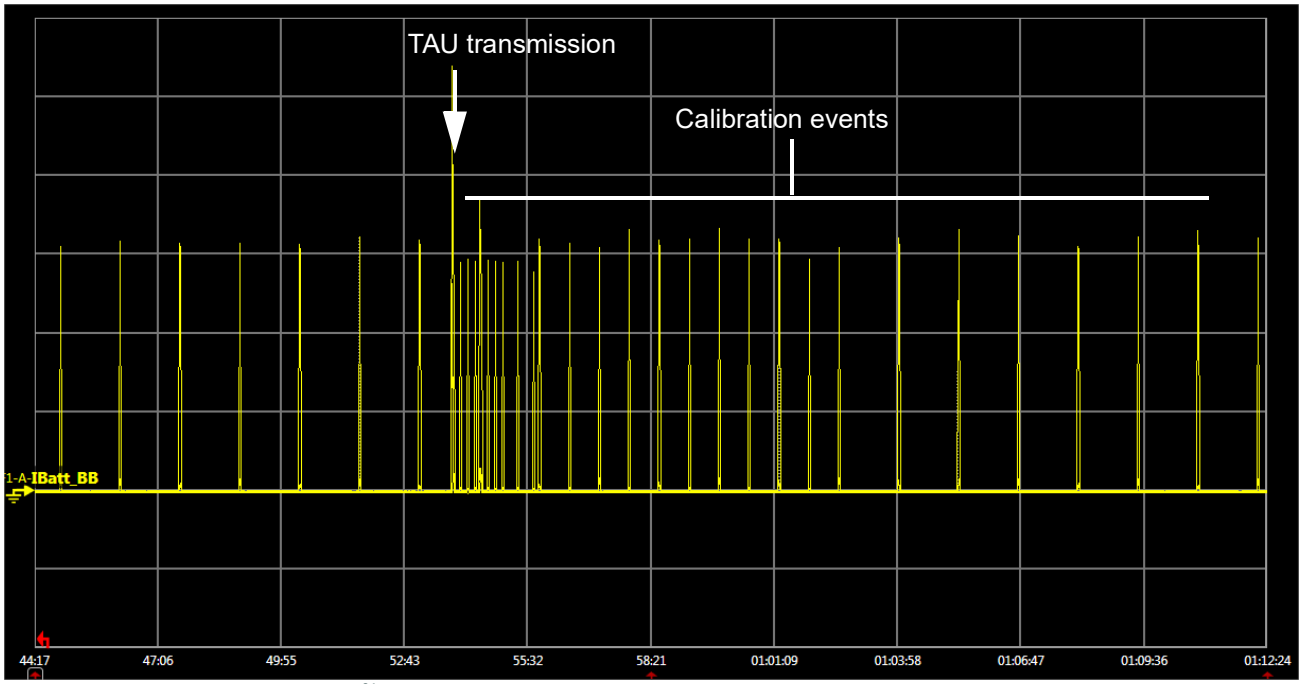


Figure 3-4: eDRX Power Consumption Profile Interruption

For a more detailed explanation of eDRX, refer to the HL78xx Low Power Modes Application Note.

Configuring eDRX

Table 3-4 describes available methods for configuring eDRX.

Table 3-4: eDRX-Related Commands

AT Command	Description
AT+CEDRXS AT+KEDRXCFG	Enable / disable eDRX and configure related settings
AT+CEDRXRDP	Display current eDRX settings

For example:

- Use `AT+CEDRXS` to configure the desired $T_{I\text{-}eDRX}$ value.
- During the network attach or TAU process:
  - Module sends eDRX request with the settings (as specified in `AT+CEDRXS`) to the network.
  - Network response indicates if the module may use eDRX and the eDRX parameters that should be used. The network may adjust the eDRX parameters from those requested by the module.
- If eDRX is accepted by the network, the module only needs to monitor during the eDRX paging opportunities. The module may enter low power mode state between the eDRX paging opportunities (depending on the module configuration).

Note that:

- eDRX parameters must be carefully selected to match the intended use case(s) for the module.

  Given that the module can only be paged at an eDRX paging opportunity:
  - Longer eDRX cycles will delay (increase the latency of) mobile terminated data reception.
  - Shorter eDRX cycles will reduce the latency but will also reduce the eDRX power savings.
  - Setting a cycle longer than 81.92s may not improve power saving significantly, since the module will wake every 81.92s to do a clock calibration.

  The duration of the eDRX cycle should be appropriately selected for the specific use case.
- Network-side store and forward is supported — Packets will be stored until the module's next eDRX paging opportunity or, if the network has a storage time limit, until that limit is reached.

3.3.2.2 Concurrent PSM and eDRX

eDRX may be performed during the Active Timer (T3324) window of PSM.

For example, if PSM and eDRX are configured with the following settings:

- PSM:
  - T3412 (PSM Timer) — 86400s (24 hours)
  - T3324 (Active Timer) — 327.68s (~5.5 minutes)
- eDRX:
  - eDRX cycle time — 81.92s

Assuming the network does not attempt to contact the module after the module leaves the connected state and enters PSM idle state, the module will stay in the idle state for 327.68 seconds (the Active Timer).

While in the idle state, the module will be in eDRX power saving mode for 4 cycles of 81.92 seconds each, and then go to PSM dormant state for ~23h55m until the T3412 timer expires. At that point the module wakes, sends a periodic TAU, and then the PSM process repeats.

3.4 HL780x Low Power Modes

In addition to the 3GPP power saving features (Power Saving Mode (PSM) and Extended DRX (eDRX)), the HL780x supports the low power modes in Table 3-5.

Table 3-5: Low Power Modes

Power Mode	Possible Modem State	Impact on Module	Hardware Wake-Up Signal Sources
Sleep	Stack OFF, DRX, eDRX, PSM, No service	▪ 26 MHz system clock is OFF ▪ Application processor is idle ▪ Modem is out-of-coverage, sleeping, or off ▪ I/Os are retained	WAKEUP UART1_DTR[a] RTC alarm event
Lite Hibernate	Stack OFF, eDRX, PSM, No service	▪ 26 MHz system clock is OFF ▪ Application processor is OFF ▪ Modem is out-of-coverage, sleeping, or off ▪ Flash memory and most RAM is off (some retention memory remains on) ▪ I/Os are retained	WAKEUP UART1_DTR[a] RTC timeout interrupt
Hibernate	Stack OFF, eDRX, PSM, No service	▪ 26 MHz system clock is OFF ▪ Application processor is OFF ▪ Modem is OFF ▪ Flash memory and most RAM is off (some retention memory may remain on, PSM/eDRX-dependent) ▪ I/Os are not retained (e.g. in an undefined state)	WAKEUP RTC timeout interrupt
OFF	Stack OFF	▪ 26 MHz system clock is OFF & RTC clock is OFF ▪ Application processor is OFF ▪ Modem is OFF ▪ Flash memory and RAM off ▪ I/Os are not retained (e.g. in an undefined state)	WAKEUP

a. Only if configured with +KSLEEP <mngt> parameter set to 0

An end product uses the `AT+KSLEEP` command to specify the preferred lowest power mode. Then when the module sleeps, its power management algorithm determines the appropriate mode based on the module's current operating requirements.

Note: When a module that is configured for PSM enters Hibernate mode, its non-persistent configurations are lost (just like when it power cycles). Refer to the HL78xx AT Commands Interface Guide to identify commands that manage persistent configurations.

Warning: *If USB_VBUS is powered and the USB interface is enabled, it will not be possible to enter Lite Hibernate or Hibernate mode.*

For additional low power mode details (including the relationship between 3GPP power saving features and HL780x power modes), refer to the HL78xx Low Power Modes Application Note. For band selection details (which impact power consumption), refer to the HL78xx Customization Guide Application Note.

Current Consumption

This section describes the HL780x module's current consumption under various power states/modes.

- Low Power Current Consumption Modes — Table 3-6 to Table 3-9
- Connected Mode — Table 3-10 to Table 3-14

Important: *The module's current consumption will depend on the actual operating/environmental conditions of the customer platform. The current consumption measurements presented in this section (Table 3-6 to Table 3-14) are typical values obtained under the following test conditions:*

- *Nominal supply voltage — 3.7V, TX power — 0 dBm*
- *Nominal ambient temperature — 25 °C*
- *PSM connect type (call box equipment setting) — test mode*
- *eDRX test conditions:*
  - *Cat-M1 eDRX paging cycle — 1.28 sec*
  - *Cat-NB eDRX paging cycle — 2.56 sec*
- *Conducted 50Ω load on RF port(s)*
- *External UICC/USIM that can be activated*

- *In addition, the following conditions apply to Hibernate and OFF mode measurements:*
  - *VGPIO is OFF*
  - *Customer platform ensures module I/Os are **not** driven > 0.2V*
  - *External UICC/USIM that is pre-configured to allow the module to automatically disable the USIM power.*
    (See ▪ HL78xx Low Power Modes Application Note Reference: 2174229 for details.)
  - *WAKEUP signal Low*

For detailed low power current consumption information, refer to the HL78xx Customization Guide Application Note.

Note: To be able to enter PSM mode when the module's lowest attainable power state is Lite Hibernate or Hibernate (i.e., +KSLEEP <level> is 1 or 2) and LwM2M is enabled (AutoConnect is enabled by default), the host must not de-assert the WAKEUP pin until it receives a CEREG:4 unsolicited result code.

Table 3-6: HL7800 / HL7800-M LPM Current Consumption — Cat-M1[a]

Modem Radio State	Lowest Power Mode	Details	Typ	Unit
OFF	OFF	▪ Module is switched off by AT command (+CPWROFF) ▪ Power supplies (VBAT_BB, VBAT_RF) are connected	1.8	µA
PSM		TAU — Occurrence is network dependent	63	µAh
	Hibernate	Floor current during PSM dormant	1.8	µA
	Lite Hibernate		30[b]	µA
	Hibernate Cycle[c]	▪ T3412 = 24h ▪ T3324 = 20s	9[d]	µA
	Lite Hibernate Cycle[c]		35[d]	µA
	Hibernate Cycle[c]	▪ T3412 = 1h ▪ T3324 = 20s	107[d]	µA
	Lite Hibernate Cycle[c]		97[d]	µA
eDRX[e]		Calibration — Applies to eDRX 81.92s and longer	9	µAh
	Hibernate	Floor current during eDRX	26[b]	µA
	Lite Hibernate		28[b]	µA
	Hibernate Cycle[c]	▪ eDRX cycle ($T_{I\text{-}eDRX}$) = 81.92s ▪ PTW and DRX = 1.28s	40[f]	µA
	Lite Hibernate Cycle[c]		41[f]	µA
	Hibernate Cycle[c]	▪ eDRX cycle ($T_{I\text{-}eDRX}$) = 20.48s ▪ PTW and DRX = 1.28s	88[f]	µA
	Lite Hibernate Cycle[c]		92[f]	µA
DRX	Sleep	1.28s	3.2	mA
	Hibernate		2.0	mA
	Sleep	2.56s	2.4	mA
	Hibernate		1.2	mA
	Running	DRX independent, +KSLEEP=2 or Wake active	40	mA

a. Values measured under following conditions:
   ▪ Good channel conditions (SINR > 5 dB)
   ▪ Static scenario
b. The floor current range of PSM lite hibernate, eDRX lite hibernate and eDRX hibernate mode is from 15µA to 50µA based on chip-set variation distribution.
c. Cycle (Lite Hibernate or Hibernate) includes boot, cell acquisition, network attach, wait for timer expiry, and back to Sleep.
d. Values are floor current and T3324-dependent.
e. See 3.3.2 Extended DRX (eDRX) for details.
f. Values are floor current, PTW, and DRX-dependent.

Table 3-7: HL7800 / HL7800-M LPM Current Consumption — Cat-NB1[a]

Modem Radio State	Lowest Power Mode	Details	Typ	Unit
OFF	OFF	Module is switched off by AT command and VBATs are connected	1.8	µA
PSM		TAU — Occurrence is network dependent	78	µAh
	Hibernate	Floor current during PSM dormant	1.8	µA
	Lite Hibernate		30[b]	µA
	Hibernate Cycle[c]	▪ T3412 = 24h ▪ T3324 = 20s	10[d]	µA
	Lite Hibernate Cycle[c]		40[d]	µA
	Hibernate Cycle[c]	▪ T3412 = 1h ▪ T3324 = 20s	133[d]	µA
	Lite Hibernate Cycle[c]		132[d]	µA
eDRX[e]		Calibration — Applies to eDRX 81.92s and longer	13	µAh
	Hibernate	Floor current during eDRX	22[b]	µA
	Lite Hibernate		27[b]	µA
	Hibernate Cycle[c]	▪ eDRX cycle ($T_{I\text{-}eDRX}$) = 81.92s ▪ PTW and DRX = 1.28s	60[f]	µA
	Lite Hibernate Cycle[c]		67[f]	µA
	Hibernate Cycle[c]	▪ eDRX cycle ($T_{I\text{-}eDRX}$) = 20.48s ▪ PTW and DRX = 1.28s	170[f]	µA
	Lite Hibernate Cycle[c]		175[f]	µA
DRX	Sleep	1.28s	3.5	mA
	Hibernate		2.6	mA
	Sleep	2.56s	3.8	mA
	Hibernate		1.4	mA
	Sleep	10.24s	2.1	mA
	Hibernate		0.6	mA
	Running	DRX independent, +KSLEEP=2 or Wake active	45	mA

a. Values measured under following conditions:
   ▪ Good channel conditions (SINR > 5 dB) (TBC)
   ▪ Static scenario
b. The floor current range of PSM lite hibernate, eDRX lite hibernate and eDRX hibernate mode is from 15µA to 50µA based on chip-set variation distribution.
c. Cycle (Lite Hibernate or Hibernate) includes boot, cell acquisition, network attach, wait for timer expiry, and back to Sleep.
d. Values are floor current and T3324-dependent.
e. See 3.3.2 Extended DRX (eDRX) for details.
f. Values are floor current, PTW, and DRX-dependent

Table 3-8: HL7802 LPM Current Consumption — Cat-M1[a]

Modem Radio State	Lowest Power Mode	Details	Typ	Unit
OFF	OFF	Module is switched off by AT command. Power supplies (VBAT_BB, VBAT_RF) are connected.	1.8	µA
PSM		TAU — Occurrence is network dependent	65	µAh
	Hibernate	Floor current during PSM dormant	1.8	µA
	Lite Hibernate		30[b]	µA
	Hibernate Cycle[c]	▪ T3412 = 24h ▪ T3324 = 20s	9[d]	µA
	Lite Hibernate Cycle[c]		35[d]	µA
	Hibernate Cycle[c]	▪ T3412 = 1h ▪ T3324 = 20s	122[d]	µA
	Lite Hibernate Cycle[c]		92[d]	µA
eDRX[e]		Calibration — Applies to eDRX 81.92s and longer	12	µAh
	Hibernate	Floor current during eDRX	26[b]	µA
	Lite Hibernate		28[b]	µA
	Hibernate Cycle[c]	▪ eDRX cycle ($T_{I\text{-}eDRX}$) = 81.92s ▪ PTW and DRX = 1.28s	40[f]	µA
	Lite Hibernate Cycle[c]		41[f]	µA
	Hibernate Cycle[c]	▪ eDRX cycle ($T_{I\text{-}eDRX}$) = 20.48s ▪ PTW and DRX = 1.28s	92[f]	µA
	Lite Hibernate Cycle[c]		93[f]	µA
DRX	Sleep	1.28s	3.4	mA
	Hibernate		2.2	mA
	Sleep	2.56s	2.8	mA
	Hibernate		1.3	mA
	Running	DRX independent, +KSLEEP=2 or Wake active	40	mA

a. Values measured under following conditions:
   ▪ Good channel conditions (SINR > 5 dB)
   ▪ Static scenario
b. The floor current range of PSM lite hibernate, eDRX lite hibernate and eDRX hibernate mode is from 15µA to 50µA based on chip-set variation distribution.
c. Cycle (Lite Hibernate or Hibernate) includes boot, cell acquisition, network attach, wait for timer expiry, and back to Sleep.
d. Values are floor current and T3324-dependent.
e. See 3.3.2 Extended DRX (eDRX) for details.
f. Values are floor current, PTW, and DRX-dependent

Table 3-9: HL7802 LPM Current Consumption — Cat-NB1[a]

Modem Radio State	Lowest Power Mode	Details	Typ	Unit
OFF	OFF	Module is switched off by AT command and VBATs are connected	1.8	µA
PSM		TAU — Occurrence is network dependent	75	µAh
	Hibernate	Floor current during PSM dormant	1.8	µA
	Lite Hibernate		30[b]	µA
	Hibernate Cycle[c]	▪ T3412 = 24h ▪ T3324 = 20s	10[d]	µA
	Lite Hibernate Cycle[c]		40[d]	µA
	Hibernate Cycle[c]	▪ T3412 = 1h ▪ T3324 = 20s	115[d]	µA
	Lite Hibernate Cycle[c]		113[d]	µA
eDRX[e]		Calibration — Applies to eDRX 81.92s and longer	13	µAh
	Hibernate	Floor current during eDRX	22[b]	µA
	Lite Hibernate		27[b]	µA
	Hibernate Cycle[c]	▪ eDRX cycle ($T_{I\text{-}eDRX}$) = 81.92s ▪ PTW and DRX = 1.28s	60[f]	µA
	Lite Hibernate Cycle[c]		67[f]	µA
	Hibernate Cycle[c]	▪ eDRX cycle ($T_{I\text{-}eDRX}$) = 20.48s ▪ PTW and DRX = 1.28s	170[f]	µA
	Lite Hibernate Cycle[c]		175[f]	µA
DRX	Sleep	1.28s	4.0	mA
	Hibernate		2.8	mA
	Sleep	2.56s	3.1	mA
	Hibernate		1.5	mA
	Sleep	10.24s	2.4	mA
	Hibernate		0.7	mA
	Running	DRX independent, +KSLEEP=2 or Wake active	45	mA

a. Values measured under following conditions:
   ▪ Good channel conditions (SINR > 5 dB) (TBC)
   ▪ Static scenario
b. The floor current range of PSM lite hibernate, eDRX lite hibernate and eDRX hibernate mode is from 15µA to 50µA based on chip-set variation distribution.
c. Cycle (Lite Hibernate or Hibernate) includes boot, cell acquisition, network attach, wait for timer expiry, and back to Sleep.
d. Values are floor current and T3324-dependent.
e. See 3.3.2 Extended DRX (eDRX) for details.
f. Values are floor current, PTW, and DRX-dependent

Table 3-10: HL7800 / HL7800-M Current Consumption — LTE Cat-M1 Connected Mode[a]

Parameter	Band	Output Power	Avg. Current (Typical Values)[b]
LTE Cat-M1 ▪ Modem State: Connected ▪ 4RB DL at MCS 14 1RB_UL at MCS 15 ▪ Maximum 3 UL sub-frames and 3 DL sub-frames every 10 ms ▪ Transferring UDP payload data rates: concurrent 280 kbps DL + 45 kbps UL	1, 2, 3, 4, 5, 8, 12, 13, 18, 19, 20, 25, 26, 27, 28, 66	23 dBm	185–225 mA
		0 dBm	120–135 mA

a. Subject to change
b. Ranges reflect variations between band / channel combinations

Table 3-11: HL7800 Current Consumption — LTE NB-1 Connected Mode[a]

Parameter	Band	Output Power	Avg. Current (Typical Values)
NB1 DL peak throughput (27.2kbps) 1 NPDCCH, 4 Guard, 3 NPDSCH, 12 Guard, 2 NPUSCH, 3 Guard	1, 2, 3, 4, 5, 8, 12, 13, 17, 18, 19, 20, 25, 26, 28, 66	23 dBm	105 mA
		0 dBm	100 mA
NB1 UL peak throughput (62.5kbps) 1 NPDCCH, 8 Guard, 4 NPUSCH, 3 Guard		23 dBm	165 mA
		0 dBm	130 mA

a. Subject to change

Table 3-12: HL7802 Current Consumption — LTE Cat-M1 Connected Mode[a]

Parameter	Band	Output Power	Avg. Current (Typical Values)[b]
LTE Cat-M1 ▪ Modem State: Connected ▪ 4RB DL at MCS 14 1RB_UL at MCS 15 ▪ Maximum 3 UL sub-frames and 3 DL sub-frames every 10 ms ▪ Transferring UDP payload data rates: concurrent 280 kbps DL + 45 kbps UL	1, 2, 3, 4, 5, 8, 12, 13, 18, 19, 20, 25, 26, 27, 28, 66	23 dBm	200–240 mA
		0 dBm	135–150 mA

a. Subject to change
b. Ranges reflect variations between band / channel combinations

Table 3-13: HL7802 Current Consumption — LTE NB-1 Connected Mode[a]

Parameter	Band	Output Power	Avg. Current (Typical Values)
NB1 DL peak throughput (27.2kbps) 1 NPDCCH, 4 Guard, 3 NPDSCH, 12 Guard, 2 NPUSCH, 3 Guard	1, 2, 3, 4, 5, 8, 12, 13, 17, 18, 19, 20, 25, 26, 28, 66	23 dBm	105 mA
		0 dBm	100 mA
NB1 UL peak throughput (62.5kbps) 1 NPDCCH, 8 Guard, 4 NPUSCH, 3 Guard		23 dBm	165 mA
		0 dBm	130 mA

a. Subject to change

4: Detailed Interface Specifications

This chapter describes the interfaces supported by the HL780x and provides specific voltage, timing, and circuit recommendations for those interfaces, as appropriate.

4.1 VGPIO

The VGPIO (GPIO voltage output) 1.8 V supply state is:
- ON (available) — Voltage output is high when module is in Active, Sleep, or Lite Hibernate mode
- OFF (not available) — Voltage output is low when module is in OFF, Reset, or Hibernate mode

VGPIO can be used to:
- Pull-up signals such as I/Os. For additional details, see I/O Behavior in Hibernate Mode.
- Supply LED drivers
- Indicate the module power state
- Control buffering of module I/O (required in Hibernate)

Table 4-1 and Table 4-2 describe the VGPIO supply.

Table 4-1: VGPIO Pin Description

Pad #	Signal Name	I/O[a]	Description
C45	VGPIO	PO	GPIO voltage supply

a. Signal direction with respect to the module

Refer to the following table for the electrical characteristics of the VGPIO supply.

Table 4-2: VGPIO Electrical Characteristics

Parameter		Min	Typ	Max	Unit	Remarks
Voltage level		1.75	1.8	1.85	V	Applies to Active, Sleep, and Lite Hibernate modes
Current capability	Active, Sleep	–	–	25	mA	Total current supplied by VGPIO should not exceed 25 mA.
	Lite Hibernate	–	–	1	mA	
Output capacitance		–	–	1	µF	External decoupling capacitance should not exceed 1 µF.

4.1.1 I/O Behavior in Hibernate Mode

The following behaviors apply, only in Hibernate mode, to I/Os that are referenced to VGPIO (i.e. UART, GPIO, Clock, UIM1, Indication, and ADC signal groups — see Table 2-2); they do not apply in Lite Hibernate or Sleep modes.

- VGPIO is OFF (voltage output is low)

Note: The host platform should isolate these signals during module Hibernate mode to prevent back-powering the module. For details, see Hibernate — Isolation Requirements.

- No I/O should be biased as no internal source exists. The maximum allowed voltage is ±0.2V at any I/O.
- All I/Os that are referenced to VGPIO will be in an undefined state.

The host should ignore all activity on these signals until the module has initialized and reached AT-READY state (i.e. when UART1_CTS transitions from high to low (and stays low) and VGPIO is high). For timing details, see Unmanaged POWER_ON_N (Default) and Wakeup from Low Power Modes.

4.2 USIM Interface

The HL780x implements a USIM interface that can be used to control either:

- the module's eSIM (internal, embedded SIM)

  or
- an external 1.8V USIM (UIM1); 3V USIM is not supported

To associate USIM1 with the eSIM or external USIM, use the `AT+KSIMSEL` command. For details, refer to the HL78xx AT Commands Interface Guide.

4.2.1 eSIM Interface

eSIM is an internal interface supporting Sierra Smart Connectivity. For details about using the HL780x's eSIM with Sierra Smart Connectivity, refer to the Sierra Wireless Ready-to-Connect Module Integration Guide. For additional information on Sierra Smart Connectivity, explore www.semtech.com or contact Semtech.

4.2.2 External UIM1 Interface

The USIM1 interface is fully compliant with GSM 11.11 recommendations concerning USIM functions.

Table 4-3 describes the USIM1 interface.

Table 4-3: UIM1 Pin Description

Pad #	Signal Name	I/O[a]	Description	I/O Type
C26	UIM1_VCC	PO	USIM1 Power supply	1.8V (VGPIO)
C27	UIM1_CLK	O	USIM1 Clock	1.8V (VGPIO)
C28	UIM1_DATA	I/O	USIM1 Data	1.8V (VGPIO)
C29	UIM1_RESET	O	USIM1 Reset	1.8V (VGPIO)
C64	UIM1_DET[b]	I	USIM1 Detection	1.8V (VGPIO)

a. Signal direction with respect to the module
b. Buffer is required if UIM_DET1 is powered from host; not required if powered from VGPIO. UIM1_DET can be used as GPIO3 if external SIM is not required.

Note: UIM1_VCC max output current is 50 mA in Active and Sleep modes, 1 mA in Lite Hibernate, and Off in Hibernate. For UIM1 electrical interface details, see UIM1.

4.2.3 UIM1_DET

UIM1_DET is used to detect the insertion or removal of a USIM in the USIM socket connected to the main USIM interface (UIM1).

When a USIM is:
- Inserted — UIM1_DET is HIGH.
- Removed — UIM1_DET is LOW.

Note: In Hibernate mode, UIM1_DET is in an undefined state.

To enable or disable the USIM detect feature, use the `AT+KSIMDET` command. For details, refer to the HL78xx AT Commands Interface Guide.

4.3 USB Interface

The HL780x module provides a full speed USB 2.0 interface that conforms to the Universal Serial Bus Specification, Revision 2.0.

Table 4-4 and Table 4-5 describe the USB interface.

Table 4-4: USB Pin Description

Pad #	Signal Name	I/O[a]	Description
C12	USB_D-	I/O	USB Data Negative
C13	USB_D+	I/O	USB Data Positive
C16	USB_VBUS	PI	USB VBUS

a. Signal direction with respect to the module

Table 4-5: USB Electrical Characteristics

Parameter	Min	Typ	Max	Unit
Voltage at pins USB_D+ / USB_D-	3.15	3.3	3.45	V
USB_VBUS	4.75	5.0	5.25	V

Important: *For USB operation, USB_VBUS is a mandatory connection. The host must ensure USB_VBUS is provided before establishing USB communication.*
When USB operation is enabled, the lowest power mode supported is Active — the module cannot enter Low Power state.
When USB operation is disabled, the lowest power mode supported is Hibernate.

For USB enumeration timing, refer to Unmanaged POWER_ON_N (Default) and Wakeup from OFF Mode.

Simultaneous UART and USB is supported by default, but can be affected by the +KUSBCOMP command. For details, refer to the HL78xx AT Commands Interface Guide.

4.4 General Purpose Input/Output (GPIO)

The HL780x provides several GPIOs, some of which are multiplexed with other signals, as described in Table 4-6. For electrical specifications, see Table 3-3.

Table 4-6: GPIO Pin Descriptions

Pad #	Signal Name	Alternate Function	Default State[a]	I/O Type
C1	GPIO1	–	Input Pull-down	1.8V (VGPIO)
C10	GPIO2	Alternative default Ring Indicator (Active High Output)	Input Pull-down	1.8V (VGPIO)
C40	GPIO7	–	Input Pull-down	1.8V (VGPIO)
C41	GPIO8	VBAT_PA_EN (Output)	Input Pull-down	1.8V (VGPIO)
C46	GPIO6	Low power mode monitoring	Input Pull-down	1.8V (VGPIO)
C51	GPIO14	UART3_CTS (Output)	Input Pull-down	1.8V (VGPIO)
C52	GPIO10	UART3_TX (Input)	Input Pull-down	1.8V (VGPIO)
C53	GPIO11	UART3_RTS (Input)	Input Pull-down	1.8V (VGPIO)
C54	GPIO15	UART3_RX (Output)	Input Pull-down	1.8V (VGPIO)
C64	GPIO3	UIM1_DET (Input)	Input Pull-down	1.8V (VGPIO)
C65	GPIO4	–	Input Pull-down	1.8V (VGPIO)
C66	GPIO5	–	Input Pull-down	1.8V (VGPIO)

a. Default state is software-controlled when module has initialized and reached AT-READY state. Default state is configurable by customer using AT+KGIOCFG command. For details, refer to the HL78xx AT Commands Interface Guide .

Table 4-6 notes the default state for each signal.

By default, at power up, all GPIOs are configured as inputs. During power up, power down, reset and Hibernate, the signals are in an undefined state. Therefore, the host should ignore all activity on I/Os until the module has reached AT-READY state (i.e. when UART1_CTS transitions from high to low (and stays low) and VGPIO is high). For timing details, see Unmanaged POWER_ON_N (Default) and Wake Up Signal (WAKEUP).

4.5 Main Serial Link (UART1)

The HL780x implements the UART1 serial interface (up to 921.6 kbps, default rate of 115.2 kbps) for communication between the module and a PC or host processor. UART1 consists of a flexible, 8-wire asynchronous serial, 1.8V interface that complies with RS-232 interface. UART1 can also be used to upgrade the module firmware locally.

Simultaneous UART and USB is supported by default, but can be affected by the +KUSBCOMP command. For details, refer to the HL78xx AT Commands Interface Guide .

Note: The host platform may use UART1 as an 8-wire, 4-wire, or 2-wire interface as shown in Figure 4-1, Figure 4-2, and Figure 4-3.

Note that in Hibernate mode the host platform (MCU) interfaces can remain powered — it is important that the host interfaces do not back-power the module.

The UART1 interface is not active during Hibernate mode, so the host should ignore all activity on UART1 during Hibernate. If the module will enter Hibernate mode, Sierra Wireless recommends adding buffer circuits to ensure UART signals are not driven high (i.e. >0.2V).

Note that a buffer is not required in Lite Hibernate mode. For detailed information, refer to I/O Behavior in Hibernate Mode on page 38.

Table 4-7 describes the UART1 interface.

Table 4-7: UART1 Pin Description

Pad #	Signal Name[a]	Default State[b] [c]	Active	I/O Type	Description
C2	UART1_RI	Output	L	1.8V (VGPIO)	Ring Indicator Data reception, SMS, etc.
C3	UART1_RTS	Input with pull-down	L	1.8V (VGPIO)	Request To Send
C4	UART1_CTS	Output	L	1.8V (VGPIO)	Clear To Send[d] The module is ready to receive AT commands.
C5	UART1_TX	Input with pull-up	–	1.8V (VGPIO)	Transmit data
C6	UART1_RX	Output	–	1.8V (VGPIO)	Receive data
C7	UART1_DTR	Input with pull-up	L	1.8V (VGPIO)	Data Terminal Ready[e]
C8	UART1_DCD	Output	L	1.8V (VGPIO)	Data Carrier Detect Signal data connection in progress
C9	UART1_DSR	Output	L	1.8V (VGPIO)	Data Set Ready Signal UART interface is ON

a. Signals are named with respect to the host device (i.e. DTE (Data Terminal Equipment) convention — PC view). For example, UART1_RX is the signal used by the host to receive data from the module.
b. Signal direction with respect to the module. For example, UART1_RX is an output from the module to the host.
c. Default state is software-controlled when module has initialized and reached AT-READY state.
d. Host can monitor UART1_CTS and VGPIO to determine when the module is ready to receive AT commands (AT-READY). The UART1 interface is not active during Hibernate mode, so the host should ignore all activity on UART1_CTS during Hibernate.
e. UART1_DTR has software-controlled pull-up (PU) (if enabled by using `AT+KSLEEP` with the <mngt> parameter set to 0), which is active only when module has initialized and reached AT-READY state. When the signal is low, the module wakes in all operational modes except Hibernate. When the signal is high, the module can enter sleep mode or lite hibernate mode but not hibernate mode.

Note: If possible, it is highly recommended to add 0Ω on every line on the host platform to help the debug process. This will force the UART signal layout to the top PCB layer and allow access to the signal on the resistors.

4.5.1 Ring Indicator (UART1_RI or Alternative)

UART1_RI is an active-low output signal that indicates incoming events (e.g. SMS, data reception, etc.).

The signal is available in all power modes except Hibernate mode. In Hibernate mode, the UART_RI signal is in an undefined state.

Therefore, if a customer platform requires a RI signal to wake its host processor on SMS or IP reception, an alternative signal must be used.

The `AT+KRIC` command can configure GPIO2 (by default) as an inverted RI signal (RI_inverse_gpio). (For details, refer to the HL78xx AT Commands Interface Guide and the HL78xx Low Power Modes Application Note).

Note: Because GPIO2 is in an undefined state while in (and exiting) Hibernate, use the following recommendations when GPIO2 is used as the RI signal:

- *If 4.3.4.0 or newer firmware is used, enable the internal PD on GPIO2 using `AT+KRIC` (default state is No Pull).*
- *If 4.3.3.0 or older firmware is used, a 10 kΩ PD is recommended on the host platform to maintain Low state. Alternatively, use Lite Hibernate mode.*

4.5.2 UART1_RTS/UART1_CTS

UART1_RTS (Request to Send) is an active-low input signal used for module flow control (in combination with UART1_CTS).

By default, the UART1_RTS signal state is software-controlled as pull-down, and the host platform must drive this signal. The signal can be configured as a pull-up using the `AT+KHWIOCFG` command (minimum firmware version 4.6.8)—for details, refer to ▪ HL78xx AT Commands Interface Guide Reference: 41111821

For detailed UART1 flow control information (including use of UART1_RTS and UART1_CTS), refer to the HL78xx Low Power Modes Application Note).

4.5.3 UART Application Examples

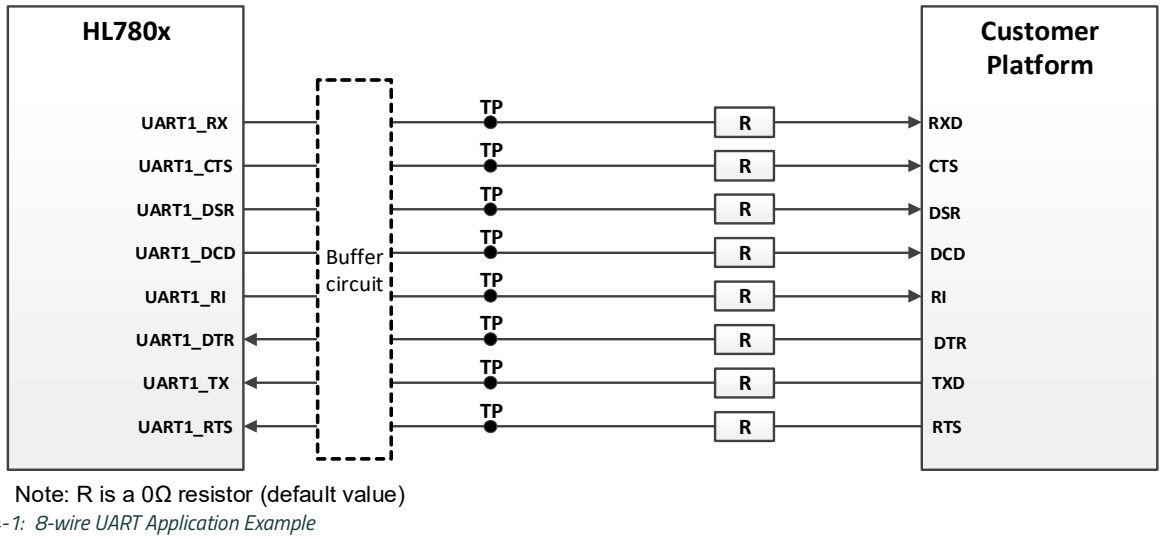


Figure 4-1: 8-wire UART Application Example

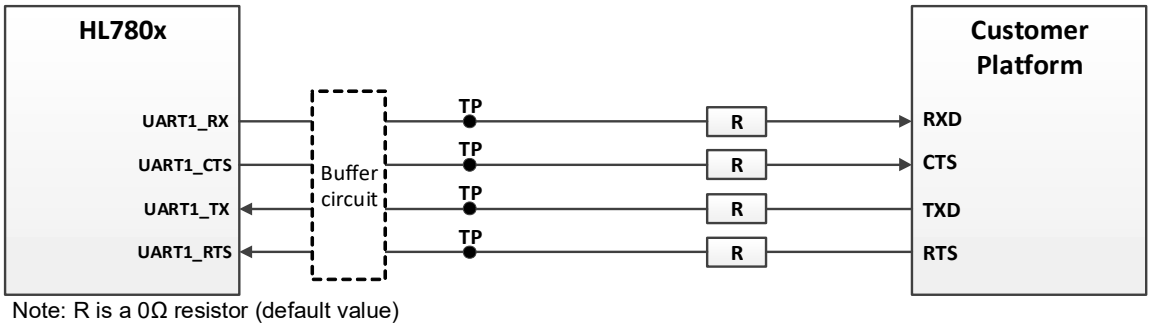


Figure 4-2: 4-wire UART Application Example

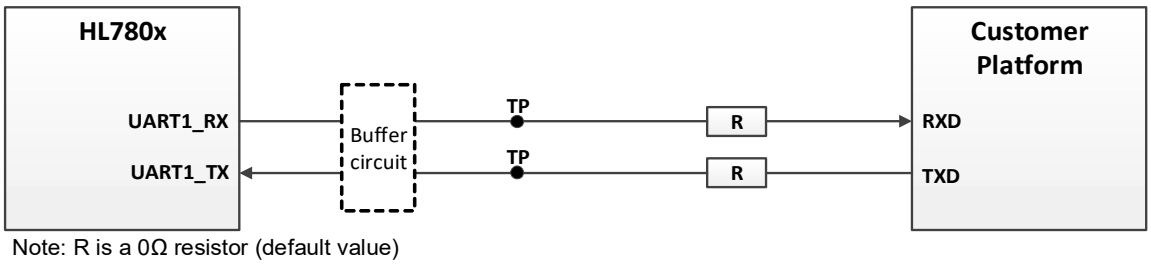


Figure 4-3: 2-wire UART Application Example

Note: All UART signals operate at 1.8V. A voltage level shifter is required when connecting to a 3V3 domain.

4.6 Power On Signal (POWER_ON_N)

The POWER_ON_N hardware control signal can be used by the host platform to turn the module on.

The signal is internally biased high by default. Bias voltage is dependent on the module mode — 1.3–1.4V in Active or Sleep mode, and 1.1–1.2V in Hibernate or Lite Hibernate mode.

The module has two possible operational modes — Host-managed and unmanaged:

- Unmanaged (default configuration) — The module starts regardless of the POWER_ON_N state. In this mode, the POWER_ON_N signal must be left open.

  Note: If RESET_IN_N is low, the module will not start until RESET_IN_N is released.

- Host-Managed — A low-level pulse must be provided by the host to switch the module ON. Use an open drain / open collector type circuit to drive the signal low (< 0.3V (Input Voltage-Low (V))).

Table 4-8 and Table 4-9 describe the POWER_ON_N signal.

Table 4-8: POWER_ON_N Pin Description

Pad #	Signal Name	I/O[a]	Description
C59	POWER_ON_N[b]	I	Powers the module ON

a. Signal direction with respect to the module
b. Signal provided by host. Does not need to be buffered, and can be directly connected to module using an open drain/collector type circuit.

Table 4-9: POWER_ON_N Electrical Characteristics

Parameter	Min	Typ	Max	Unit
Input Voltage-Low (v)	–	–	0.3	V

To ensure safe power on, the module VBAT (VBAT_BB / VBAT_RF) must be discharged below 0.3V before re-applying VBAT power.

4.6.1 Unmanaged POWER_ON_N (Default)

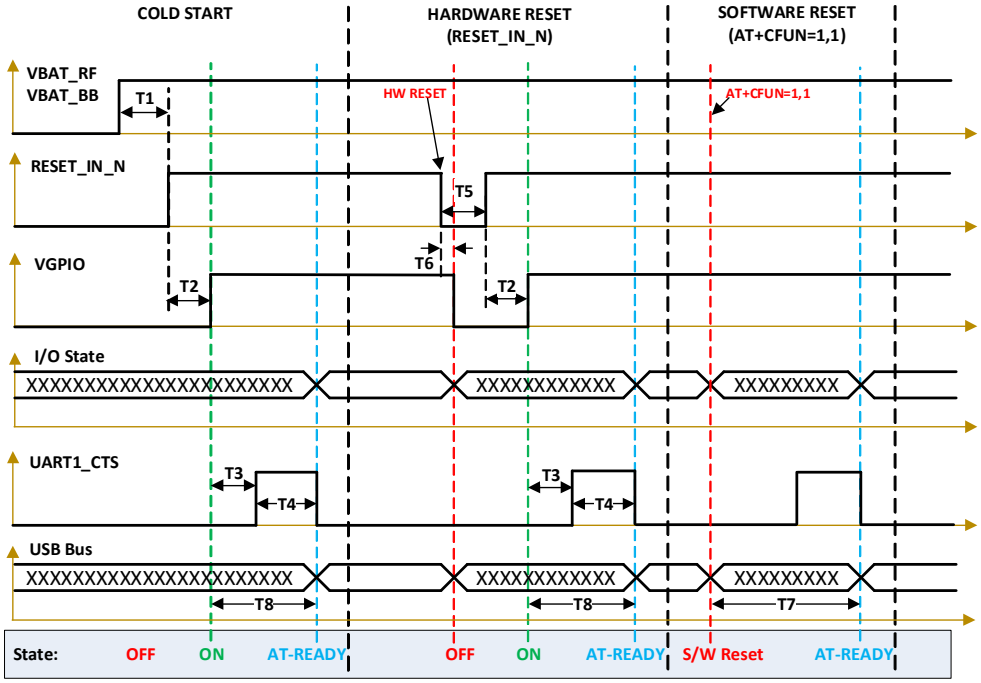


Figure 4-4: Power On and Reset Sequence (unmanaged POWER_ON_N)

Important: *At the completion of T4/T8/T7, the module is ready to receive AT commands ('AT-READY') via UART1 or USB.*

Table 4-10: POWER_ON_N Timing (unmanaged)[a]

Parameter	Min	Typ	Max[b]	Unit
T1: Delay between VBAT_BB and RESET_IN_N	–	–	1	ms
T2: Delay between RESET_IN_N and VGPIO	–	–	1	ms
T3: Delay between VGPIO and UART1_CTS	–	–	100	µs
T4: Delay	–	–	10	s
T5: HW RESET_IN_N assertion time	100	–	–	µs
T6: Off delay between VGPIO and RESET_IN_N	–	–	300	µs
T7: Delay between software reset and AT-READY (UART/USB)	–	–	10	s
T8: Delay between VGPIO and USB enumeration	–	–	$T3_{max} + T4_{max}$	s

a. Timing of first power cycle after FOTA/FW upgrade is not captured in this table.
b. Measurements taken with HL78xx Development Kit.

4.6.2 Host-Managed POWER_ON_N

To turn on the module, provide a pulse on POWER_ON_IN (pulse duration TBD). Use an open drain / open collector type circuit to drive the signal low (< 0.3V (Input Voltage-Low (V))),

Do not add a pull-up resistor on this signal as it is internally biased high by default.

4.7 Power Down, Off, and VBAT Removal

4.7.1 Software Power Off in Unmanaged Mode

To power down the module via software:

1. Initiate the power down process:
   a. Use the +cfun=0 command to stop SIM processes.
   b. Use the +CPWROFF command (For details, refer to the HL78xx AT Commands Reference Guide):

      ```
      AT+CPWROFF
      OK
      ```

   c. Immediately after receiving the "OK" response, set WAKEUP low.
2. Monitor VGPIO — When VGPIO is low (e.g. < 0.2 V), the module is in OFF mode.
   (Note — The module can be woken from OFF mode by setting WAKEUP high. For timing details, see Wake Up Signal (WAKEUP).)
3. It is now safe to remove power (VBAT_BB and VBAT_RF) from the module.

Note: While the module is in OFF mode, the host platform (MCU) interfaces can remain powered. To prevent these signals from back-powering the module, the host platform should make sure to isolate them — the signals should not be driven high (i.e. > 0.2 V). If the module is back-powered, the VGPIO low value will be higher (e.g. 0.8~1.1 V).

4.7.2 Emergency Power Removal

The Software Power Off in Unmanaged Mode procedure (which uses AT commands) should be used to safely power down the module.

However, if the module's UART and USB interfaces cannot be accessed, or are unresponsive (i.e. do not respond after an AT command is issued (see Command Timeout appendix in the HL78xx AT Commands Interface Guide), the following procedure can be used to power down the module, if necessary.

Important: *This procedure should be used with caution. If the module is interrupted while processing certain AT commands or performing a firmware upgrade, or the procedure is not followed correctly, the module may become unusable.*

1. Set RESET_IN_N low, and keep it asserted.
2. Monitor VGPIO — When VGPIO is low (e.g. < 0.2 V), the module is powered down.
3. Remove VBAT (both VBAT_BB and VBAT_RF) power.
4. Monitor VBAT — When VBAT is discharged below 0.3V, de-assert RESET_IN_N.

Note:

- *To power up the module, it is critical that VBAT be fully discharged (or below 0.3V) and that RESET_IN_N must be de-asserted. For details, refer to Unmanaged POWER_ON_N (Default).*
- *While the module is in OFF mode, the host platform (MCU) interfaces can remain powered. To prevent these signals from back-powering the module, the host platform should make sure to isolate them — the signals should not be driven high (i.e. > 0.2 V). If the module is back-powered, the VGPIO low value will be higher (e.g. 0.8~1.1 V).*

4.8 Reset Signal (RESET_IN_N)

The RESET_IN_N hardware control signal can be used to reset the module in any power state.

To reset the module, assert RESET_IN_N low for 100 µs (minimum) — this action immediately resets the module. For timing details, see Figure 4-4 (HARDWARE RESET segment).

Use an open drain / open collector type circuit to drive the signal low (< 0.3V (Input Voltage-Low (V))),

Do not add a pull-up resistor on this signal as it is internally biased high by default. The bias voltage depends on the module operating state — 1.3–1.4V in Active and Sleep modes, and 1.1–1.2V in Hibernate and Lite Hibernate modes.

Note: For power-sensitive applications, the module does not reach minimal power consumption when held in reset. Therefore, it is not recommended to hold the module in reset state for long periods.

Warning: *RESET_IN_N should only be used to reset the module if it is unresponsive to AT commands and a power cycle cannot be performed. If used inappropriately (e.g. to reset during a firmware upgrade), memory corruption can occur.*
As an alternative, Semtech recommends implementing a software reset using `AT+CFUN=1,1`. For details, refer to the HL78xx AT Commands Interface Guide.

Warning: *During a module reset:*

- *All I/Os will be in an undefined state.*
- *I/Os must not be driven high (over 0.2 V), otherwise the module may be damaged.*
- *RESET_IN_N must not be set low during a power cycle, otherwise the module will not boot.*
- *VBAT_BB must always be > 3.2V when reset is asserted.*

Table 4-11 and Table 4-12 describe the RESET_IN_N signal.

Table 4-11: RESET_IN_N Pin Description

Pad #	Signal Name	I/O[a]	Active	Description
C11	RESET_IN_N[b]	I	L	Reset signal

a. Signal direction with respect to the module
b. Signal provided by host. Does not need to be buffered, and can be directly connected to module using an open drain/collector type circuit.

Refer to the following table for the electrical characteristics of the RESET_IN_N interface.

Table 4-12: RESET_IN_N Electrical Characteristics

Parameter	Min	Typ	Max	Unit
Input Voltage-Low	–	–	0.3	V
Reset assertion time	0.1	1	–	ms

4.9 Analog to Digital Converter (ADC)

The HL780x provides two general purpose ADC signals (ADC0, ADC1). These converters are 12-bit resolution ADCs with voltage range of 0–1.8V.

Typical ADC use is for monitoring external signals. The `AT+KADC` command is used to read the ADC values. For details, refer to the HL78xx AT Commands Interface Guide.

Table 4-13 describes the ADC signals.

Table 4-13: ADC Pin Description

Pad #	Signal Name	I/O[a]	Description	I/O Type
C24	ADC1	AI	Analog to digital converter	1.8V (VGPIO)
C25	ADC0	AI	Analog to digital converter	1.8V (VGPIO)

a. Signal direction with respect to the module

4.10 Clock Interface

The HL780x supports two digital clock output signals.

These signals are disabled by default. To enable (or disable) these signals, use the `AT+KHWIOCFG` command. For details, refer to the HL78xx AT Commands Interface Guide.

Note: To reduce noise and radiated spurious emission (RSE), disable the clock signals if they are not being used.

Table 4-14 describes the clock signals.

Table 4-14: Clock Interface Pin Description

Pad #	Signal Name	I/O[a]	Voltage Supply Domain	Description
C22	26M_CLKOUT	O	1.8V (VGPIO)	26 MHz Digital Clock output
C23	32K_CLKOUT	O	1.8V (VGPIO)	32.786 kHz Digital Clock output

a. Signal direction with respect to the module

4.11 Debug Interfaces

The HL780x provides two 4-wire debug port interfaces (Diagnostic Interface, Modem Logs) that can be used with the AT interface for full debug capability.

Note: All UART signals operate at 1.8V. A voltage level shifter is required when connecting to a 3V3 domain.

UART interfaces are not active during Hibernate mode, so the host should ignore all activity on UART interfaces during Hibernate. If the module will enter Hibernate mode, Sierra Wireless recommends adding buffer circuits to ensure module I/Os are not driven high (i.e. >0.2V).

To enable debug interfaces, refer to the HL78xx AT Commands Interface Guide.

4.11.1 Diagnostic Interface

The Diagnostic interface is implemented over UART0. When the module begins to boot, UART0 is enabled at 115200 baud and writes an initial boot log.

Availability and behavior of UART0 after the initial boot log is written depends on the configured debug mode (using the AT command +SWITRACEMODE):

- Customer mode (`AT+SWITRACEMODE=CUSTOMER`) — UART0 is disabled after the initial boot log is written.
- Debug mode (`AT+SWITRACEMODE=LOG` or `AT+SWITRACEMODE=SFPLOG`) — UART0 remains enabled for logging. Unless configured differently using +SWITRACEMODE options, the default baud rate (921600) and default flow control (enabled) are used.
  With flow control enabled (4-wire logging), UART0_CTS is asserted. To receive logging data, the host must assert UART0_RTS, and then use UART0_RX/UART0_TX to receive/send data.

  With flow control disabled (2-wire logging), note that the host must be fast enough to capture all data streamed from the module so that log files are not corrupted.
- Boot mode for firmware upgrades (using SFT (Standalone File Tool)) — UART0 remains enabled for 2-wire communication (flow control is disabled by default; UART0_CTS is not asserted, and UART0_RTS is ignored).

  Note that Flow control may be enabled using `AT+KBOOTCFG=1`, but is not required for successful firmware upgrades. For SFT details, refer to the HL78xx Low Power Modes Application Note.

Table 4-15: Diagnostic Interface Pin Description

Pad #	Signal Name[a]	Default State[b,c]	Active	I/O Type	Description
C55	UART0_RX	Output	—	1.8V (VGPIO)	Debug Receive Data
C56	UART0_TX	Input	—	1.8V (VGPIO)	Debug Transmit Data
C57	UART0_CTS	Output	L	1.8V (VGPIO)	Debug Clear to Send
C58	UART0_RTS	Input	L	1.8V (VGPIO)	Debug Request to Send

a. Signals are named with respect to the host device (i.e. DTE (Data Terminal Equipment) convention — PC view). For example, UART0_RX is the signal used by the host to receive data from the module.
b. Signal direction with respect to the module. For example, UART0_RX is an output from the module to the host.
c. Default states are for the module in Debug mode with flow control enabled.
In Debug and Boot modes, with flow control disabled, UART0_CTS and UART0_RTS are disabled.
In Customer mode, all signals are disabled.

Note: It is highly recommended to provide access through Test Points to this interface (required for customer platform debugging).

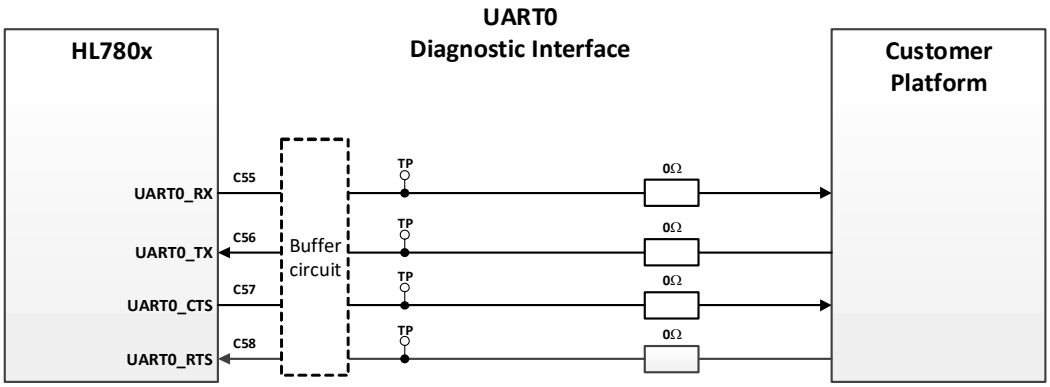


Figure 4-5: Diagnostic Interface connection example

4.11.2 Modem Logs Interface (MLI)

Table 4-16: Modem Logs Interface Pin Description

Pad #	Signal Name	I/O[a]	I/O Type	Description
C51	GPIO14	O	1.8V (VGPIO)	UART3_CTS[b]
C52	GPIO10	I	1.8V (VGPIO)	UART3_TX[b]
C53	GPIO11	I	1.8V (VGPIO)	UART3_RTS[b]
C54	GPIO15	O	1.8V (VGPIO)	UART3_RX[b]

a. Signal direction with respect to the module. For example, GPIO14 is an output from the module to the host.
b. Signals are named with respect to the host device (i.e. DTE (Data Terminal Equipment) convention — PC view). For example, UART3_RX is the signal used by the host to receive data from the module.

Note: To enable use of the UART3 interface for customer platform debugging, it is highly recommended to provide access through Test Points to these 4 GPIOs.

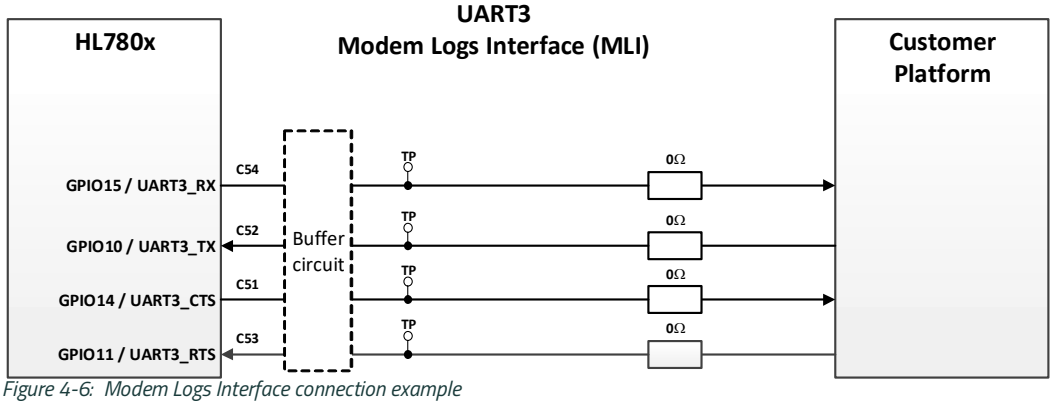


Figure 4-6: Modem Logs Interface connection example

4.12 Wake Up Signal (WAKEUP)

The WAKEUP hardware control signal is used to wake the module from low power modes (Sleep, Lite Hibernate, Hibernate, OFF) by driving the signal high to 1.8V.

The module will not enter or return to low power mode while the WAKEUP signal is high.

Table 4-17 and Table 4-18 describe the WAKEUP signal.

Table 4-17: WAKEUP Pin Description

Pad #	Signal Name	I/O[a]	I/O Type	Description
C44	WAKEUP[b]	I	1.8V	Wakes the module up from low power mode

a. Signal direction with respect to the module
b. Signal provided by host. Signal does not need to be buffered, and can be directly connected to the module.

Table 4-18: WAKEUP Electrical Characteristics

Parameter	Minimum	Typical	Maximum	Unit
V_{IL}	–	–	0.3	V
V_{IH}	1.2	–	–	V
Wakeup assertion time[a]	100	–	–	µs
Internal PD	–	100K	–	Ω

a. Assertion time — Time required to keep WAKEUP at high level to ensure module can wake up successfully.

4.12.1 Wakeup from Low Power Modes

This section describes the module's signal behaviors when waking from the low power modes defined in Table 3-5.

4.12.2 Wakeup from OFF Mode

Figure 4-7 and Table 4-19 describe signal behavior when WAKEUP is used to wake the module from OFF mode.

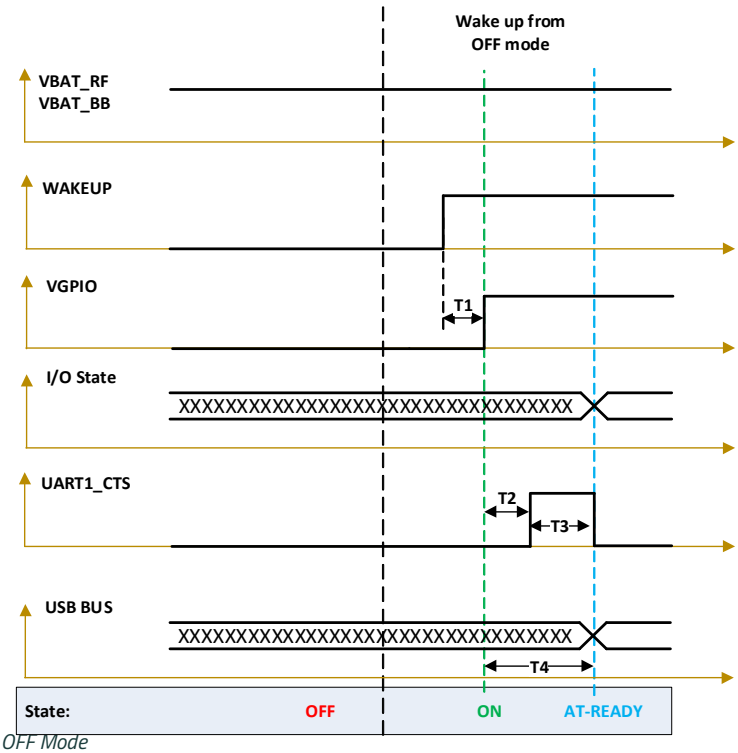


Figure 4-7: Wake up from OFF Mode

Table 4-19: WAKEUP Timing (from OFF Mode)

Parameter	Min	Typ	Max[a]	Unit
T1: Delay between WAKEUP and VGPIO	–	–	1	ms
T2: Delay between VGPIO and UART1_CTS	–	–	100	µs
T3: Delay	–	–	10	s
T4: Delay between VGPIO and USB enumeration	–	–	$T2_{max} + T3_{max}$	s

a. Measurements taken with the HL78xx Development Kit.

4.12.3 Wakeup from Lite Hibernate Mode

Figure 4-8 and Table 4-20 describe the module's signal behaviors when WAKEUP is used to wake the module from Lite Hibernate mode.

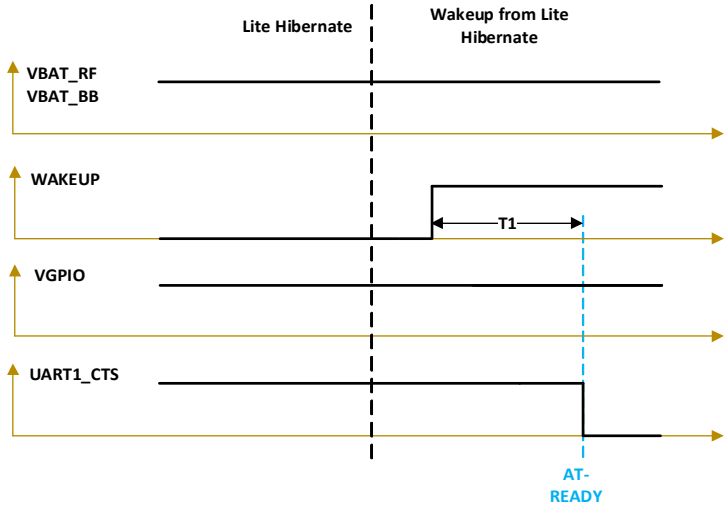


Figure 4-8: Wake up from Lite Hibernate Mode

Table 4-20: WAKEUP Timing (from Lite Hibernate Mode)

Parameter	Min	Typ	Max[a]	Unit
T1: Delay between WAKEUP and AT-READY	–	–	6	s

a. Measurements taken with HL78xx Development Kit

4.12.4 Wakeup from Hibernate Mode

Figure 4-9 and Table 4-21 describe the module's signal behaviors when WAKEUP is used to wake the module from Hibernate mode.

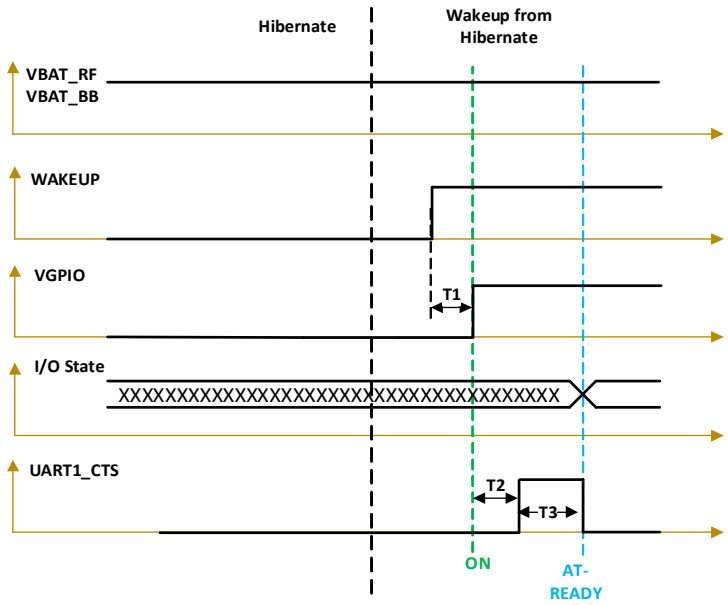


Figure 4-9: Wake up from Hibernate Mode

Table 4-21: WAKEUP Timing (from Hibernate Mode)

Parameter	Min	Typ	Max[a]	Unit
T1: Delay between WAKEUP and VGPIO	–	–	1	ms
T2: Delay between VGPIO and UART1_CTS high	–	–	15	ms
T3: UART1_CTS high to AT-READY	–	–	6	s

a. Measurements taken with HL78xx Development Kit

4.13 RF Interface

The RF interface of the HL780x provides a single RF antenna connection for the transmission/reception of RF signals.

Contact Semtech technical support for assistance in integrating the HL780x on applications with embedded antennas.

4.13.1 RF Antenna Connection

A 50Ω RF track (with maximum VSWR 1.1:1, and 0.5 dB loss) is recommended to connect the module's RF_MAIN to standard RF antenna connectors (e.g. SMA, U.FL, etc).

Table 4-22 describes the module's RF interface.

Table 4-22: RF Main Pin Description

Pad #	RF Signal	Impedance	VSWR Rx (max)	VSWR Tx (max)
C48	GND	–	–	–
C49	RF_MAIN	50Ω	2.5:1	2.5:1
C50	GND	–	–	–

4.13.2 LTE RF Interface

4.13.2.1 Maximum Output Power

The HL780x module's LTE maximum transmitter output power for all bands in normal operation conditions (25°C) is specified in Table 4-23.

Table 4-23: HL7800 / HL7800-M / HL7802 Conducted Tx Max Output Power Tolerances — LTE[a]

LTE Bands	Min	Typ	Max	Units	Notes
All bands	21.5[b]	23	24.5	dBm	Power class 3

a. Under normal operating conditions (25°C)
b. Additional power reduction is applied to the lowest and highest supported channels for each band — see Table 1-1 on page 10 footnote "[b]" for supported Tx channel ranges. (e.g. applies to B2 channels 18602 and 19198)

4.13.2.2 Rx Sensitivity

The module's LTE receiver sensitivity is specified in the following tables.

Table 4-24: HL780x Typical Conducted Cat-M1 RX Sensitivity[a]

LTE Band	Typical Reference Sensitivity Level @ 95% of Maximum Throughput		
	@ +25°C (dBm)	@ Class A (dBm)	3GPP Limit (dBm)[b]
B1	-104	-102.5	-102.3
B2	-104	-103	-100.3
B3	-105	-103.5	-99.3
B4	-104	-102.5	-102.3
B5	-105	-104	-100.8
B8	-105	-103	-99.8
B9	-105	-103.5	—[c]
B10	-104	-102.5	—[c]
B12	-105	-103.5	-99.3
B13	-105	-104	-99.3

Table 4-24: HL780x Typical Conducted Cat-M1 RX Sensitivity[a] (Continued)

LTE Band	Typical Reference Sensitivity Level @ 95% of Maximum Throughput		
	@ +25°C (dBm)	@ Class A (dBm)	3GPP Limit (dBm)[b]
B17	-105	-103.5	—[c]
B18	-105	-104	-100.3
B19	-105	-104	-102.3
B20	-105	-104	-99.8
B25	-105	-103	—[c]
B26	-105	-104.5	-100.3
B27	-105	-104.5	-100.8
B28	-105	-104	-100.8
B66	-104	-102.5	—[c]

a. Test conditions per 3GPP TS 36.521-1 v13: Bandwidth: 5MHz on Reference Measurement Channel
b. Displayed limits derived from 3GPP TS 36.521-1 V16.3.0, Table 7.3EA-2, adjusted by +0.7 dB for measurement uncertainty
c. Band not defined by 3GPP, therefore no associated limit

Table 4-25: HL780x Typical Conducted NB1 RX Sensitivity[a]

LTE Band	Typical Reference Sensitivity Level @ 95% of Maximum Throughput		
	@ +25°C (dBm)	@ Class A (dBm)	3GPP Limit (dBm)[b]
B1	-113	-111.5	-107.5
B2	-113.5	-112.1	-107.5
B3	-114	-112.5	-107.5
B4	-113	-111.6	-107.5
B5	-113.5	-112.3	-107.5
B8	-113	-111.8	-107.5
B9	N/A	N/A	N/A
B10	N/A	N/A	N/A
B12	-112.5	-111.2	-107.5
B13	-113	-111.8	-107.5
B17	-113	-111.7	-107.5
B18	-113.5	-112.2	-107.5
B19	-113.5	-112.2	-107.5
B20	-113	-111.7	-107.5
B25	-113	-111.7	-107.5

Table 4-25: HL780x Typical Conducted NB1 RX Sensitivity[a] (Continued)

LTE Band	Typical Reference Sensitivity Level @ 95% of Maximum Throughput		
	@ +25°C (dBm)	@ Class A (dBm)	3GPP Limit (dBm)[b]
B26	-113.8	-112.5	-107.5
B27	N/A	N/A	N/A
B28	-113	-111.7	-107.5
B66	-113	-111.5	-107.5

a. Test conditions per 3GPP TS 36.521-1 v13: on DL Reference Measurement Channel defined
b. Displayed limits derived from 3GPP TS 36.521-1 V16.3.0, Table 7.3F.1.3-1, adjusted by +0.7 dB for measurement uncertainty

4.13.3 2G RF Interface (HL7802 only)

The HL7802 module is a GPRS only device (no EGPRS support) supporting GSM multislot class 10 (4 DL/2UL max (5 slots)).

4.13.3.1 Tx Output Power

The module's 2G maximum transmitter output power is specified in Table 4-26.

Table 4-26: HL7802 Conducted Tx Max Output Power Tolerances — 2G[a,b]

RF Band	Min	Typ	Max	Units	Notes
GSM 850	31.5	32.5	33.5	dBm	GMSK mode (Class 4; 2 W, 33 dBm)
E-GSM 900	31.5	32.5	33.5	dBm	GMSK mode (Class 4; 2 W, 33 dBm)
DCS 1800	28.5	29.5	30.5	dBm	GMSK mode (Class 1; 1 W, 30 dBm)
PCS 1900	28.5	29.5	30.5	dBm	GMSK mode (Class 1; 1 W, 30 dBm)

a. Stated power tolerances satisfy 3GPP TS 51.010-1 requirements for normal (25°C) and Class A (extreme) conditions
b. Stated power tolerances for input voltage of 3.7V

4.13.3.2 Rx Sensitivity

The module's GPRS receiver sensitivity is specified in Table 4-27.

Table 4-27: Typical Conducted RX Sensitivity — GPRS Bands[a]

GPRS Band	Parameters	Typical Reference Sensitivity Level @ 95% of Maximum Throughput		
		@ +25°C (dBm)	@ Class A (dBm)	Standard Limit (dBm)
GSM 850	10% BLER; GMSK CS1	-110	-108	-102
E-GSM 900	10% BLER; GMSK CS1	-111	-108	-102
DCS 1800	10% BLER; GMSK CS1	-112	-108	-102
PCS 1900	10% BLER; GMSK CS1	-112	-108	-102

a. Stated sensitivity values satisfy 3GPP TS 51.010-1 requirements for normal (25°C) and Class A (extreme) conditions

4.14 TX Burst Indicator (TX_ON)

The HL780x provides the TX_ON signal for TX activity indication.

Note: This signal is currently available for LTE Cat-M1. Support for LTE Cat-NB1 (HL7800/HL7802) and 2G (HL7802) will be available in a future firmware release.

Table 4-28: TX_ON Pin Description

Pad #	Signal Name	I/O[a]	I/O Type	Description
C60	TX_ON	O	1.8V (VGPIO)	High during Tx activity

a. Signal direction with respect to the module

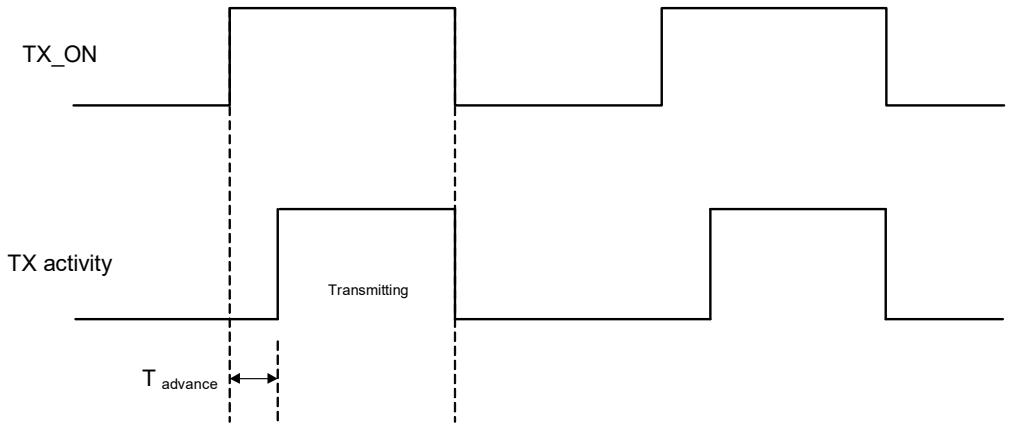


Figure 4-10: TX_ON State High during TX Activity

To enable/disable this feature, use the AT+KHWIOCFG command. For details, refer to the HL78xx AT Commands Interface Guide.

Table 4-29: TX_ON Characteristics

$T_{advance}$	30 µs

4.15 Tx/Rx Activity Indicator; External RF Voltage Control

The HL780x provides the VBAT_PA_EN signal for RF activity (Tx/Rx) indication.

Depending on customer requirements, it can be also be used to select the module VBAT_RF power source during RF activity, and support antenna switching.

To enable/disable this feature, use the AT+KHWIOCFG command. For details, refer to the HL78xx AT Commands Interface Guide.

Table 4-30, Figure 4-11 and Table 4-31 describe the VBAT_PA_EN signal.

Table 4-30: VBAT_PA_EN Pin Description

Pad #	Signal Name	I/O[a]	I/O Type	Description
C41	GPIO8	I/O	1.8V (VGPIO)	High during Tx/Rx activity
	VBAT_PA_EN	O		

a. Signal direction with respect to the module

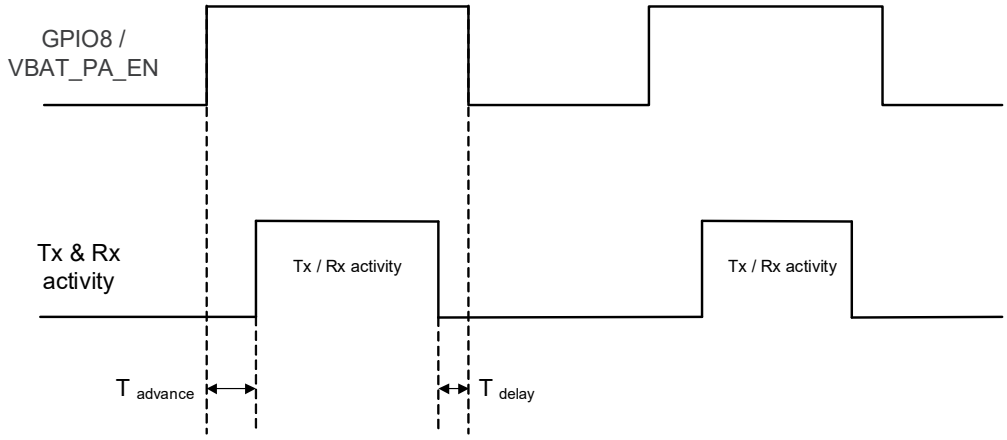


Figure 4-11: VBAT_PA_EN State during Tx/Rx Activity

Table 4-31: VBAT_PA_EN Characteristics (TBC)

Parameter	Min	Max
$T_{advance}$	0.4 ms	5 ms
T_{delay}	10 µs	20 µs

4.16 GNSS

The HL780x's GNSS implementation supports GPS L1 and GLONASS G1 operation.

Note: The GNSS receiver and LTE/GSM receiver share the same RF resources, therefore GNSS can only be used when the module is not actively connected on LTE/GSM. An example of a suitable implementation of GNSS in an end product would be the use of GNSS positioning for asset management applications where infrequent and no real-time position updates are required.

Table 4-32 describes the GNSS antenna specifications. Note that the HL780x does not support an active GPS/GNSS antenna.

Table 4-32: GNSS Antenna Specifications

Characteristics		Value	Unit
Frequency	GPS L1	1575.42 ± 20	MHz
	GLONASS G1	1589.0625–1605.375	MHz
RF Impedance (RF_GNSS pad)		50	Ω
VSWR max		2:1	–

4.16.1 GNSS Performance

Table 4-33 summarizes the HL780x module's GNSS performance characteristics.

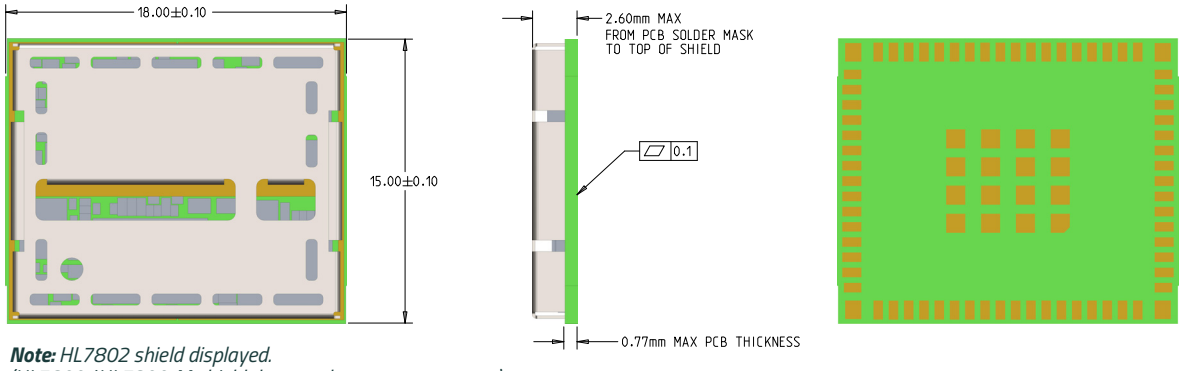
Table 4-33: GNSS Performance[a]

Parameters	Conditions	Typical Value
Sensitivity	Cold Start	-145.8 dBm
	Hot Start	-146.4 dBm (TBC)
	Tracking	-163.6 dBm
Time To First Fix (TTFF)	Cold start, Input power -130 dBm	39s
	Hot start, Input power -130 dBm	2.7s (TBC)
2D Position Error	Input power -130 dBm	1.29 m

a. Preliminary values

5: Mechanical Drawings

For tolerances, refer to Table 1-2 and Table 1-3.



Note: *HL7802 shield displayed.*
(HL7800/HL7800-M shield does not have center cutouts.)

Figure 5-1: Mechanical Drawing

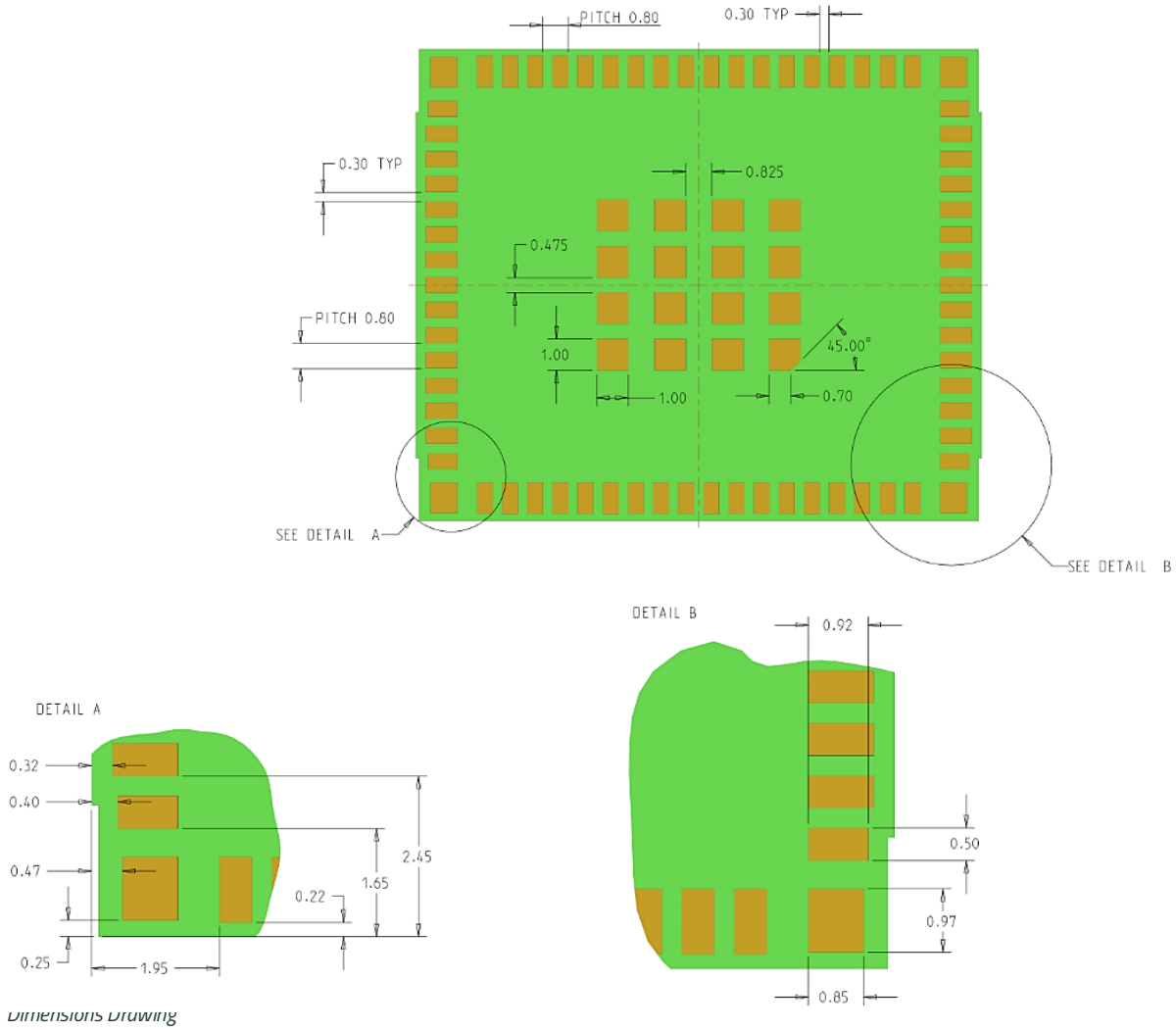


Figure 5-2: Dimensions Drawing

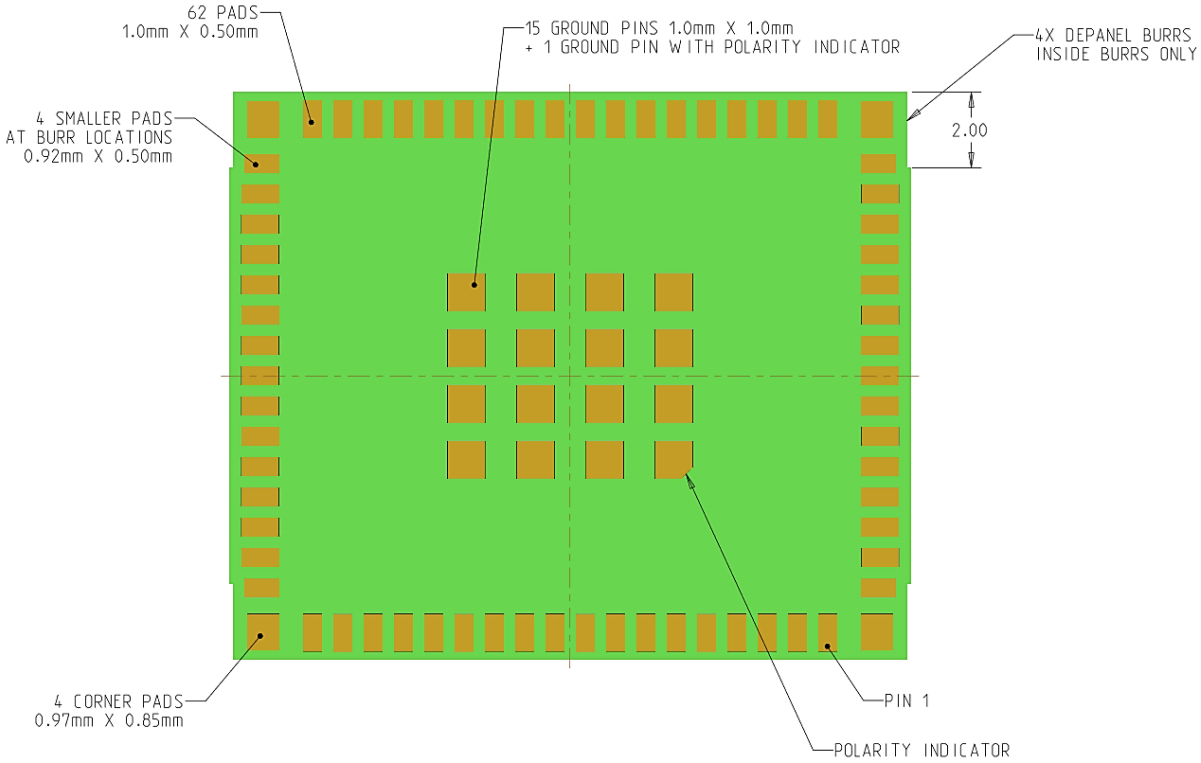


Figure 5-3: Footprint Drawing

6: Design Guidelines

6.1 Power Supply Design

When designing the power supply, make sure VBAT_BB/VBAT_RF meet the requirements listed in Table 3-2 — Semtech recommends adding a 30% design margin, if possible.

Careful attention should be paid to the following:

- Power supply design — A low-ripple, low-noise source such as LDO, battery, or switching power supply (SMPS) is recommended.
- (HL7802 GSM Tx) Capacity to deliver high current peaks in a short time
  - VBAT_BB/VBAT_RF must support peak currents with an acceptable voltage drop that guarantees the minimum required VBAT_BB/VBAT_RF value.
- VBAT_BB/VBAT_RF signal voltage must never exceed the maximum value, otherwise the module may be severely damaged.
  - If necessary, add a voltage limiter to the module's power supply lines to ensure VBAT will never receive a voltage surge over 4.35V. There are a few protection options from a basic linear regulator to a voltage limiter, as simple as a Zener diode.
- ESD protection is recommended on VBAT_BB/VBAT_RF supply rails — Semtech recommends Diodes Inc part number D8V0L1B2LP3-7.
- Both over-voltage protection and ESD protection devices will increase platform current consumption.
- All ground pins (C30, C32, C37, C39, C48, C50, CG1–CG4, G1–G16) must be connected to the same net.

6.2 UIM1

UIM1 can operate at clock rates up to 5 MHz.

Most UIM1 signal lines do not require a buffer during Hibernate, and can be directly connected to the UIM card or holder. A buffer is required for UIM_DET1 if powered from the host (not required if powered from VGPIO).

Decoupling capacitor(s) must be added to UIM1_VCC and UIM1_DET, as close as possible to the UIM card. Decoupling capacitors for UIM1_CLK, UIM1_RST, and UIM1_DATA are recommended to be added as placeholders for potential EMC issues.

The two resistors (RCLK and RDAT) should be added as placeholders to compensate for potential layout issues. Both can be populated to slew the UIM1 signals, if required.

The UIM1_DATA trace should be routed away from the UIM1_CLK trace.

Keep the distance between the module and the UIM holder as short as possible.

Semtech recommends using the following ESD protection on the UIM1 interface:

- INFINEON ESD112-B1-02EL E6327 — UIM1_CLK, UIM1_DATA, UIM1_RESET
- Diodes Inc D8V0L1B2LP3-7 — UIM1_VCC, UIM1_DET

Figure 6-1 illustrates the recommended implementation of a UIM interface.

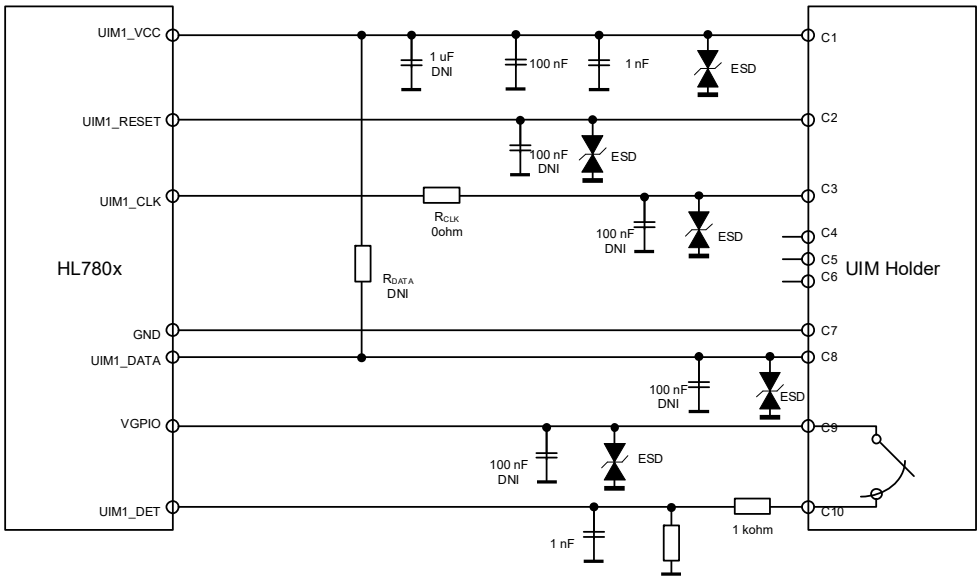


Figure 6-1: EMC and ESD Components Close to the USIM

6.3 USB Interface

The USB interfaces requires 90Ω differential pair routing to the host side.

For USB operation, USB_VBUS is a mandatory connection. The host must ensure USB_VBUS is provided before establishing USB communication.

When the USB interface is externally accessible, ESD protection is required on the USB_VBUS, USB_D+ and USB_D- signals.

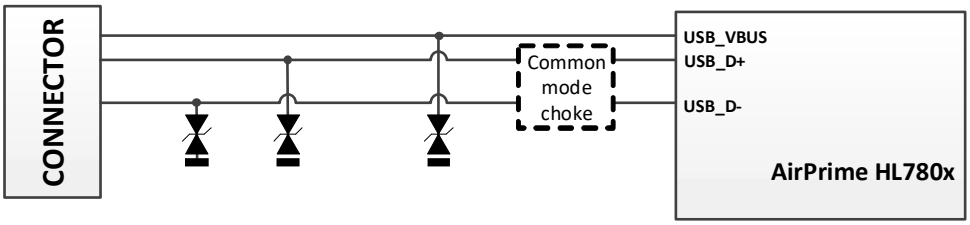


Figure 6-2: ESD Suppressors for USB FS

Semtech recommends using the following for ESD and EMI protection:

- ESD diodes — INNOCHIPS ULCE0505A015FR for USB data lines, and Diodes Inc D8V0L1B2LP3-7 for USB_VBUS
- Optional common mode choke for EMI protection, depending on customer requirements — Panasonic EXC24CG900U

6.4 ESD Protection for I/Os

ESD protection is highly recommended where module signals (GPIO, UART, H/W control, Indication, ADC, Clock) are externally accessible and potentially subjected to ESD by the user. Semtech recommends using Diodes Inc D8V0L1B2LP3-7.

6.5 Hibernate — Isolation Requirements

While the module is in Hibernate mode, the host platform (MCU) interfaces can remain powered.

Important: *To prevent these signals from back-powering the module, the host platform should make sure to isolate them — the signals should not be driven high (e.g. > 0.2 V).*

To ensure the host platform does not back-power the module:

- The host can add a buffer circuit to isolate module I/O during Hibernate. Sierra Wireless recommends using VGPIO to tristate I/O signals.
- The MCU can tristate any I/O that does not have an external PU/PD.

Note: A buffer is not required in Lite Hibernate mode.

If adding a buffer circuit, consider the signal type:

- Bidirectional (Input/Output) signals — For module I/O signals (e.g. GPIOs), an analog switch that can tri-state both the output and the input can be used (e.g. Texas Instruments TMUX1511). As shown in Figure 6-3, I/O signals connected to the buffer will be tri-stated.
- Directional (Input) signals — For module inputs (e.g. UART1_TX), a logic buffer with output tri-state mode can be used (e.g. Texas Instruments SN74LVC1G126). As shown in Figure 6-4, the signal is controlled and, when disabled, the output signal is tri-stated.

Note: Parts and usage descriptions above are intended as examples to assist the host platform designer in developing an appropriate solution for the platform. Selection and use of specific parts is the responsibility of the host platform designer.

Control of the buffer circuit is based on the status of VGPIO — for details, see VGPIO Monitoring and Buffer Control.

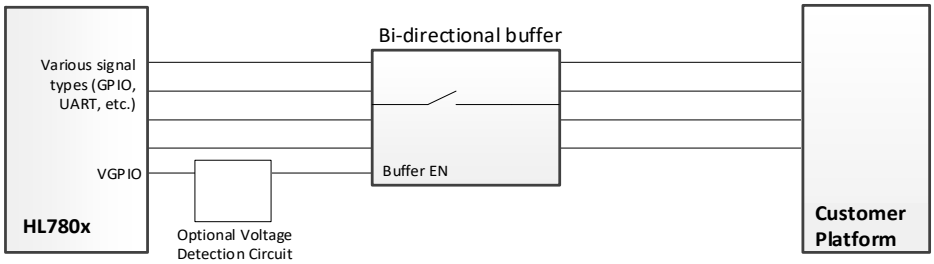


Figure 6-3: Example — Buffer – Bidirectional Signal

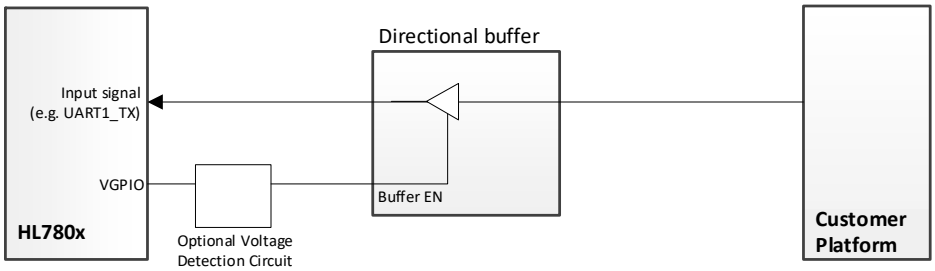


Figure 6-4: Example — Buffer – Directional Signal

6.5.1 VGPIO Monitoring and Buffer Control

Because the host platform can remain powered in Hibernate and Reset states, the host platform must react quickly, when VGPIO transitions low, to ensure signals do not back-power the module.

The host platform can monitor VGPIO to determine the HL780x module's current operating mode — for details, see VGPIO.

To ensure faster detection of VGPIO transitions, Sierra Wireless recommends adding an optional voltage detection circuit (as shown in Figure 6-3 and Figure 6-4) to monitor and detect the transition low, and then control (enable/disable) the associated buffer circuit.

Note: VGPIO can be used to directly connect to the buffer enable signal but the host platform must ensure that all host outputs are not driven high (i.e. > 0.2 V) before the module enters Hibernate mode.

6.6 Radio Frequency Integration

The HL780x is equipped with an external antenna.

6.6.1 Antenna Matching Circuit

A 50Ω line matching circuit between the module, the customer's board and the RF antenna is required as shown in Figure 6-5.

Because matching is dependent on the customer's platform, values marked as 'TBD' for the recommended components must be determined by the customer.

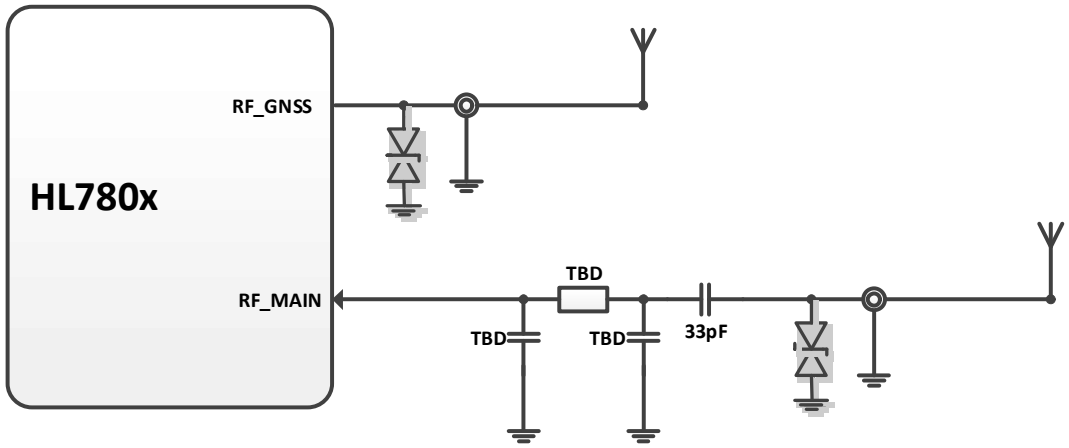


Figure 6-5: Antenna Connection

Semtech recommends using the following ESD diodes:
- TVS component
- Panasonic EZAEG1N50AC for RF_MAIN
- Diodes Inc. D5V0X1B2LP3-7 for RF_GNSS

7: Reliability Specification

The HL780x will be tested against the Semtech Industrial Reliability Specification defined below.

7.1 Preconditioning Test

Per JESD22A113, this tests the preconditioning of non-hermetic surface mount devices prior to reliability testing.

Table 7-1: Preconditioning Test

Designation	Condition
Preconditioning Test PCRM	2 reflow cycles with Tmax 245-250°C

7.2 Performance Test

Table 7-2: Performance Test

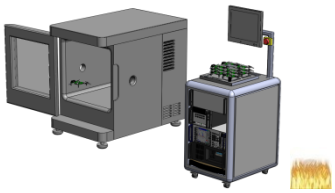
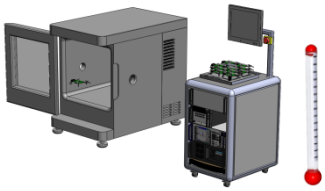
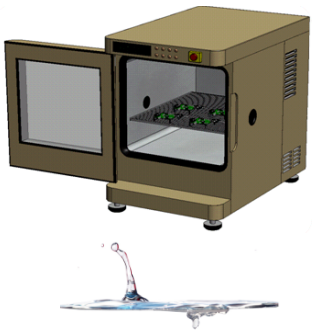
Designation	Condition
Performance Test PT3T & PTRT 	Standard: N/A

	Special conditions:
	▪ Temperature:
	  ▪ Class A: -30°C to +70°C
	  ▪ Class B: -40°C to +85°C
	  ▪ Rate of temperature change: ± 3°C/min
	▪ Recovery time: 3 hours

	Operating conditions: Powered
	Duration: 14 days

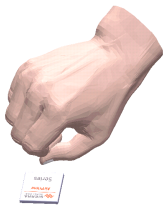
7.3 Aging Tests

Table 7-3: Aging Tests

Designation	Condition
High Temperature Operating Life test HTOL 	Standard: IEC 60068-2-2, Test Bb
	Special conditions: ▪ Temperature: +85°C ▪ Temperature variation: 1°C/min
	Operating conditions: Powered ON with a power cycle of 45 minutes ON and 15 minutes Idle
	Duration: 20 days
Thermal Shock Test TSKT 	Standard: IEC 60068-2-14, Test Na
	Special conditions: ▪ Temperature: -40°C to +85°C ▪ Temperature Variation: less than 30s ▪ Number of cycles: 300 ▪ Dwell Time: 10 minutes
	Operating conditions: Unpowered
	Duration: 7 days
Humidity Test HUT 	Standard: IEC 60068-2-3, Test Ca
	Special conditions: ▪ Temperature: +85°C ▪ RH: 85%
	Operating conditions: Powered on, DUT is powered up for 15 minutes and OFF for 15 minutes.
	Duration: 10 days

7.4 Characterization Tests

Table 7-4: Characterization Tests

Designation	Condition
Low Temperature and Cold Start Cycles LTCS	Special conditions: ▪ Temperature: -40°C ▪ AT commands read or write memory
	Operating conditions: 5 mins powered ON, 30 mins powered OFF (1 power cycle)
	Duration: 5 days
Component Solder Wettability CSW 	Standard: JESD22 - B102, Method 1/Condition C, Solderability Test Method
	Special conditions: ▪ Test method: Surface mount process simulation test (preconditioning 16 h ±30 minutes dry bake)
	Operating conditions: Unpowered
	Duration: 1 day
Unprotected Free Fall Test FFT1 	Standard: IEC 680068-2-32, Test Ed
	Special conditions: ▪ Number of drops: 6 drops per unit (1 drop per direction: ±X, ±Y, ±Z) ▪ Height: 1m
	Operating conditions: Unpowered
	Duration: 1 day

8: Legal Information

8.1 RoHS Directive Compliance

Semtech certifies that to the best of its knowledge, the HL7800, HL7800-M, and HL7802 modules are RoHS Compliant, as defined and detailed in the module-specific RoHS Compliance Statements available at source.sierrawireless.com.

8.2 Disposing of the Product

This electronic product is subject to the EU Directive 2012/19/EU for Waste Electrical and Electronic Equipment (WEEE). As such, this product must not be disposed of at a municipal waste collection point. Please refer to local regulations for directions on how to dispose of this product in an environmental friendly manner.

8.3 Compliance Acceptance and Certification

The AirPrime HL7800/AirPrime HL7800-M/AirPrime HL7802 is designed to be compliant with the 3GPP Release 9 UTRA and Release 13 E-UTRA Specifications for Mobile Terminated Equipment.

Final regulatory and operator certification requires regulatory agency testing and approval with the fully integrated UE host device incorporating the AirPrime HL7800/AirPrime HL7800-M/AirPrime HL7802 module.

The OEM host device and, in particular, the OEM antenna design and implementation will affect the final product functionality, RF performance, and certification test results.

Note: Tests that require features not supported by the AirPrime HL7800/AirPrime HL7800-M/AirPrime HL7802 (as defined by this document) are not supported.

8.4 Regulatory and Industry Approvals/Certifications

The AirPrime HL7800/AirPrime HL7800-M/AirPrime HL7802 module is designed to meet, and upon commercial release, will meet the requirements of the following regulatory bodies and regulations, where applicable:

- Federal Communications Commission (FCC) of the United States
- The Certification and Engineering Bureau of Industry Canada (IC)
- (HL7800/HL7800-M) South Korea (KC)
- (HL7800/HL7800-M) The National Communications Commission (NCC) of Taiwan, Republic of China
- Regulatory Compliance Mark (RCM), Electrical Regulatory Authorities Council (Australia and New Zealand)
- Radio Equipment Directive (RED) of the European Union
- Ministry of Internal Affairs and Communications (MIC) of Japan

Upon commercial release, the following industry certifications will have been obtained, where applicable:

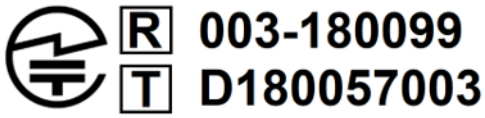
- GCF
- PTCRB

Additional certifications and details on specific country approvals may be obtained upon customer request — contact your Semtech account representative for details.

Additional testing and certification may be required for the end product with an embedded HL7800/HL7800-M/HL7802 module and are the responsibility of the OEM. Semtech offers professional services-based assistance to OEMs with the testing and certification process, if required.

8.5 Japan Radio and Telecom Approval

The HL7800 and HL7800-M modules have been granted Japan radio and telecom approvals with the approval numbers shown below.



Additional approval may be required for end products embedding HL7800 or HL7800-M modules.

8.6 Important Compliance Information for North American Users

The AirPrime HL7800/AirPrime HL7800-M/AirPrime HL7802 modules have been granted modular approval for mobile applications under:

- AirPrime HL7800 — FCC ID: N7NHL78 and IC: 2417C-HL78
- AirPrime HL7800-M — FCC ID: N7NHL78M and IC: 2417C-HL78M
- AirPrime HL7802 — FCC ID: N7NHL7802 and IC: 2417C-HL7802

Integrators may use these modules in their end products without additional FCC/IC (Industry Canada) certification if they meet the following conditions. Otherwise, additional FCC/IC approvals must be obtained.

1. The end product must use the RF trace design approved with the HL7800, HL7800-M, or HL7802. The Gerber file of the trace design can be obtained from Semtech upon request.
2. At least 20 cm separation distance between the antenna and the user's body must be maintained at all times.

3. To comply with FCC/IC regulations limiting both maximum RF output power and human exposure to RF radiation, the maximum antenna gain including cable loss in a mobile-only exposure condition must not exceed the limits stipulated in Table 8-1.

Table 8-1: Product Name Antenna Gain Specifications

Device	Technology	Band	Frequency (MHz)	Maximum antenna gain (dBi)	
				Standalone	Collocated
AirPrime HL7800 AirPrime HL7800-M AirPrime HL7802	LTE	B2	1850–1910	8	6
		B4	1710–1755	6	6
		B5	824–849	6	4
		B12	699–716	6	3
		B13	777–787	6	3
		B25	1850–1915	6	6
		B26	814–849	6	4
		B66	1710–1780	6	6
AirPrime HL7802	GPRS/EDGE	GPRS G850	824–849	3	1
		GPRS G1900	1850–1910	3	3

4. The HL7800, HL7800-M, or HL7802 may transmit simultaneously with other collocated radio transmitters within a host device, provided the following conditions are met:
   - Each collocated radio transmitter has been certified by FCC/IC for mobile application.
   - At least 20 cm separation distance between the antennas of the collocated transmitters and the user's body must be maintained at all times.
   - The radiated power of a collocated transmitter must not exceed the EIRP limit stipulated in Table 8-2.

Table 8-2: HL7800 / HL7800-M / HL7802 Collocated Radio Transmitter Specifications

Device	Technology	Frequency (MHz)	EIRP Limit (dBm)
Collocated transmitters[a]	WLAN 2.4 GHz	2400–2500	30
	WLAN 5 GHz	5150–5850	30
	BT	2400–2500	16
	WiGig	58320–62640	25

a. Valid collocated transmitter combinations: WLAN+BT; WiGig+BT. (WLAN+WiGig+BT is not permitted.)

5. A label must be affixed to the outside of the end product into which the HL7800, HL7800-M or HL7802 is incorporated, with a statement similar to the following:
   - (HL7800) — **This device contains FCC ID: N7NHL78 / IC:2417C-HL78**.
   - (HL7800-M) — **This device contains FCC ID: N7NHL78M / IC:2417C-HL78M**.
   - (HL7802) — **This device contains FCC ID: N7NHL7802 / IC:2417C-HL7802**.
6. A user manual with the end product must clearly indicate the operating requirements and conditions that must be observed to ensure compliance with current FCC/IC RF exposure guidelines.

The end product with an embedded HL7800, HL7800-M or HL7802 may also need to pass the FCC Part 15 unintentional emission testing requirements and be properly authorized per FCC Part 15.

Note: If this module is intended for use in a portable device, you are responsible for separate approval to satisfy the SAR requirements of FCC Part 2.1093 and IC RSS-102.

A: References

For more details, several references can be consulted, as detailed below.

A.1 Web Site Support

Check source.sierrawireless.com for the latest documentation available for HL780x modules.

A.1.1 Reference Documents

- HL78xx Series Customer Process Guidelines
  Reference: 41112095
- HL78xx AT Commands Interface Guide
  Reference: 41111821
- HL Series Development Kit User Guide
  Reference: 4114877
- HL78xx Low Power Modes Application Note
  Reference: 2174229
- HL78xx Customization Guide Application Note
  Reference: 2174213
- Ready-to-Connect Module Integration Guide
  Reference: 41113385
- HL78xx Firmware Update Methods Application Note
  Reference: 2174259

A.2 Ordering Information

Table 1-1: Ordering Information

Model Name	Description	Part Number
HL7800	HL7800 embedded module	Contact Semtech for the latest SKU.
HL7800-M	HL7800-M embedded module	Contact Semtech for the latest SKU.
HL7802	HL7802 embedded module	Contact Semtech for the latest SKU.
DEV-KIT	HL780x Development Kit	6001210

A.3 Abbreviations

Table 1-2: Terms and Abbreviations

Abbreviation	Definition
Active state	All sub-systems, including the MAP process, are up and running. User can access module via UART (e.g. to configure/query module settings/states, and send/receive data.
ADC	Analog to Digital Converter
AT	Attention (prefix for modem commands)
AT-READY	Module is initialized and ready to accept AT commands
Cat-M1	LTE enhanced Machine Type Communication (eMTC) Category M1 (3GPP Release 14)
Cat-NB1	LTE Narrowband Internet of Things (NB-IoT) Category NB1 (3GPP Release 14)
CF3	Common Flexible Form Factor
CLK	Clock
DTR	Data Terminal Ready
DRX	Discontinuous Reception
eDRX	Extended DRX
EIRP	Equivalent Isotropically Radiated Power
EMC	Electro-Magnetic Compatibility
EMI	Electro-Magnetic Interference
EN	Enable
ESD	Electro-Static Discharges
ETSI	European Telecommunications Standards Institute
GLONASS	Global Navigation Satellite System
GND	Ground
GNSS	Global Navigation Satellite System

Table 1-2: Terms and Abbreviations (Continued)

Abbreviation	Definition
GPIO	General Purpose Input Output
GPRS	General Packet Radio Service
GPS	Global Positioning System
GSM	Global System for Mobile communications
Hi Z	High impedance (Z)
IC	Industry Canada
I/O	Input/Output
LED	Light Emitting Diode
MAX	Maximum
MIN	Minimum
N/A	Not Applicable
PA	Power Amplifier
PC	Personal Computer
PCB	Printed Circuit Board
PCL	Power Control Level
periodic TAU	See TAU
PSM	Power Save Mode
PTW	Paging Transmission Window
PWM	Pulse Width Modulation
RF	Radio Frequency
RST	Reset
RTC	Real Time Clock
RX	Receive
SIM	Subscriber Identification Module
SINR	Signal to Interference plus Noise Ratio
SW	Software
TAU	Tracking Area Update TAU — An update sent when the PSM parameters are changed or when the module changes location. periodic TAU — Sent by the module to notify its availability to the network.
TBC	To Be Confirmed
TBD	To Be Determined To Be Defined

Table 1-2: Terms and Abbreviations (Continued)

Abbreviation	Definition
TP	Test Point
TX	Transmit
TYP	Typical
UART	Universal Asynchronous Receiver-Transmitter
UICC	Universal Integrated Circuit Card
USB	Universal Serial Bus
UIM	User Identity Module
UMTS	Universal Mobile Telecommunications System
USIM	UMTS Subscriber Identity Module
VBAT_BB	Main Supply Voltage from Battery or DC Adapter
VSWR	Voltage Standing Wave Ratio