



Melody Audio I2S and TLV320AIC33 Test Setup

Application Note



SIERRA
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41110793
Rev 1

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Revision History

| Revision number | Release date | Changes |
|-----------------|----------------|-----------------------------------|
| 1 | March 22, 2017 | Initial revision in SWI Template. |

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>> 1: Introduction

In order to verify Melody Audio I2S interface functionality Sierra Wireless employs several steps:

1. Scope traces
2. Logic analyser traces
3. Full functional test with a third party codec and development board.

Please read this document to understand how to verify Melody I2S operation using a third party codec using the TLV320AIC33EVM board by TI.

»» | 2: Equipment and Procedure

Equipment used

1. BC127 Development Kit
2. TLV320AIC33EVM Board
3. Jumper cables for connecting the two boards (5x female-female)

Procedure

1. Download and set-up any required software for the TLV320AIC33EVM Board All document and software available from TI here: <https://www.ti.com/tool/tlv320aic33evm-pdk>.
2. Ensure TLV320AIC33EVM is configured to defaults, as specified in TI documentation.
3. Ensure BC127 Dev kit is reset to defaults by typing *RESTORE* then *WRITE* then *RESET*.
4. Follow instructions in *Configuring the TLV320AIC33*.
5. Follow instructions in *Configuring BC127 Development Kit*.
6. Follow instructions in *Connecting I2S lines TLV320AIC33EVM and BC127 Dev Kit*.
7. Plug in a headset into the HEADSET jack of the TLV320AIC33EVM.
8. Connect to your BC127 from a phone and start playing music.
9. Music will be heard on the headset.

3: Configuring the TLV320AIC33

Turn switch SW2.4 (USB I2S) to OFF.

Please ensure that the setting on your TLV320AIC33 match the ones on the figures below. The relevant parameters are highlighted in red rectangles.

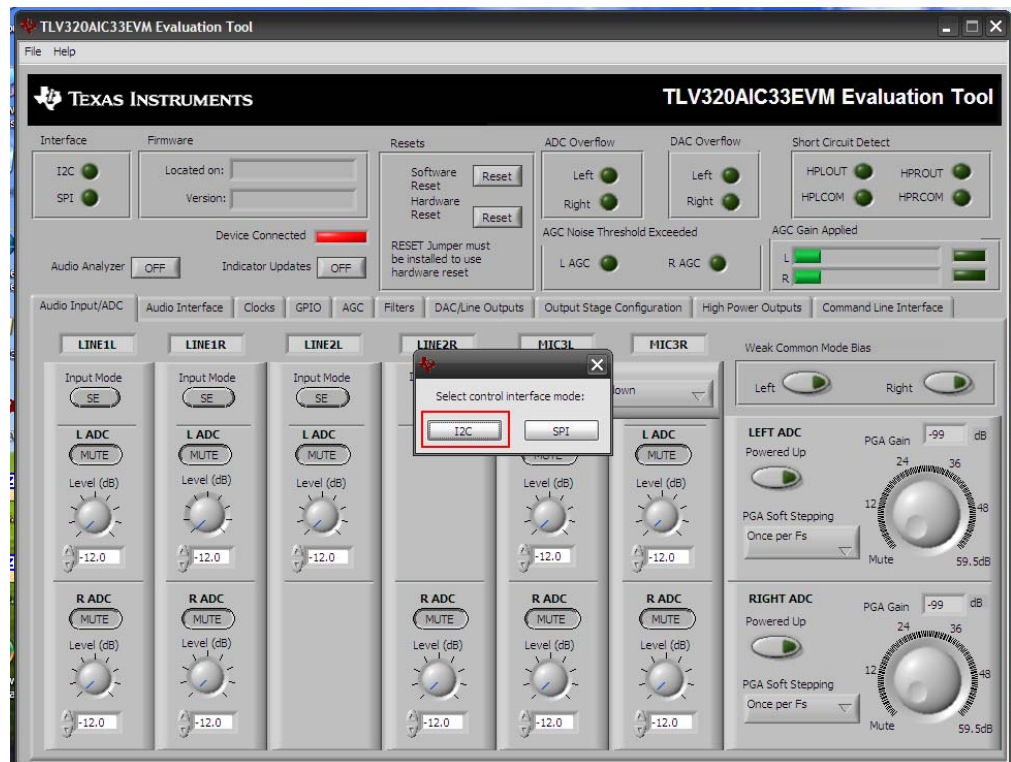


Figure 3-1: Select I2C transport (Default for TLV320 EVM)

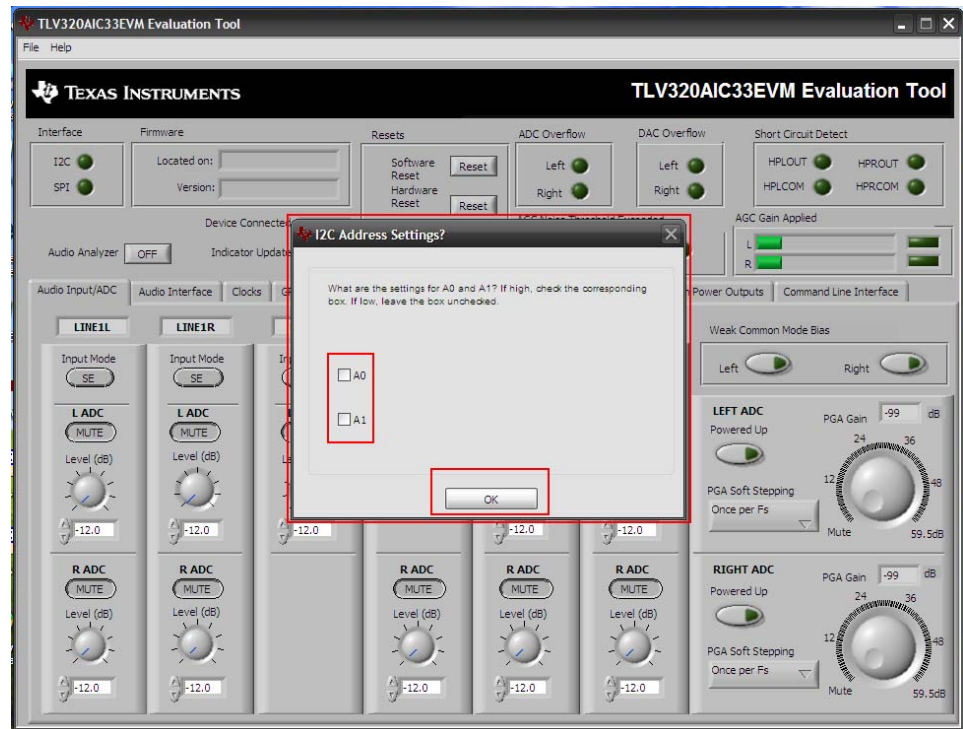


Figure 3-2: Leave A0 and A1 unticked (Default for TLV320 EVM)

When set-up for I2S slave, use I2S BCLK to generate system clocks. This ensures that the codec will operate at arbitrary sample rates, and that there will be no sample rate mismatch between the I2S source and the TVM320 DACs.

Melody BCLK is calculated as follows:

$$BCKL = F_s * 16 * 2 * 2$$

For $F_s = 44100\text{Hz}$ this will be:

$$BCKL = 44100 * 16 * 2 * 2 = 2822400\text{Hz}$$

For $F_s = 46000\text{Hz}$ this will be:

$$BCKL = 46000 * 16 * 2 * 2 = 2944000\text{Hz}$$

On the TVM320 side, the P, K, R coefficients are determined following the TVM manual, however, for use with Melody $P=1$, $K=32$ and $R=1$ will generate the correct PLLDIV_OUT clock to ensure that the DAC is clocked at the same F_s as the I2S interface.

Since this ratio is constant, the TVM320 can be used with any F_s supported with Melody.

The only constraints here are that any Digital Filtering applied on the TVM320 will need to be developed to produce the appropriate frequency response at the correct sample rate.

Please note that the PLLCLK_IN field is user supplied and not auto-detected. The value of the Actual Fsref and Error fields depends on the PLLCLK_IN field and the position of the Desired Fsref switch. Please note that these field bear no effect on the actual chip clocking.

For example below, the correct BCLK is entered for $F_s 44.1\text{kHz}$.

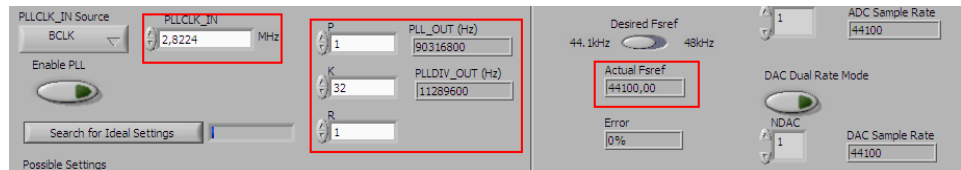


Figure 3-5: Clock indication fields, as described above. I2S is operating at 44100Hz, so the DAC is actually clocked at 44.1kHz

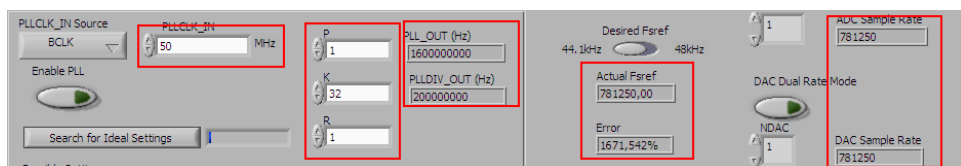


Figure 3-6: Clock indication fields, with wrong input clock supplied. Please note the UI calculated frequencies are wrong. Since I2S is operating at 44.1kHz and the device is slave, the DAC is clocked at 44.1kHz.

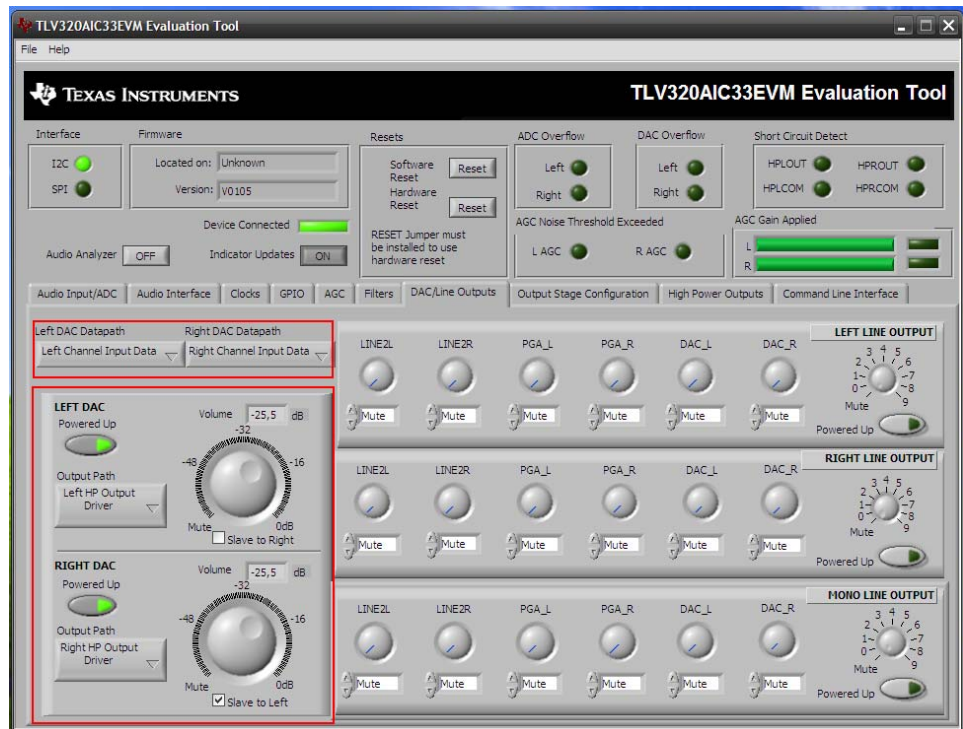


Figure 3-7: DAC configuration

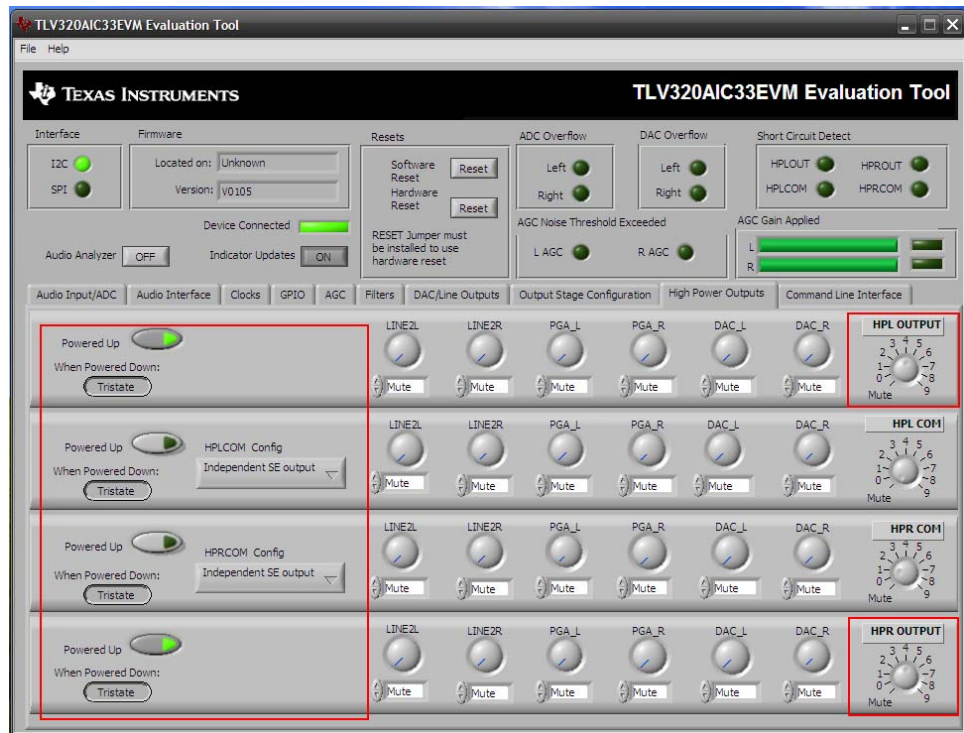


Figure 3-8: High Power Output configuration

>> 4: Configuring the BC127 Development Kit

1. Set SPI/#PCM switch to #PCM to enable digital audio interface.
2. Configure Melody using the following commands:

```
SET AUDIO=3
SET CODEC=0 44100 1
SET I2S=0002
WRITE
RESET
```

>> 5: Connecting I2S lines TLV320A-IC33EVM and BC127 Dev Kit

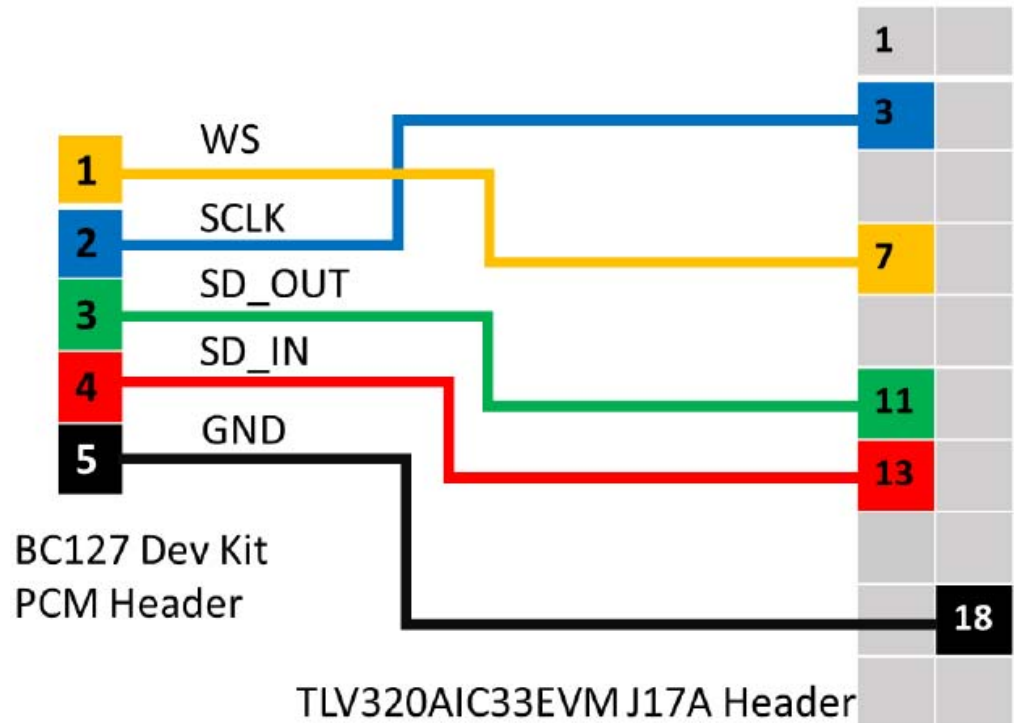


Figure 5-1: Wiring Diagram